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M1 System Management Board

User's Guide

Actel
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

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Introduction

The Actel M1 System Management Board Development Kit provides an excellent platform for developing system management applications and/or applications with a microprocessor. The kit includes a Cortex™-M1-enabled Fusion device, a system management GUI, and a platform (Figure 1) for systems that performs the following functions:

- Power-up detection
- Power sequencing
- Thermal management
- Sleep modes
- System diagnostics
- Remote communications
- Clock generation and management

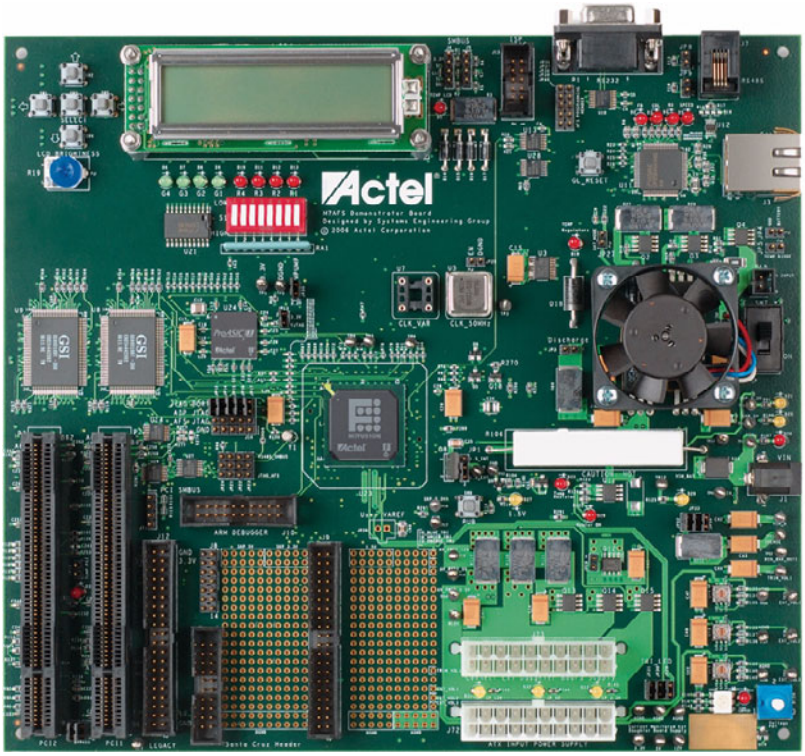

Figure 1. M1 System Management Board

The M1 System Management Board includes an M1AFS1500 device, which is compatible with Cortex-M1, Core8051, and other processors, as well as non-processor-based implementations. The kit's demonstration design uses the MicroC/OS-II on Cortex-M1 with the system management GUI, which is multi-tabbed for board status, application data, IPMI data, and a graphical display of the monitored analog data. In addition, the GUI source code is available for custom modification. All the documentation in this M1 System Management user's guide for the M1-SYSMGMT-DEV-KIT board, fitted with an M1AFS1500 part, is equally applicable to the old M7-enabled board that was fitted with an M7AFS600 device. The board is essentially the same and only the FPGA has been changed. As a result, this guide can also be used as documentation for the older SYSMGMT-DEV-KIT board that featured an ARM® CoreMP7-enabled device. The new M1-enabled board features a much larger AFS device with more embedded nonvolatile memory and a greater programmable silicon space.

The system management GUI (Figure 2, Figure 3 and Figure 4) includes the following tabs:

- Board status
- Application data
- IPMI data
- Graphical display of analog data

The GUI helps users to:

- Monitor power supplies
- Monitor temperature sensors
- Set LEDs and text for display
- Set and read the RTC
- Display embedded Flash contents

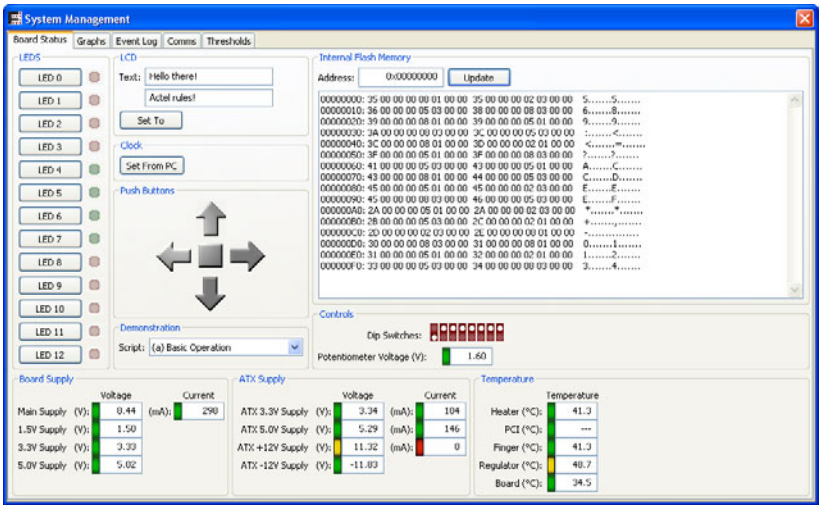

Figure 2. Board Status Tab

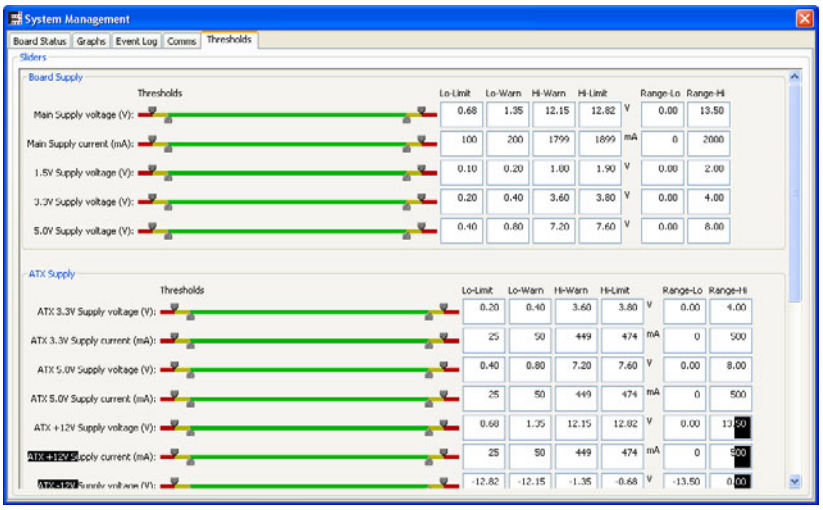

Figure 3. Threshold Tab

Figure 4. Graphs Tab

Design Example

This user's guide utilizes the M1 System Management Board, the System Management software and examples to demonstrate System Management's capabilities. It can also be used as a reference design to jumpstart user application designs, including a firmware platform for re-use. Design examples for the older CoreMP7-enabled board, featuring the M7AFS600 device, may still be found on the Actel web site. Only Cortex-M1-enabled designs should be used with the M1-SYSMGMT-DEV-KIT board.

The System Management software enables the user to run tests for demonstration purposes, using a laptop or PC connected via serial communications link to the board. These are the main features:

- View the board's status in real-time.
- Observe all voltages, current and temperature in specific places on the board for real-time diagnostics.
- Test asynchronous buttons on the board and view the result in the software upon depressing any given button.
- Threshold control and event logging to control the warning limits within a given range and log specific events as a result of these threshold levels.

Future releases will extend the capabilities to include power sequencing and a range of other more advanced features.

Document Contents

Chapter 1 – Contents and System Requirements describes the contents of the M1 System Management Kit.

Chapter 2 – Hardware Components describes the components of the System Management Board and the system requirements for the System Management software installation.

Chapter 3 – System Management Software describes the System Management user interface.

Chapter 4 – Setting Thresholds describes how to set the thresholds graphically or using the sliders.

Chapter 5 – Demonstration Scripts provides simple instructions of the basic scripts for the System Management software.

Appendix A – M1AFS1500-FG484 Pin List

Appendix B – A3P250-FG144 Pin List

Appendix C – Board Schematics

Appendix D – Board Stackup

1 Contents and System Requirements

This chapter details the contents of the Cortex-M1-enabled Fusion-based System Management Kit and lists the necessary components required to use it.

Kit Contents

- M1 System Management Board
- Switching brick power supply (rated from 110 V to 240 V AC) from 50 Hz to 60 Hz input, an providing 9 V DC output at up to 2 A, part number DTS090220UP5P-SZ from CUI, Inc.
- Power cables and adapter
- RS-232 cable
- User's guide

Optional:

- 7.2 V 2100 mAh NiMH battery
- Temperature diode two-pin flex cable
- ATX power supply
- 10-pin JTAG cable for Fusion to Fusion programming
- FlashPro v5.0
- Libero IDE GOLD
- CD with design/application examples

System Requirements

The system requirements for the System Management Board and the System Management software:

- ATX power supply, which can connect directly to the board
- Actel M1AFS1500-FG484 Demonstrator Board
- Serial communications cable (RS-232)
- PC running Windows® XP. Windows XP is the only supported operating system.
- Serial communications port, preferably COM Port 1. Future versions will incorporate ethernet communication.

2 Hardware Components

This chapter describes the hardware components of the M1 System Management Board.

Power Supplies

A 9 V power supply is provided with the kit. The 9 V brick is connected to the J1 connector on the board. This power supply feeds the input voltage of three LDO-type regulators—U1, U2, and U3—through a slide switch, SW7. The switch toggles between two positions On-Off. The regulators provide three voltages 5 V, 3.3 V and 1.5 V.

Table 2-1 illustrates LEDs provided to ensure that all the voltage reach the correct state.

Table 2-1 · LEDs

LED	Reference Designator	SW7		Description
		Off	On	
Red LED	D26	On	On	9 V input voltage before switch SW7
Yellow LED	D29	Off	On	9 V input voltage after switch SW7
Yellow LED	D25	Off	On	5 V supply
Yellow LED	D21	Off	On	3.3 V supply
Yellow LED	D27	Off	On	1.5 V supply

Jumper Settings

JP13 is a two-pin jumper that provides V_{JTAG} with a 3.3 V supply. V_{JTAG} is needed to power up the JTAG circuitry of the M1AFS1500-FG484 and A3P250-FG144 parts. While programming these two parts, make sure this location has a jumper.

JP35 is a two-pin jumper that provides V_{PUMP} with a 3.3 V supply. V_{PUMP} is needed while programming the M1AFS1500-FG484 and A3P250-FG144 parts. While programming these two parts, make sure this location has a jumper.

JP1 is a three-pin jumper that provides 1.5 V to the M1AFS1500-FG484 part.
JP1.1-2 connects the 1.5 V going to the M1AFS1500-FG484 part to 1.5_INT. This voltage is generated internally by the M1AFS1500-FG484 part through an on-chip regulator powered by the 3.3 V supply. JP1.2-3 connects the 1.5 V going to the M1AFS1500-FG484 part to voltage 1.5_EXT. This voltage is generated externally by the on-board regulator U3.

M1AFS1500-FG484

This is the Actel ARM-enabled Fusion FPGA demonstrated on the System Management Board and located at U23. Refer to "M1AFS1500-FG484 Pin List" on page 47 for pin list information.

A3P250-FG144

This device is an Actel FPGA used purely due to the limitation on the number of I/Os on the M1AFS1500-FG484 part. This device controls all user interfaces: LCD, key pads, DIP switch, LEDs, etc. The M1AFS1500-FG484 and the A3P250 device communicate via a UART interface using the Actel CoreUART IP. Refer to "A3P250-FG144 Pin List" on page 63 for pin list information.

Clocks and Reset

CLK Source

A 50 MHz clock with 50 ppm stability is provided at location U5. This clock is the clock source for the A3P250-FG144 device at U24 (pin F12) and the M1AFS1500-FG484 device at location U23 (pin A3). A user clock is also provided at location U7. Any 3.3 V clock can be installed in the socket of this location. The user clock feeds only to the M1AFS1500-FG484 device.

A 32.768 kHz crystal is provided at location Y1 on the board. This is the crystal used to start the internal RTC counter on the M1AFS1500-FG484 device.

Jumper Settings

JP25 is a two-pin jumper. By default there is no jumper at this location. In this state, the clock is free running. If the jumper is placed, it puts the enable pin of the clock to GND and shuts off the clock oscillator.

PUB Signal

The PUB signal of the M1AFS1500-FG484 unit has a 1 MΩ pull to 3.3 V along with a push button SW8 to provide an active low pulse.

Reset

An active low pin reset is provided by the push button SW6. The reset signal goes to the M1AFS1500-FG484 device at pin B17 and A3P250 device at pin E2.

Programming

Different programming techniques are provided on the System Management Board.

FlashPro3

In-system programming is provided to enable programming of all devices on the JTAG boundary scan chain, see Figure 2-1.

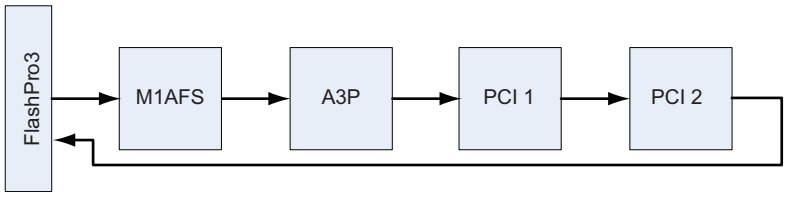

Figure 2-1. FlashPro3 In-System Programming Setup

Place all jumpers as shown in Table 2-2 and plug in the FlashPro3 connector on J13 to start programming .

Table 2-2 · Jumpers Settings for In-System Programming

Jumper	Setting for In-System Programming
JP35	1-2
JP13	1-2
JP12	1-2

Table 2-2 · Jumpers Settings for In-System Programming (Continued)

Jumper	Setting for In-System Programming
JP14	1-2
JP15	1-2
JP16	1-2
JP17	1-2
JP10 (If PCI1 is not in chain)	1-2
JP11 (If PCI2 is not in chain)	1-2

M1AFS1500-FG484 to A3P Programming

The board can be configured to program an A3P250 device with the M1AFS1500-FG484 device, see Figure 2-2. Table 2-3 shows the jumpers settings required.

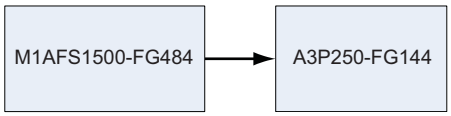

Figure 2-2. M1AFS1500-FG484 to A3P Programming Setup

Table 2-3 · Jumper Settings for M1AFS1500-FG484 to A3P250-FG144 Programming

Jumper	Setting for In-System Programming
JP35	1-2
JP13	1-2
JP12	2-3
JP14	2-3
JP15	2-3
JP16	2-3
JP17	2-3
JP24	2-3
JP21	2-3
JP22	2-3
JP23	2-3

External Programming

The System Management Board can program an external JTAG compliant device with the M1AFS1500-FG484 device. Figure 2-3 shows the external programming setup. See Table 2-4 for the jumper settings.

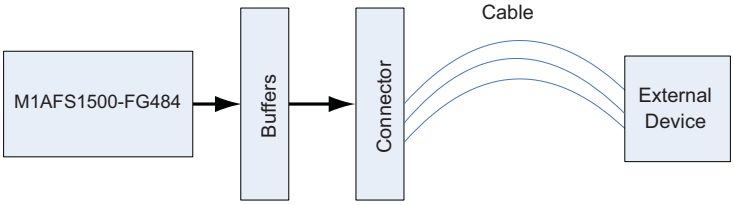

Figure 2-3. External Programming Setup

Table 2-4 · Jumper Settings for External Programming

Jumper	Setting for Programming External Device
JP24	2-3
JP21	2-3
JP22	2-3
JP23	2-3

Figure 2-4 shows the JTAG complaint device.

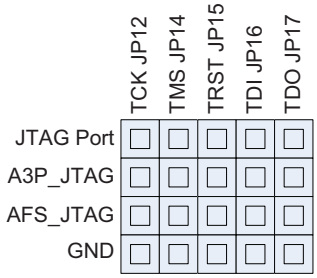

Figure 2-4. JTAG Compliant Device

DIP Switch, LEDs and Push Buttons

DIP Switch S1

Eight signals are provided for debug purposes. The signals toggle between 0 V (low) and 3.3 V (high) logic. The signals are controlled by the A3P250 FPGA.

LEDs

Four green LEDs (D6, D7, D8 and D9) and four red LEDs (D10, D11, D12 and D13) are provided for debug purposes. The LEDs are controlled by the A3P250 FPGA. If the signals are at logic high, the LEDs are On. If the signals are driven low, the LEDs are Off.

Push Buttons

Five push buttons are provided at SW1, SW2, SW3, SW4 and SW5, see Figure 2-5. These push buttons are located near the LCD display and are used to navigate the LCD screen for different tests/demo scripts. These signals are driven to the A3P250 device.

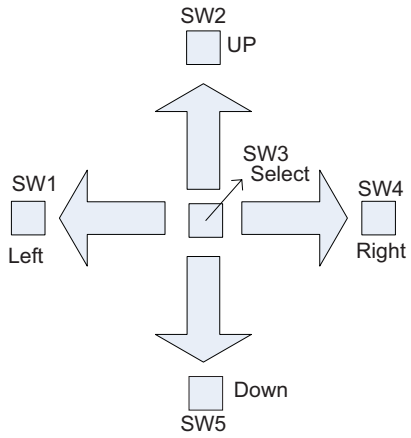

Figure 2-5. Push Buttons

LCD Display

An 8-bit, 16 x 2 character LCD display (part# LCMS01602DSFC) is provided on the board at LCD1. The A3P250-FG144 device controls the 8-bit signals, control signals, and backlight of the display. The contrast of the LCD display can be changed using the potentiometer at R19.

Memory

An external synchronous SRAM (part# 816018) is provided with 1 M x 32 bits memory, located at U8 and U9 on the board.

Flash memory (part# M29W160ET) is provided with 1 M x 32 bits of memory, located at U25 and U26 on the board.

All signals interface with the M1AFS1500-FG484 device at U23.

PCI

Two PCI ports, P2-PCI_1 and P3-PCI_2, are provided. These two ports interface with the M1AFS1500-FG484 device. The PCI bus supports the 3.3 V 32-bit operations at a system frequency of 33 MHz and 66 MHz and is compliant with the local bus PCI 2.3 specifications.

Legacy Connector

A 40-pin 0.100 in x 0.100 in connector (J12) is provided for debug purposes. All Actel demonstration and evaluation boards are populated with this connector so they can interface with other Actel boards.

All I/Os on the legacy connector are shared with the PCI signals.

Note: **Do not exercise the PCI connector and the Santa Cruz connector header simultaneously.**

Santa Cruz Connector Header

A set of three headers (J8, J9, and J11), per the Santa Cruz header specification, are provided for debug purposes and installing compatible daughter boards. All I/Os on the Santa Cruz header are shared with the PCI signals.

Note: Do not exercise the PCI connector and the Santa Cruz connector header simultaneously.

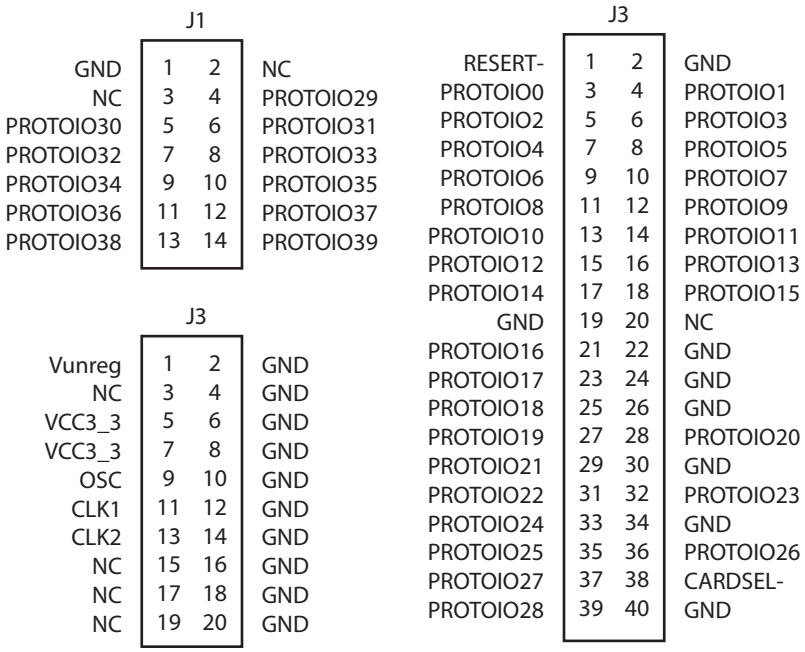

Figure 2-6. Santa Cruz Connector Pinout

ARM Debugger

A 20-pin port (J10) is provided (see Figure 2-7) for installing an ARM Real View debugger that interfaces with the M1AFS1500-FG484 device.

Note: While using the debugger to run the software, add a jumper from JP16 pin 1 to JP17 pin 1. This will make the M1AFS1500-FG484 the only part in the chain.

Figure 2-7. ARM Debugger

Ports

RS232

This kit contains one RS-232 port with a MAX3221 transceiver that can be used for communications between the M1AFS1500-FG484 device and a common serial port found on a PC or other RS-232 compatible device.

Note: The RS-232 interface does not support hardware RTS/CTS hand shaking. The default configuration has the RTS and CTS shorted together to create a loopback connection.

RS485

This kit contains one RS485 2-wire port with a MAX3362 that can be used for communications between the M1AFS1500-FG484 device and a RS485 port. Necessary terminating resistors are provided on the board.

Ethernet 10/100 PHY

One MII ethernet port is provided on the part. It uses a DP83846A transceiver chip and an RJ-45 connector. This directly interfaces with the M1AFS1500-FG484 device. Four LEDs are provided along with the port. See Table 2-5.

Table 2-5 · LED Description

LED Reference Designator	Silkscreen
D2	FD
D3	COL
D4	RX
D5	SPEED

SMBUS Port

Three ports (J4, J5, and J71) are provided for SMBus communications. All signals directly interface with the M1AFS1500-FG484 device. The connections are shown in Table 2-6 and Table 2-7 on page 17. 0.100 in x 0.100 in center-to-center connectors are used as the interface. 1.8-kΩ pull-ups are used for all the signals.

Table 2-6 · Jumper Settings

Jumper	Connections
JP21	1-2
JP22	1-2
JP23	1-2
JP24	1-2

Table 2-7 · Connector Settings

Connector	Settings
Pin 1	3.3 V
Pin 2	SCL
Pin 3	SDA
Pin 4	1-GND

ATX Connector Supply

The ATX connections demonstrate the analog function features of the M1AFS1500-FG484 device. The functional description and pin out information is shown in Figure 2-8. All supplies on the ATX power supply can support a maximum of 10 A.

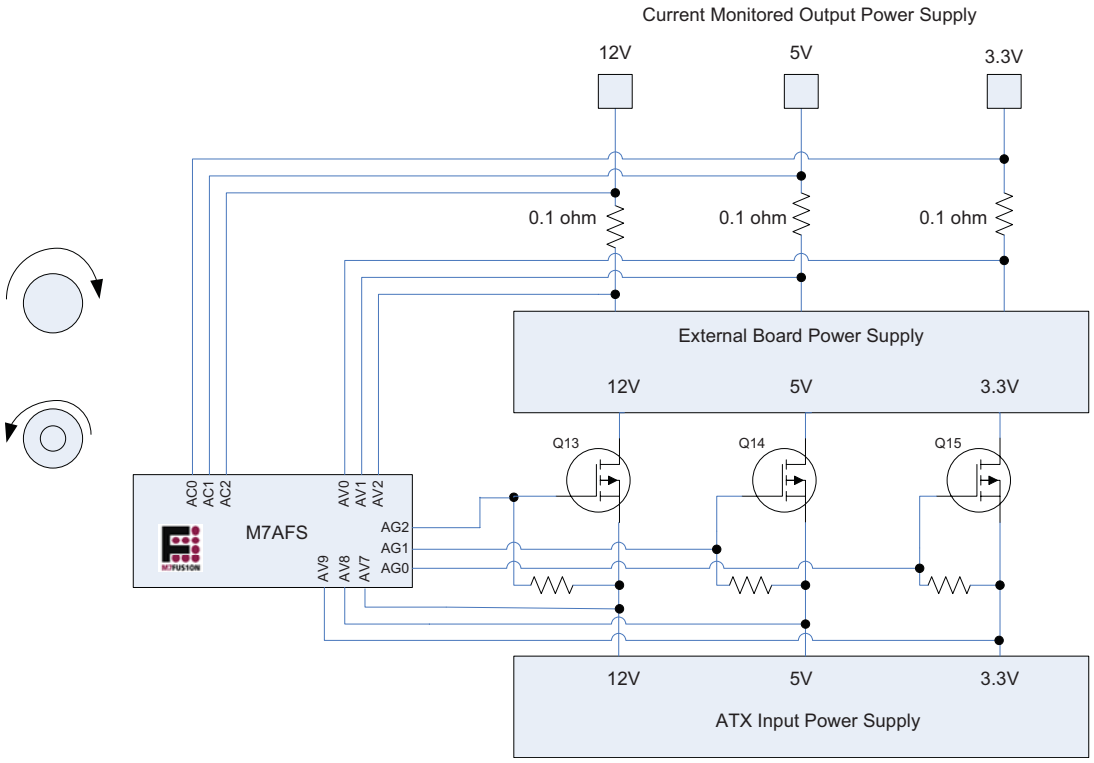

Figure 2-8. M1AFS1500-FG484 Functional Description

Table 2-8 · ATX Main Power Connector Pinout

Pin Number	Signal Function
1	+3.3 VDC
2	+3.3 VDC
3	COM
4	+5 VDC
5	COM
6	+5 VDC
7	COM
8	PWR_OK

Table 2-8 · ATX Main Power Connector Pinout (Continued)

Pin Number	Signal Function
9	+5 VSB
10	+12 VDC
11	+3.3 VDC
12	–12 VDC
13	COM
14	PS_ON#
15	COM
16	COM
17	COM
18	N/C
19	5 VDC
20	5 VDC

Note: Do not plug in the ATX supply to J73.

Table 2-9 · ATX Main Power Connect Pinout by Function

Signal Function	Pin Number
+3.3 VDC	1
+3.3 VDC	2
+3.3 VDC	11
5 VDC	19
5 VDC	20
+5 VDC	4
+5 VDC	6
+5 VSB	9
–12 VDC	12
+12 VDC	10
COM	3
COM	5
COM	7
COM	13
COM	15

Table 2-9 · ATX Main Power Connect Pinout by Function (Continued)

Signal Function	Pin Number
COM	16
COM	17
N/C	18
PS_ON#	14
PWR_OK	8

PS_ON# Signal

The ATX supply plugs in to the J72 connector. The PS_ON# signal is the main switch for the ATX supply. The signal logic is controlled by the signal AFS_PS_ON on the M1AFS1500-FG484 device.

Table 2-10 · PS_ON# Signal Settings

AFS_PS_ON (M1AFS1500-FG484)	PS_ON# (ATX)	ATX Supply
0	1	Off
1	0	On

Power_OK Signal

The PWR_OK signal is an output of the ATX supply. It is a flag set by the ATX supply if all output voltages are good. The PWR_OK is continuously monitored by the M1AFS1500-FG484 device using a regular I/O pin IN_POWER_OK.

Table 2-11 · PWR_OK Signal Settings

PWR_OK (ATX)	IN_POWER_OK (M1AFS)	ATX Supply
0	3.3 V	BAD
5 V	0	GOOD

5VSB Signal

The 5VSB signal on the J72 ATX supply is routed directly to the 5VSB pin on the J73 ATX connector. It does not go to the M1AFS1500-FG484 device. This signal is a sense voltage, which is an input signal to the ATX supply from a plugged in daughter board.

Gate Driver

All input voltages (12 V, 5 V, 3.3 V) are monitored through the AV pads on the M1AFS1500-FG484 device (Figure 2-8 on page 18). The input voltage goes to a P-Type Power MOSFET (FDS7079ZN3). All three voltages can be switched On/Off using the gate driver (AG) controlling the FET.

Table 2-12 · Gate Driver Settings

AG	FET	Output Voltage
Tristate	Off	0 V
On	On	12 V, 5 V, 3.3 V

Note: The gate driver has to be configured as a constant current sink with a 10-µa or 30-µa drive level to get different ramp-rates.

Power-Out Connectors

The output voltage of the FETs goes to two different power-out connectors:

ATX Connector J73 – Any external daughter board can be plugged into this connector. All voltages on the J73 connector are monitored by the M1AFS1500-FG484 device.

MB_PS_ON# – This signal may be driven by an external daughter board. It is an output from the external daughter board. The function of the signal is similar to the PS_ON signal. This signal behaves as a switch to the power going to the external daughter board.

Table 2-13 · MB_PS_ON Settings

MB_PS_ON# (ATX-J73)	AFS_MB_PS_ON (M1AFS)	External DB Power
NC	0	Off
0	1	On
1	0	Off

MB_POWER_OK – This sense/flag signal is an input to the external daughter board. It indicates whether the power going to the external board is good. This signal is driven by the M1AFS1500-FG484 device.

Table 2-14 · MB_POWER_OK Settings

12 V, 5 V, 3.3 V Output Voltage	MB_POWER_OK (M7ADS)
GOOD	3.3 V
BAD	0

Header pins – Header pins are provided for 12 V, 5 V, and 3.3 V in the current monitored external daughter board section of the board. Alligator clips can be used to connect any external board to these pins to power the board. All voltages and current are monitored using 0.1 Ω resistors through the M1AFS1500-FG484 device.

Note: The external board connected to the header pins consumes less than 3 A.

Dummy Loads

Dummy loads can be connected to the output voltages to demonstrate the capability of the M1AFS1500-FG484 device to monitor current in the absence of an external daughter board. Connect the dummy loads as shown in Table 2-15.

Table 2-15 · Dummy Loads Settings

Reference Designator	Load	Output Voltage	Approximate Current
JP32	110 Ω	12 V	109 mA
JP33	39 Ω	5 V	128 mA
JP34	39 Ω	3.3 V	84 mA

Temperature Diodes

Five temperature diodes (MMBT3904) are provided across the board for monitoring environment temperature: heater, regulators, board, PCI, and copper pad.

Heater

Temperature diode Q10 is located very close to the heater element, R161, and monitors the temperature of the heater. The red LED, D22, can be used to toggle if the temperature crosses some threshold.

Regulators

Temperature diode Q7 is located in the middle of all the LDO regulators to monitor the temperature. The red LED D19 can be used to toggle if the temperature crosses some threshold.

Board

Temperature diode Q1 is located beneath the LCD display to monitor average board temperature. The red LED D1 can be used to toggle if the temperature crosses some threshold.

PCI

A two-pin header, JP19, is located between the two PCI connectors. Attach a two-pin cable with a temperature-sensing device to this connector to monitor temperature of the PCI card. The red LED D30 can be used to toggle if the temperature crosses some threshold.

Copper Pad

Temperature diode Q16 is located next to the exposed copper area to monitor the temperature of the exposed copper pad. This pad will be used for calibration purposes to record a stable room temperature. The red LED D34 can be used to toggle if the temperature crosses some threshold.

Potentiometer

A 2-kΩ potentiometer (R150) is provided with a control knob to demonstrate voltage monitoring by exercising an AV pad on the M1AFS1500-FG484 device. The potentiometer is connected across a 5 V signal. The voltage strobe moves

from 0 V to 5 V using the knob control (Figure 2-9).

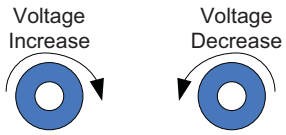

Figure 2-9. Potentiometer Knob Control

Tri-Color LED

A tri-color LED (AAF5060PBESEEVG) is provided on the board. The LED has three colors—blue, orange, and green—controlled by three gate driver (AG) pins from the M1AFS1500-FG484 device. A combination of colors can be turned On to form new colors. To make the tri-color LED operational, place jumpers on JP29, JP30, and JP31, as shown in Table 2-16 and Table 2-17.

Table 2-16 · AG Pads Settings

AG Pads (M1AFS1500-FG484)	LED
Tristate	Off
On-High Current Drive	On

Table 2-17 · Jumpers Settings

Jumpers	LED
JP29	Blue
JP30	Orange
JP31	Green

Note: Set the AG pad in a high current drive mode, which can sink 25 mA.

Heater/FAN Loads

The board has two loads controlled by the gate drivers from the M1AFS1500-FG484 device: heater and fan.

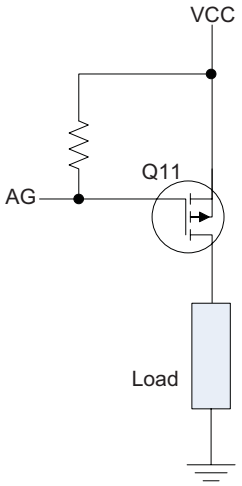

Figure 2-10. Heater/ Fan Loads.

Table 2-18 · AG Pads Settings

AG Pads (M1AFS1500-FG484)	LED
Tristate	Off
On-High Current Drive	On

Note: Set the AG pad in a high current drive mode, which can sink 25 mA.

Heater

A 7.5 Ω wire-wound resistor (R106) is provided on the board. The resistor is a conduction type of heater element that dissipates heat of up to 11 W. The heater is used to demonstrate the temperature variance on the temperature diode (Q10) sitting close to it.

Fan

A 3.3 V fan is provided on the board with a tachometer option to measure the speed of the fan. Each revolution creates two pulses on the tachometer output. The tachometer output signal goes to the A3P250-FG144 device. A connector JP18 is provided in parallel to the fan load to allow removing the fan and adding an external load.

Note: Do not add a load that requires more than 300 mA.

Voltage Monitors

Three monitors are provided on the board to monitor external voltages: EXT_VOL[1:3]. Voltages of an external board can be monitored by using alligator clips to plug into one of the monitor pins. The voltage is monitored using the AV pads of the M1AFS1500-FG484 device. The input voltage (V1) from the external board can be divided down to one of the options below using a 4-pole switch (Table 2-19). Three switches are provided to allow independent division of the external voltages: switch U15 is used for EXT_VOL[1}, switch U17 is used for EXT_VOL[2] and switch U18 is used

for EXT_VOL[3]. Identical switch positions are used for common division factors across all three switches. The table below applies to any switch.

Table 2-19 · Switch Settings

Numerical Switch Position	Internal Voltage as Factor of External Voltage Vext
1	Vext * 1
2	Vext * 1/2
3	Vext * 1/4
4	Vext * 1/8

Note: If an external board has voltages greater than 12 V that need to be monitored, use these options to apply the right range of voltage to the AV pad.

Digital Brick

You can connect a digital brick on the board. The following signals are common to all digital bricks.

VIN_D

This is the input power to the digital brick. Use alligator clips to connect the VIN_D pin to the input supply of the digital brick. This pin can provide 9-12 V, depending on the input supply used for the System Management Board.

DIG_BRK_OUT

This is the output voltage of the digital brick. This voltage is monitored by the M1AFS1500-FG484 device using the AV pads.

VSENSE

This pin is an input to the digital brick that senses back the output voltage of the brick (Figure 2-11).

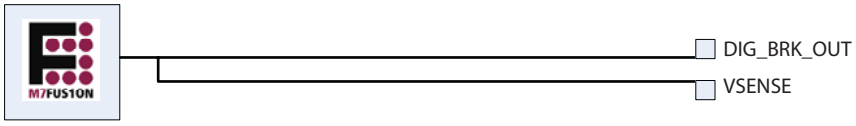

Figure 2-11. VSENSE

TRIM_VOL

This pin is an input to the digital brick controlled by the M1AFS1500-FG484 I/O with a PWM control. The PWM output can be configured using different RC values on the surface mount pads (Figure 2-12).

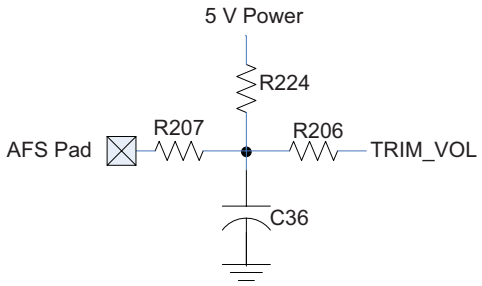

Figure 2-12. TRIM_VOL

This pin can be used to trim the output voltage of the digital brick. The trim voltage varies based on the type of digital brick being used.

Smart Battery

Battery operation of the System Management Board includes battery backup, charging, and discharging routines using the M1AFS1500-FG484 device.

A maximum 7.2 V NiMH 2100 mAh battery can be plugged in the two pin header JP4. The battery operates for approximately 15 to 20 minutes. Make sure the polarity of the battery matches the silkscreen on the header. A temperature diode can be plugged in the two pin header JP5 and can be placed on the battery to monitor temperature, see Table 2-20.

Table 2-20 · Switch Settings

Header	Function
JP4 pin 1	GND
JP4 pin 2	Battery Voltage
JP5 pin 1	TRN – Temperature Diode
1/JP5 pin 2	AT – Temperature Diode

Charging and Discharging Routines

The battery is charged/discharged using the two FET controls (Figure 2-13). When Q3 is turned On and Q2 is turned Off, the constant current source (20 mA) will slowly charge up the 7.2 V battery. When Q3 is turned Off and Q2 is turned On, the battery is placed in discharge mode and will power up the board and start discharging. All voltages and current are monitored by the M1AFS1500-FG484 device. A number of algorithms can be designed in the M1AFS device for implementing the charging and discharging routines of the battery.

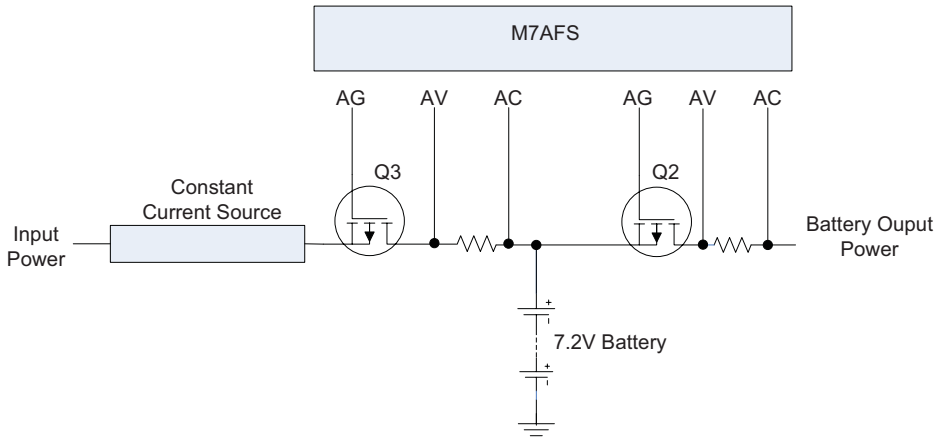

Figure 2-13. Charging and Discharging Routines

For demonstration purposes, you can discharge the battery and place a jumper on JP3. This adds an extra 110 Ω load to the battery output voltage.

Note: The above figure is not a complete representation of the board schematics.

Temperature Monitoring

Connect a temperature diode to header JP5 to monitor battery temperature. Charging/discharging algorithms monitor battery temperature.

Battery Backup

If you need a constant battery backup without any discharging algorithms in the M1AFS1500-FG484 device, place a jumper to JP27. This keeps Q2 On and puts the battery in discharge mode. Both the power brick and the battery are connected, but the power brick powers up the board automatically because the power brick is at a higher voltage than the battery. If the power brick is pulled out in the middle of operation, the battery supply takes over with no interruptions.

Test Points

Table 2-21 and Table 2-22 show various test points provided across the board, and how to access them.

Table 2-21 · Test Points by Numerical Sequence

Test Points	Signal Name
TP1	Digital 3.3 V
TP2	Digital GND
TP3	Digital GND

Table 2-21 · Test Points by Numerical Sequence (Continued)

Test Points	Signal Name
TP4	Digital 3.3 V
TP5	1.5 V EXT
TP6	1.5 V
TP9	Main 3.3 V
TP10	1.5 V
TP11	Analog GND
TP12	VIN_D
TP13	Main GND
TP14	5 V
TP15	VIN
TP16	Analog 3.3 V
TP17	Analog GND
TP18	ATX output 12 V
TP19	ATX output 5 V
TP24	ATX Output 3.3 V

Table 2-22 · Test Points in Signal Name Order

Signal Name	Test Points
1.5 V	TP6
1.5 V	TP10
1.5 V EXT	TP5
5 V	TP14
Analog 3.3 V	TP16
Analog GND	TP17
Analog GND	TP11
ATX output 12 V	TP18
ATX Output 3.3 V	TP24
ATX output 5 V	TP19
Digital 3.3 V	TP1
Digital 3.3 V	TP4
Digital GND	TP2

Table 2-22 · Test Points in Signal Name Order (Continued)

Signal Name	Test Points
Digital GND	TP3
Main 3.3 V	TP9
Main GND	TP13
VIN	TP15
VIN_D	TP12

Prototype Section

A prototype section is provided at the bottom of the board for debug and development purposes (Figure 2-14). The section is 20 holes x 20 holes large with the hole size at 0.100 in x 0.100 in, center to center.

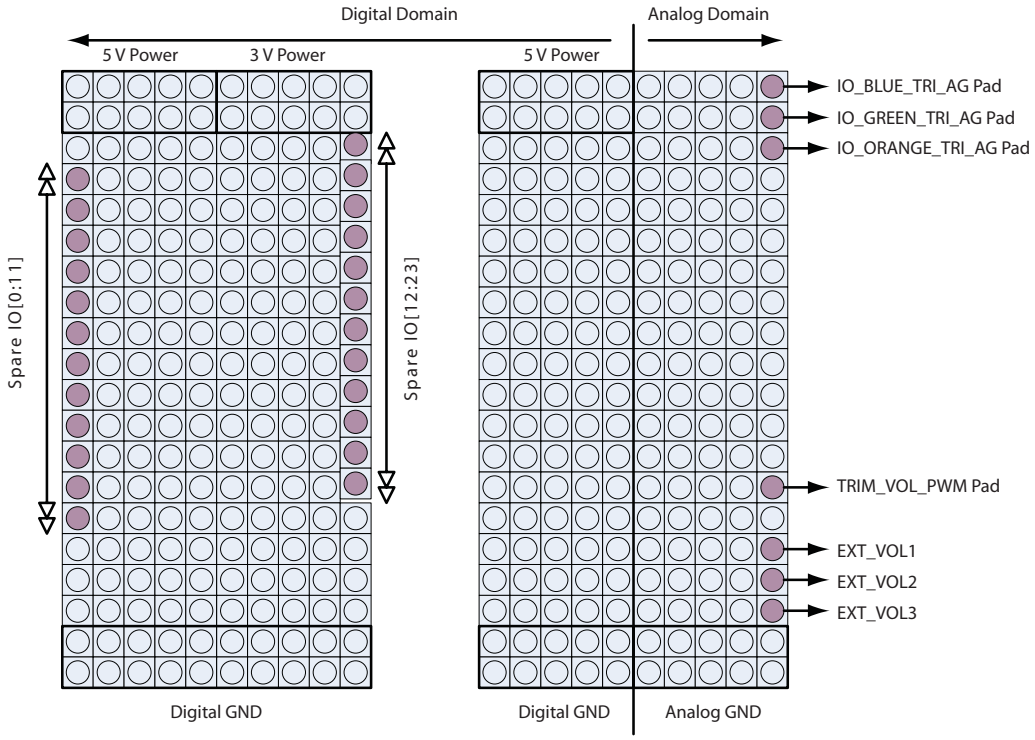

Figure 2-14. Prototype Section

The following signals are provided in the debug area:

- **Power:** 5 V, 3.3 V, 1.5 V and digital and analog GND are provided in this are for easy access. Ensure that the current consumption for any part added to this does not exceed 500 mA.
- **Spare I/Os:** 24 I/Os are provided for debug purposes. These I/Os are connected to the A3P250-FG144 FPGA part.
- **Gate Driver:** Three gate driver pins are provided: IO_BLUE_TRI, IO_GREEN_TRI, IO_ORANGE_TRI. When using these gate drivers, check the jumper settings (Figure 2-23).

Table 2-23 · Jumper Settings

Signal	Jumpers	Tri-LED	Gate Driver
IO_BLUE_TRI	JP29	1-2	Remove Jumper
IO_GREEN_TRI	JP30	1-2	Remove Jumper
IO_ORANGE_TRI	JP31	1-2	Remove Jumper

- **Trim Voltage:** This signal is used in the digital brick application. See "Digital Brick" on page 25. This signal is also routed to the prototype area. This pin can be configured as PWM output.
- **External Voltages:** These are the same input signal provided in "Voltage Monitors" on page 24 and can be used for debug purposes.

3 System Management Software

The System Management software has scrollable, zoomable, and sizeable real-time updated diagrams that enable the simultaneous monitoring of the voltages, currents, and temperatures throughout the board. You can also set the thresholds for these variables and log specific events, when they breach a target level. A full range of current capabilities include the following:

- Event logging with type, time-stamp, and description of each event
- Voltage, current, and temperature monitoring and graphing
- Zoom functions on graph page: zoom in, zoom out, zoom fit, and zoom reset
- Adjustable threshold levels for voltage, current, and temperature
- Internal Flash memory (NVM) address and data screen dump
- Each individual line of raw data displayed in the **Comms** tab
- Display on board components in GUI: LEDs, push buttons, DIP switches, potentiometer, etc.
- Adjustable, on-board LCD text through GUI

The System Management software can also be used to set the RTC by matching it with the host PC. Logging events are controlled and monitored through the interface.

The software initially communicates via RS-232 serial communications. Baud rate is selectable from the **Comms** tab. The COM port is selectable, but Actel recommends you use COM port 1.

There is limited self-testability in the absence of an actual board. You can use one copy of the software to generate serial communications traffic and to log that traffic with another running copy.

The user interface is organized in the following tabs (Figure 3-1 on page 31):

- **Board Status:** Covering the basic I/O tests and RTC, including real-time voltage, current, and temperature monitoring, and internal Flash memory reading.
- **Graphs:** A set number of labelled graphs to the same time-base, monitoring of board voltages and currents, including readings for the heater, PCI, finger pad, regulator, board, and potentiometer.
- **Event Log:** Event logging is displayed here. By uploading the stored event log from the board, you can view the events and their individual warning level, type of event, time of occurrence, and a short description.
- **Comms:** This tab enables the user to change the baud rate and COM port (COM port 1 is recommended). In this tab, you can enable a System Management software test to start/stop reception and transmission of bit sequences for observation. A raw data window displays the sampled data. This tab contains a continuously updated display of data sent and received.
- **Thresholds:** The board thresholds can be set for the board supply, PSU supply, temperature, and potentiometer.

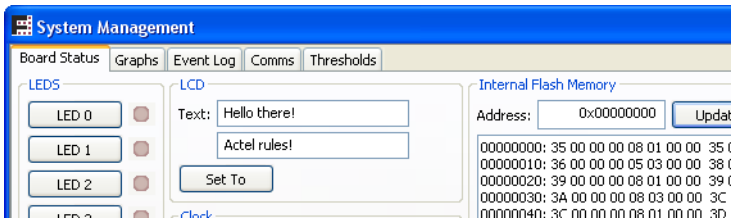

Figure 3-1. Tabs

Board Status

The **Board Status** tab is split into ten panels that control the behavior of the board (Figure 3-2).

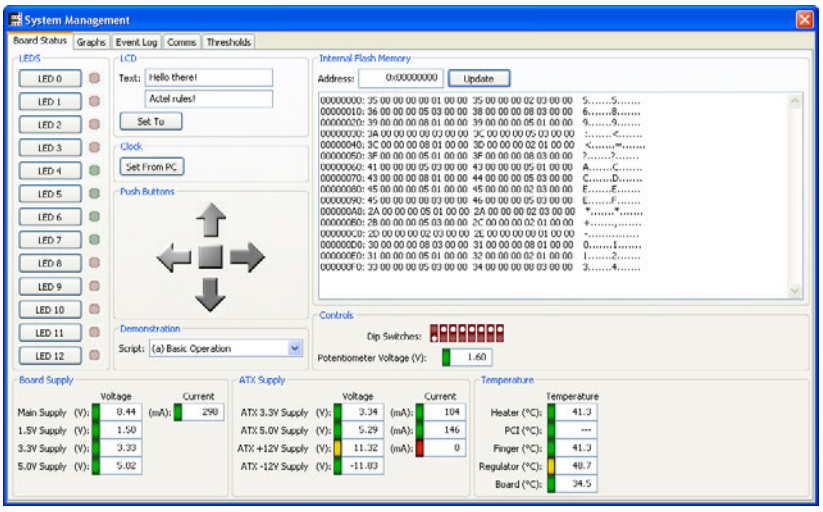

Figure 3-2. Board Status Tab

LEDs

To turn on and off each LED on the board, click the corresponding LED button in the software.

LCD

To output two lines of text to the LCD screen, type the text that you want to display and click the **Set to** button. The board firmware also uses the LCD and displays the "Clock".

Clock

To synchronize the real-time on-board clock with the computer's local time, click the **Set From PC** button.

Push Buttons

To test the correct synchronization between the push buttons on the board and the software, push the button on the board and check that the corresponding button in the software lights up.

Demonstration

In this version only basic operations are demonstrated. However, in future versions you will be able to select from a range of pre-selected demonstration scripts.

Internal Flash Memory

Enter the starting address (in hexadecimal) and click the **Update** button to dump all current data and the addresses stored in the internal Fusion nonvolatile Flash memory into this window for debug purposes. Commencing at the starting address, the data lists each byte chunk on each line, 16 in total, ending in their corresponding ASCII code. 16 lines are printed, representing 256 bytes of nonvolatile memory.

Controls

To display the state (open or closed) of the on-board DIP switches, open and close the DIP switches on the board. The results are displayed in the software.

To display the potential difference across the potentiometer, adjust the rotating switches on the board. The results are displayed in the software.

Board Supply

The board supply displays a real-time reading of the voltage and current ratings for the main supply. It also displays the real-time voltages for the 1.5 V, 3.3 V, and 5.0 V supplies respectively. See "Voltage, Current and Temperature Status Indicators" for more information on the status indicators.

PSU Supply (ATX Supply)

The PSU supply displays the real-time voltage and current ratings for the attached ATX (3.3 V, 5.0 V, and +12 V) supply, and the real-time voltage for the -12 V supply.

Temperature

The temperature section displays the real-time temperature (°C) on the board from the sensors loaded at the heater, the PCI, the finger pad, the regulator, and the board itself.

Voltage, Current and Temperature Status Indicators

The following explains the voltage, current, and temperature status indicators found in the Board Status tab next to each reading.

Red - Voltage/current/temperature is above the maximum or below the minimum.

Green - Voltage/current/temperature is within set range.

Yellow - Voltage/current/temperature between maximum and local maximum or between minimum and local minimum.

Graphs

The **Graphs** tab generates the graphs for the various voltages, currents, and temperatures involved on the board (Figure 3-3).

Figure 3-3. Graphs Tab

The **Zoom** box allows you to zoom in, zoom out, zoom fit, or zoom reset the graphs.

To turn the graph background from the default black to white, check the appropriate box in the **Background** box.

The scale in percentages to the left of each graph corresponds to the absolute measured range for any of the displayed graphs. The percentage of 0% represents Range-Lo and 100% represents Range-Hi. Refer to "Thresholds" on page 36 for more information on Range-Lo and Range-Hi. Refer to "Setting the Thresholds Graphically" on page 39 for more information about setting the thresholds on the **Graphs** tab.

Note: Figure 3-3 contains spikes, which were caused by global reset and will occur every time the reset button is pressed.

Event Log

The **Events Log** tab displays the type of triggered event followed by a timestamp, source, and historic data. The event log is stored in the on-chip NVM (nonvolatile memory). Events result from thresholds set on each monitored source

(see "Thresholds" on page 36). The timestamp is based on the time set on the board at the instant the event occurred. The events show all crossing of thresholds (including returning to normal). See "Event Log Tab" on page 35.

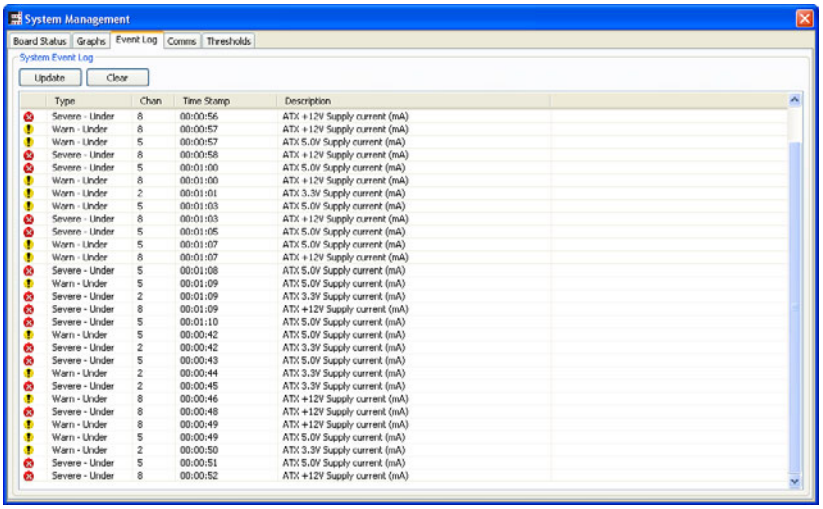

Figure 3-4. Event Log Tab

To upload the stored event log from the target board, click the **Update** button. Refer to "To set up sample/threshold data logging:" on page 46 for more information about setting up event logging.

Comms

The **Comms** tab allows you to change the baud rate, the COM port in use, and start or stop reception and transmission of bit sequences as part of the System Management software.

The following options are available from the **Comms** tab:

- Start Rx: Starts reception of data
- Start Tx: Starts transmission of data
- Stop Rx: Stops reception of data
- Stop Tx: Stops transmission of data
- Bytes Tx: Bytes transmitted
- Bytes Rx: Bytes received
- Enable GUI Test: Check this box for debugging purposes if problems arise with the demonstration

The raw data window displays raw data based on the transmitted bit sequences (Figure 3-5).

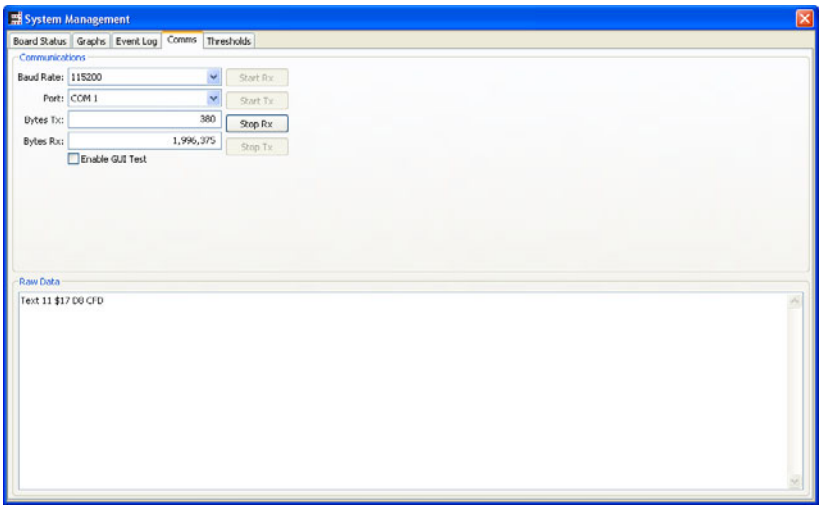

Figure 3-5. Comms Tab

Thresholds

The **Thresholds** tab allows you to adjust thresholds for which events are logged (Figure 3-6).

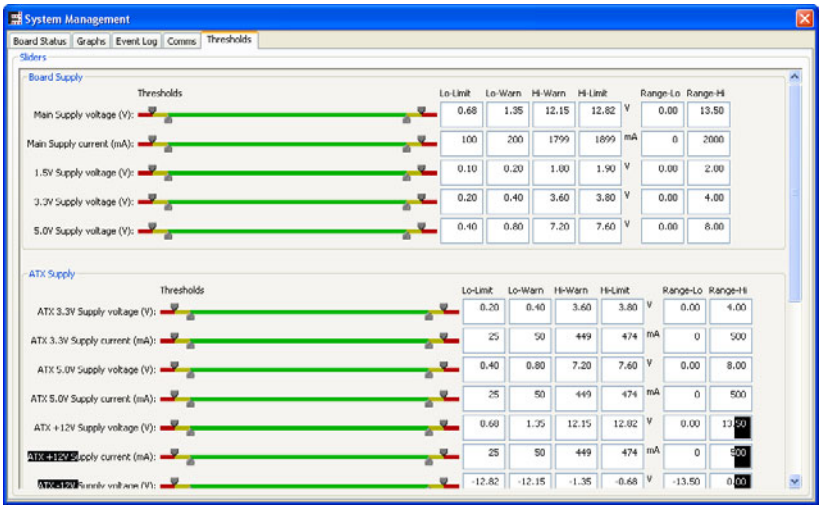

Figure 3-6. Threshold Tab

The **Thresholds** tab is divided into four sections:

- Board Supply
- PSU Supply
- Temperature
- Potentiometer

You can change the thresholds using the threshold sliders:

- Lo-Limit is the absolute minimum threshold and produces a RED if breached.

- Lo-Warn is a local minimum, which produces a YELLOW light if breached.
- Hi-Warn is a local maximum, which if passed also produces a YELLOW light.
- Hi-Limit is the absolute maximum, which produces a RED light if breached.

When the thresholds are set between Lo-Warn and Hi-Warn, a green light indicates that the board is operating at optimum levels between these two points.

The shaded boxes on the right display the exact threshold values for the Lo-Limit, Lo-Warn, Hi-Warn and Hi-Limit.

The Range-Lo and Range-Hi panels indicate the extreme far right and far left of the colored lines. None of these shaded boxes can be changed manually and can only be set by the slider markers.

See "Setting Thresholds" on page 39 for more information about setting threshold limits in the **Threshold** tab and in the **Graphs** tab.

4

Setting Thresholds

This section details how to set the thresholds used throughout the demonstration. The board thresholds can be set in two different ways in the **Thresholds** tab: you can set and see the points and triggers graphically or you can use the high-water/low-water slider marker, which will allow tracking of extreme values.

Setting the Thresholds Graphically

1. Click the **Graphs** tab.
2. Slide the marker on the right hand side of the graph to set the maximum/minimum and local maximum/minimum levels. To change these, simply drag the arrow to the desired position.
3. Click **Zoom Fit** to fit the graph in the window. The red/yellow line across the graph represents the level marker (red represents the absolute maximum/minimum or Hi-Limit/Lo-Limit; yellow represents the local maximum/minimum or Hi-Warn, Lo-Warn).

Note: The maximum/minimum and local maximum/minimum lines are better viewed in a white background.

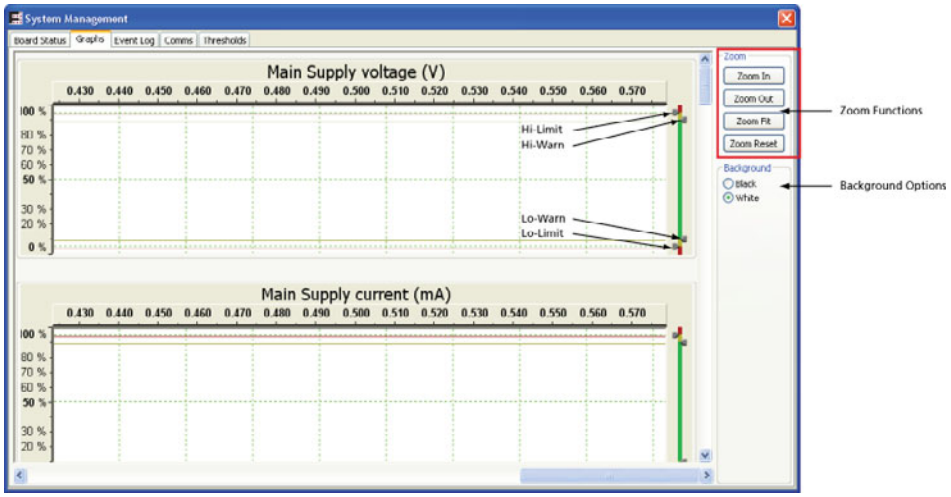

Figure 4-1. Setting Thresholds Graphically

Setting the Thresholds with the Slider Marker

1. Click the **Thresholds** tab.
2. Select the part for which you wish to alter the threshold levels.
3. Set the Lo-Warn and Hi-Warn levels as desired.
4. Set the Lo-Limit and Hi-Limit levels as desired.

Figure 4-2. Setting Thresholds by Slide Marker

Voltage, Current, and Temperature Status Indicators

The following explains the voltage, current, and temperature status indicators found in the Board Status tab next to each reading.

Red - Voltage, current, or temperature is above the maximum or below the minimum.

Green - Voltage, current, or temperature is within set range.

Yellow - Voltage, current, or temperature is between maximum and local maximum or between minimum and local minimum.

5

Demonstration Scripts

The scripts in this chapter demonstrate some of the basic functions of the board and the System Management software, including the following:

- General setup
- Basic controls
- Voltage monitoring
- Current monitoring
- Temperature monitoring
- RTC control
- Logging events

General Setup

This section describes how to set up the System Management board and software using an external power supply brick.

1. Connect the ATX power supply to the white connector labeled "ATX input power supply" (Figure 5-1, Figure 5-2 on page 41, and Figure 5-3 on page 42).

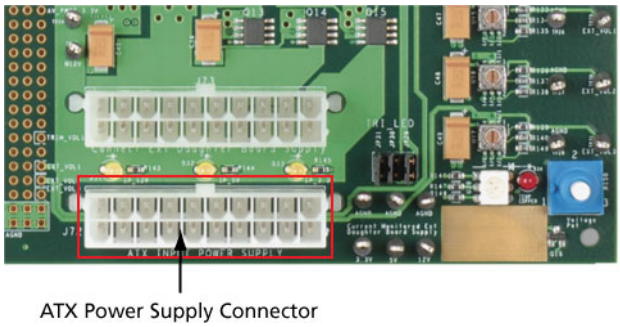

Figure 5-1. ATX Power Supply Connector (female)

Figure 5-2. Standard ATX Power Supply Connector (male)

Figure 5-3. ATX Power Supply

2. Using the RS-232 cable supplied, connect one end to the on-board RS-232 port and the other end to serial COM Port 1 (recommended) on the host PC.
3. Power-on the board controller.

   Note: The power connector can only be inserted in one way, with the tag facing towards the LCD screen.
4. Press the global reset (GL_RESET) button on-board before every demonstration (Figure 5-4).

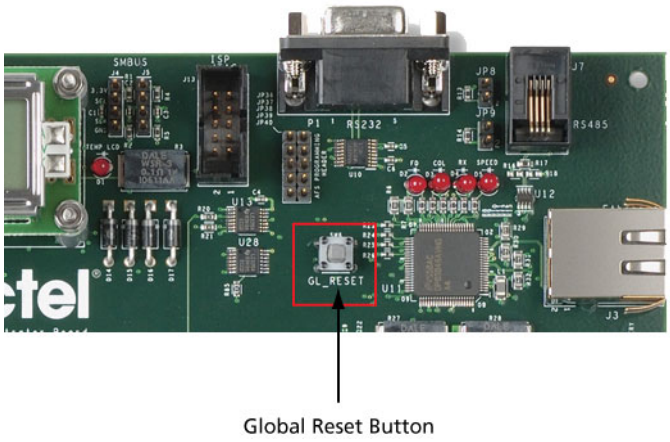

Figure 5-4. Global Reset Button

5. Start the System Management software.
6. Ensure that the System Management software is communicating with the board by pressing the buttons on the board and awaiting its graphical response in the **Board Status** tab. If you have any problems, check that the cables are correctly and fully inserted and repeat steps 1 to 6.
7. Wait for voltages and currents in the **Board Status** tab to reach a steady state (this may take several minutes).

Basic Controls

This section demonstrates simple on-board functions.

1. Set up the board, as indicated in "General Setup" on page 41.
2. Start the System Management software, and click the **Board Status** tab.
3. Click each LED, one through 12. This individually lights up the LEDs on the board. LEDs 0 to 7 are shown in Figure 5-5. LEDs 8 to 12 are scattered around the board.

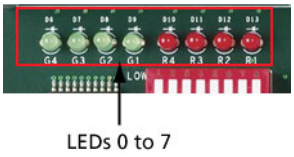

Figure 5-5. LEDs 0-7

4. Press the push buttons on the top left of the board. The result appears in the **Push Buttons** panel in the **Board Status** tab, (Figure 5-6).

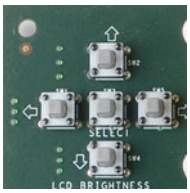

Figure 5-6. Push Buttons

5. Open and close the DIP switches. The changes appear in the **Controls** panel in the **Board Status** tab (Figure 5-7).

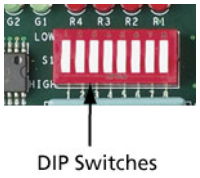

Figure 5-7. DIP Switches

6. Enter text into the **LCD Text** box in the **Board Status** tab. Now click the **Set to** button to update the on-board LCD screen with the entered information (Figure 5-8).

   Note: The LCD screen can only display 16 characters per line and errors may appear if this is exceeded.

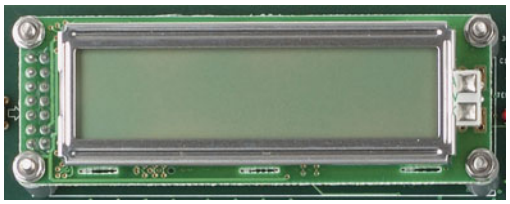

Figure 5-8. LCD Screen

Note: Refer to "RTC Control" on page 45 for more information about the real-time clock.

Voltage Monitoring

This section demonstrates how to use the System Management software to monitor the board's voltages with the external power supply.

1. Observe voltages in real-time (including potentiometer) in the **Board Status** tab (Figure 5-9).

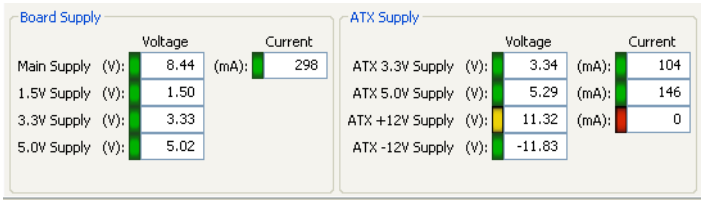

Figure 5-9. Board Voltage Monitoring

2. View the graphs in the **Graphs** tab. If necessary, scroll down to view the desired graph. Note that the graph may change slowly upon connection to power.
3. Observe the reading for **Main Supply** in the **Board Supply** panel (Figure 5-9). Compare this reading to the reading for the main supply voltage in the **Graphs** tab (Figure 5-10).

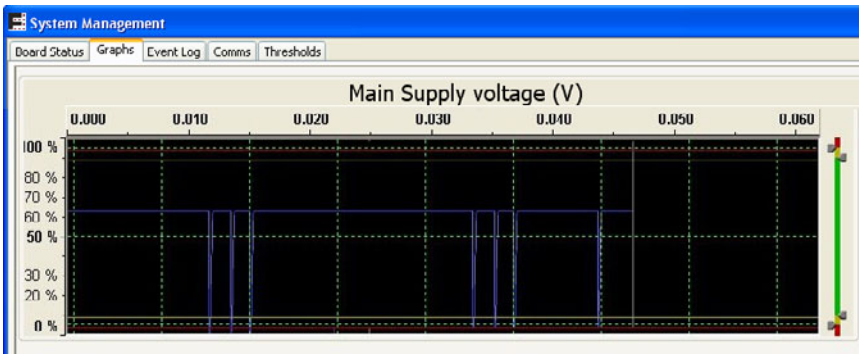

Figure 5-10. Board Voltage Monitoring: Main Supply Graph

4. Observe the reading for 3.3 V, 5.0 V, and +12 V in the **PSU Supply** panel (Figure 5-9). Compare this reading to the reading for each voltage level in the **Graphs** tab. You may have to scroll down for each voltage level using the scroll bar on the right hand side.

Current Monitoring

This example demonstrates the real-time current reading for advanced technology extended (ATX) loads (+12 V, +5 V, and +3.3 V) under the **Board Status** tab. ATX power supply refers to the power supply used throughout.

1. Observe the current of the main supply in real-time in the **Board Status** tab.
2. Compare the readings in the **Board Supply** panel in the **Board Status** tab with their corresponding graph in the **Graphs** tab.

3. Remove the load resistors (pull on the black plastic tab, shown in Figure 5-11). Observe the currents (3.3 V, 5.0 V, and +12 V) in the **PSU Supply** panel on the **Board Status** tab.

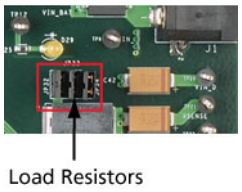

Figure 5-11. Load Resistors

4. Observe the graph as the load is removed. Note the current goes to 0 mA.
5. Compare the readings in the **Board Supply** and **PSU Supply** panels to their corresponding graphs in the **Graphs** tab.

Temperature Monitoring

Observe the board temperature in real-time in the **Board Status** tab in the System Management software (all except battery temperature).

To observe the copper pad (finger pad) temperature:

1. Hold your finger on the copper pad (Figure 5-12).

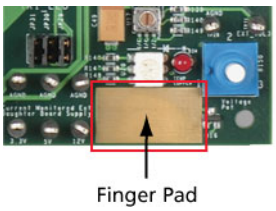

Figure 5-12. Finger Pad

2. Observe the finger pad temperature in real-time in the **Board Status** tab. Also observe the graph in the **Graphs** tab. You may have to scroll down to view the finger graph.

   Note: The finger pad may take several minutes to heat up due to body heat, but it should reach around 38.5°C. When you remove your finger, the pad will take much longer to cool down due to lack of direct cooling, but will reach room temperature.

RTC Control

The real-time clock (RTC) is the clock used on the board, which keeps track of the current time. It is possible to synchronize the on-board clock with the PC's clock through the following setup.

To set up the RTC:

1. To set the RTC from the PC, click the **Set from PC** button in the **Board Status** tab.
2. You can view the board's time stored in the real-time clock on the **System Event Log** in the **Event Log** tab.

Logging Events

The **System Event Log** available on the **Event Log** tab can be used to record the incoming captured data from the board.

To upload a stored event log from the target board, click the **Update** button. This takes all the current board information from the internal Fusion Flash nonvolatile memory and displays it on-screen with specific details about type, channel, timestamp, and description. Description may include source, time, and historic data.

To set up sample/threshold data logging:

1. Click the **Thresholds** tab and set the threshold for the potentiometer. Ensure the potentiometer is in range. Refer to "Setting Thresholds" on page 39 for more information about setting thresholds.
2. Move the potentiometer by turning the handle.
3. Click the **Board Status** tab and observe the potentiometer field as you move the potentiometer. The indicator changes from yellow to green, then to red.
4. Click the **Event Log** tab and click the **Update** button.

	Warn - Over	4	21:18:00	PSU 5.0V Supply V
	OK	24	17:40:36	Channel 24
	Warn - Over	16	12:26:04	-12V Supply V
	Warn - Under	18	19:01:44	Channel 18
	Warn - Under	8	05:42:24	+12V Supply mA
	Warn - Over	16	07:24:32	-12V Supply V
	Warn - Under	18	23:23:52	Channel 18
	OK	28	00:49:32	Main Supply V
	Warn - Under	18	00:11:24	Channel 18
	OK	24	10:41:40	Channel 24

Figure 5-13. Event Log Example

5. View the log and make note of the changes in the potentiometer field. Table 1 specifies the warning levels.

Table 1. Warning Legend

Warning		Description
	Severe – Under	Lo-Limit breached
	Warn – Under	Lo-Warn breached
	Ok	Within acceptable range
	Warn – Over	Hi-Warn breached
	Severe – Over	Hi-Limit breached

6. Click the **Graphs** tab and observe the graph for the potentiometer.

The example shown in Figure 5-13 shows that at time 23:23:52, channel 18 sent a warning event indicating that the voltage/current/temperature level dropped below the stated local minimum (Lo-Warn).

A

M1AFS1500-FG484 Pin List

This pin list is also applicable to the older SYSMGMT-DEV-KIT fitted with an M7AFS600-FG484 device. Pin usage is the same on these kits.

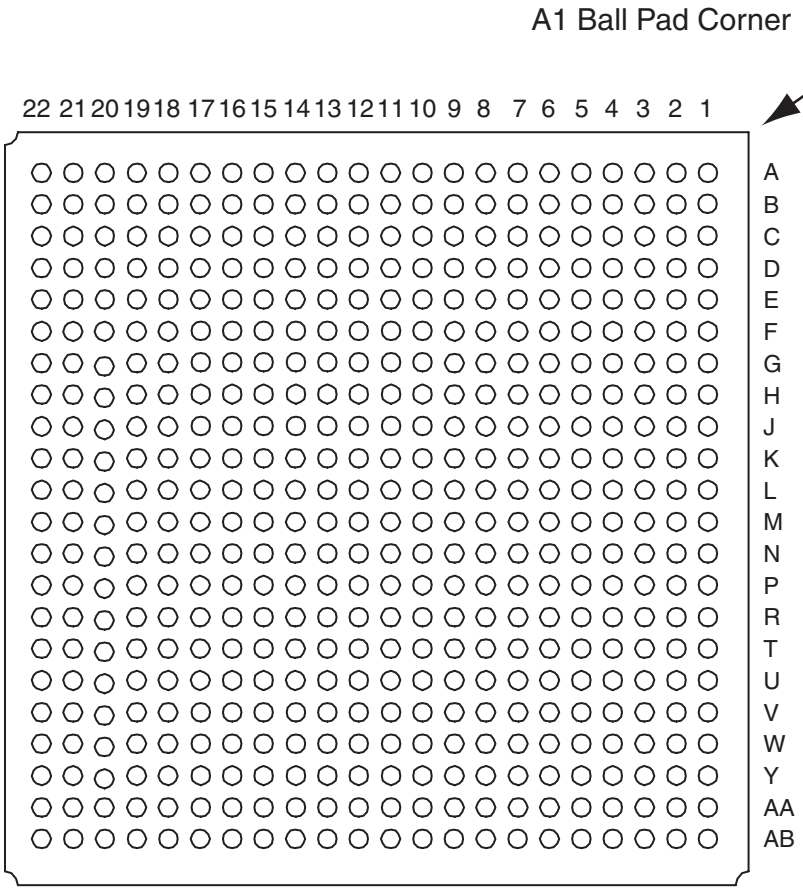

Figure A-1. 484-Pin FBGA (Bottom View)

Note: Full pin list data for the 484-Pin FBGA package is available in the Fusion datasheet, at http://www.actel.com/documents/Fusion_DS.pdf

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

Pin Name	Pin Description
A3	CLK_50MHZ
A4	FPGA-ENA-RXD[2]
A5	FLASH_WRITEN/SSRAM_BWRITTEN Shared
A6	MEM_DATA[16]
A7	MEM_DATA[15]
A8	PCIREQN[2]

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

A9	SSRAM_CSN
A10	FLASH_READN/SSRAM_READN Shared
A11	MEM_ADDR[8]
A12	IO_AFS_TX
A13	SDA1
A14	FPGA-ENA-TXD[2]
A15	MEM_DATA[12]
A16	FPGA_ENA_MDC
A17	FPGA_ENA_RXCLK
A18	RS485_RO
A19	RVI-ME-RCK
A20	RVI-ME-DBGRQ_
B3	FPGA_ENA_RXER
B5	MEM_ADDR[10]
B6	MEM_ADDR[19]
B8	MEM_ADDR[9]
B9	SSRAM_B2N
B11	MEM_DATA[3]
B12	FPGA_ENA_RXD[1]
B14	AFS_PS_ON
B17	GL_RESET
C1	SSRAM_B0N
C3	RVI-ME-Vtref
C4	RVI-ME-DBGACK
C6	MEM_DATA[31]
C7	MEM_DATA[30]
C9	FLASH_RB
C10	FLASH_RPN
C13	FPGA_ENA_TXD[0]
C14	FPGA_ENA_TXD[1]
C16	SCL1
C17	RVI_ME_TMS
C20	RS232_RX0

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

C22	FPGA_ENA_RXD[3]
D1	SSRAM_B1N
D3	MEM_DATA[5]
D4	SSRAM_CLK
D5	RVI-ME-nSRST
D6	RVI-ME-nTRST
D7	SSRAM_B3N
D8	MEM_DATA[6]
D9	MEM_DATA[4]
D10	MEM_ADDR[1]
D11	RS484_DI
D12	FPGA_ENA_CRS
D14	FPGA_ENA_MDIO
D15	FLASH_CSN
D16	FPGA_ENA_TXCLK
D17	FPGA_ENA_TXEN
D20	FPGA_ENA_RXD[0]
D22	AFS_MB_PS_ON
E1	MEM_DATA[8]
E2	MEM_DATA[9]
E4	RVI-ME-TCK
E5	RVI-ME-TDI
E11	MEM_ADDR[15]
E12	AFS_TDO
E19	SDA2/AFS_TMS
E21	AD[14]
E22	AD[1]
F1	MEM_DATA[10]
F2	MEM_DATA[7]
F4	MEM_ADDR[6]
F9	MEM_ADDR[5]
F10	MEM_ADDR[4]
F13	MEM_ADDR[3]

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

F14	MEM_ADDR[16]
F19	RS485_REB/AFS_TRST
F20	AD[3]
F21	AD[11]
F22	AD[10]
G1	MEM_DATA[21]
G3	MEM_DATA[11]
G4	MEM_DATA[22]
G9	MEM_ADDR[18]
G10	MEM_ADDR[11]
G11	PCIREQN[1]
G19	AD[2]
G20	AD[6]
G22	AD[7]
H1	MEM_DATA[19]
H2	IO_FET_FAN
H4	MEM_DATA[23]
H5	MEM_ADDR[12]
H18	MEM_DATA[2]
H19	AD[4]
H21	AD[26]
H22	AD[9]
J2	MEM_DATA[25]
J3	MEM_DATA[26]
J4	SCL2/AFS_TCK
J16	MEM_DATA[0]
J18	IO_AFS_RX
J19	AD[15]
J20	AD[23]
J22	AD[16]
K1	MEM_DATA[29]
K3	MEM_DATA[13]
K4	PCISMBDAT

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

K16	PCIPME[2]
K20	AD[22]
K22	AD[21]
L1	MEM_DATA[14]
L5	INTBN
L7	PCISMBCLK
L16	MEM_ADDR[13]
L18	MEM_ADDR[17]
L19	AD[17]
L21	AD[20]
L22	AD[5]
M5	MEM_ADDR[0]
M7	MEM_DATA[20]
M16	MEM_ADDR[14]
M18	MEM_ADDR[2]
M19	IN_POWER_OK
M21	AD[0]
M22	AD[19]
N3	PCICLK
N16	CBEN[0]
N19	AD[28]
N20	AD[12]
N22	AD[8]
P1	PCIGNTN[2]
P2	INTAN
P3	FRAMEN
P4	MEM_DATA[28]
P5	MEM_DATA[24]
P16	MEM_DATA[1]
P18	FPGA_ENA_COL
P19	AD[27]
P20	AD[29]
P21	AD[30]

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

P22	AD[25]
R1	MEM_DATA[17]
R2	MEM_DATA[18]
R4	MEM_DATA[27]
R5	IRDYN
R18	TRDYN
R19	MEM_ADDR[7]
R21	AD[24]
R22	AD[18]
T3	SERRN
T4	M66EN
T10	BAT_DISCHARGE_MON_AV
T12	AV_PSU_N12V
T13	AV_POT
T19	RVI-ME-TDO
T20	RS232_TX0
T22	AD[13]
U1	PERRN
U2	DEVSELN
U3	PCIPME[1]
U4	STOPN
U10	BAT_DISCHARGEMON_AC
U13	BAT_MODE
U19	SSRAM_PWRDWN
U20	RS485_DE/AFS_TDI
U22	MB_POWER_OK
V1	INTDN
V2	CLK_VAR
V4	INTCN
V5	PCIGNTN[1]
V10	BAT_CHARGE_MODE
V11	AT4_COPPER
V12	ATRN_COPPER

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

V13	EXT_VOL2
W4	CBEN[2]
W5	AD[31]
W6	AV_PWR2_3.3V
W8	AV_PWR2_5V
W9	AV_PWR2_12V
W11	BAT_CHARGE_MON_AV
W12	AV_PSU_12V
W14	AV_PSU_5V
W15	AV_PSU_3.3V
W17	VIN_BAT_AV
Y1	CBEN[3]
Y2	PCIRSTN
Y3	CBEN[1]
Y4	PAR
Y6	AC_PWR2_3.3V
Y8	AC_PWR2_5V
Y9	AC_PWR2_12V
Y11	BAT_CHARGEMON_AC
Y12	SKP_5V
Y14	SKP_3.3V
Y15	1.5V
Y17	VIN_BAT_AC
AA6	AG_PSU_3.3V
AA8	AG_PSU_5V
AA9	AG_PSU_12V
AA11	AG_PSU_N12V
AA12	IO_BLEU_TRI
AA14	IO_GREEN_TRI
AA15	IO_ORANGE_TRI
AA17	AG_FET_HEATER
AA18	VAREF
AB6	AT0_REG

Table A-1 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board

AB7	ATRN_REG
AB8	EXT_VOL1
AB9	BAT_AT
AB10	BAT_ATRN/ATRN_PCI Shared
AB11	AT3_PCI
AB12	AT6_LCD
AB14	EXT_VOL3
AB15	AT8_Heater
AB16	ATRN_HEATER
AB17	DIG_BRK_OUT1

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order

ARM Debugger	Pin Name
RVI-ME-DBGACK	C4
RVI-ME-DBGRQ_	A20
RVI-ME-nSRST	D5
RVI-ME-nTRST	D6
RVI-ME-RCK	A19
RVI-ME-TCK	E4
RVI-ME-TDI	E5
RVI-ME-TDO	T19
RVI-ME-TMS	C17
RVI-ME-Vtref	C3
ATX	**Pin Name**
AFS_MB_PS_ON	D22
AFS_PS_ON	B14
IN_POWER_OK	M19
IO_FET_FAN	H2
MB_POWER_OK	U22
CoreUART(A3P-M1AFS)	**Pin Name**
IO_AFS_RX	J18
IO_AFS_TX	A12

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order (Continued)

Ethernet	Pin Name
FPGA_ENA_MDC	A16
FPGA_ENA_MDIO	D14
FPGA_ENA_COL	P18
FPGA_ENA_RXCLK	A17
FPGA_ENA_RXDV	B18
FPGA_ENA_CRS	D12
FPGA_ENA_RXER	B3
FPGA_ENA_RXD[0]	D20
FPGA_ENA_RXD[1]	B12
FPGA_ENA_RXD[2]	A4
FPGA_ENA_RXD[3]	C22
FPGA_ENA_TXCLK	D16
FPGA_ENA_TXEN	D17
FPGA_ENA_TXD[0]	C13
FPGA_ENA_TXD[1]	C14
FPGA_ENA_TXD[2]	A14
FPGA_ENA_TXD[3]	B15
Gate Drivers	**Pin Name**
AG_FET_HEATER	AA17
AG_PSU_12V	AA9
AG_PSU_3.3V	AA6
AG_PSU_5V	AA8
AG_PSU_N12V	AA11
BAT_CHARGE_MODE	V10
BAT_MODE	U13
IO_BLEU_TRI	AA12
IO_GREEN_TRI	AA14
IO_ORANGE_TRI	AA15
M1AFS Pin Description	**Pin Name**
CLK_50MHZ	A3
VAREF	AA18

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order (Continued)

GL_RESET	B17
PCI	**Pin Name**
AD[0]	M21
AD[1]	E22
AD[2]	G19
AD[3]	F20
AD[4]	H19
AD[5]	L22
AD[6]	G20
AD[7]	G22
AD[8]	N22
AD[9]	H22
AD[10]	F22
AD[11]	F21
AD[12]	N20
AD[13]	T22
AD[14]	E21
AD[15]	J19
AD[16]	J22
AD[17]	L19
AD[18]	R22
AD[19]	M22
AD[20]	L21
AD[21]	K22
AD[22]	K20
AD[23]	J20
AD[24]	R21
AD[25]	P22
AD[26]	H21
AD[27]	P19
AD[28]	N19
AD[29]	P20

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order (Continued)

AD[30]	P21
AD[31]	W5
CBEN[0]	N16
CBEN[1]	Y3
CBEN[2]	W4
CBEN[3]	Y1
DEVSELN	U2
FRAMEN	P3
INTAN	P2
INTBN	L5
INTCN	V4
INTDN	V1
IRDYN	R5
M66EN	T4
PAR	Y4
PCICLK	N3
PCIGNTN[1]	V5
PCIGNTN[2]	P1
PCIREQN[1]	G11
PCIREQN[2]	A8
PCIRSTN	Y2
PERRN	U1
SERRN	T3
STOPN	U4
TRDYN	R18
CLK_VAR	V2
PCIPME[1]	U3
PCIPME[2]	K16
PCISMBCLK	L7
PCISMBDAT	K4
RS232	**Pin Name**
RS232_RX0	C20

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order (Continued)

RS232_TX0	T20
RS485	**Pin Name**
RS484_DI	D11
RS485_DE/AFS_TDI	U20
RS485_REB/AFS_TRST	F19
RS485_RO	A18
SMBus	**Pin Name**
AFS_TDO	E12
SCL1	C16
SCL2/AFS_TCK	J4
SDA1	A13
SDA2/AFS_TMS	E19
SRAM/FLASH	**Pin Name**
FLASH_CSN	D15
FLASH_RB	C9
FLASH_READN/SSRAM_READN Shared	A10
FLASH_RPN	C10
FLASH_WRITEN/SSRAM_BWRITTEN Shared	A5
MEM_ADDR[0]	M5
MEM_ADDR[1]	D10
MEM_ADDR[2]	M18
MEM_ADDR[3]	F13
MEM_ADDR[4]	F10
MEM_ADDR[5]	F9
MEM_ADDR[6]	F4
MEM_ADDR[7]	R19
MEM_ADDR[8]	A11
MEM_ADDR[9]	B8
MEM_ADDR[10]	B5
MEM_ADDR[11]	G10
MEM_ADDR[12]	H5
MEM_ADDR[13]	L16

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order (Continued)

MEM_ADDR[14]	M16
MEM_ADDR[15]	E11
MEM_ADDR[16]	F14
MEM_ADDR[17]	L18
MEM_ADDR[18]	G9
MEM_ADDR[19]	B6
MEM_DATA[0]	J16
MEM_DATA[1]	P16
MEM_DATA[2]	H18
MEM_DATA[3]	B11
MEM_DATA[4]	D9
MEM_DATA[5]	D3
MEM_DATA[6]	D8
MEM_DATA[7]	F2
MEM_DATA[8]	E1
MEM_DATA[9]	E2
MEM_DATA[10]	F1
MEM_DATA[11]	G3
MEM_DATA[12]	A15
MEM_DATA[13]	K3
MEM_DATA[14]	L1
MEM_DATA[15]	A7
MEM_DATA[16]	A6
MEM_DATA[17]	R1
MEM_DATA[18]	R2
MEM_DATA[19]	H1
MEM_DATA[20]	M7
MEM_DATA[21]	G1
MEM_DATA[22]	G4
MEM_DATA[23]	H4
MEM_DATA[24]	P5
MEM_DATA[25]	J2

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order (Continued)

MEM_DATA[26]	J3
MEM_DATA[27]	R4
MEM_DATA[28]	P4
MEM_DATA[29]	K1
MEM_DATA[30]	C7
MEM_DATA[31]	C6
SSRAM_B0N	C1
SSRAM_B1N	D1
SSRAM_B2N	B9
SSRAM_B3N	D7
SSRAM_CLK	D4
SSRAM_CSN	A9
SSRAM_PWRDWN	U19
Temperature Monitors	**Pin Name**
AT0_REG	AB6
AT3_PCI	AB11
AT4_COPPER	V11
AT6_LCD	AB12
AT8_Heater	AB15
ATRN_COPPER	V12
ATRN_HEATER	AB16
ATRN_REG	AB7
BAT_AT	AB9
BAT_ATRN/ATRN_PCI Shared	AB10
Voltage/Current Monitors	**Pin Name**
1.5V	Y15
AC_PWR2_12V	Y9
AC_PWR2_3.3V	Y6
AC_PWR2_5V	Y8
AV_POT	T13
AV_PSU_12V	W12
AV_PSU_3.3V	W15

Table A-2 · Subset of M1AFS1500-FG484 Pin List Usage Specific to System Management Board by Function Order (Continued)

AV_PSU_5V	W14
AV_PSU_N12V	T12
AV_PWR2_12V	W9
AV_PWR2_3.3V	W6
AV_PWR2_5V	W8
BAT_CHARGE_MON_AV	W11
BAT_CHARGEMON_AC	Y11
BAT_DISCHARGE_MON_AV	T10
BAT_DISCHARGEMON_AC	U10
DIG_BRK_OUT1	AB17
EXT_VOL1	AB8
EXT_VOL2	V13
EXT_VOL3	AB14
SKP_3.3V	Y14
SKP_5V	Y12
VIN_BAT_AC	Y17
VIN_BAT_AV	W17

B

A3P250-FG144 Pin List

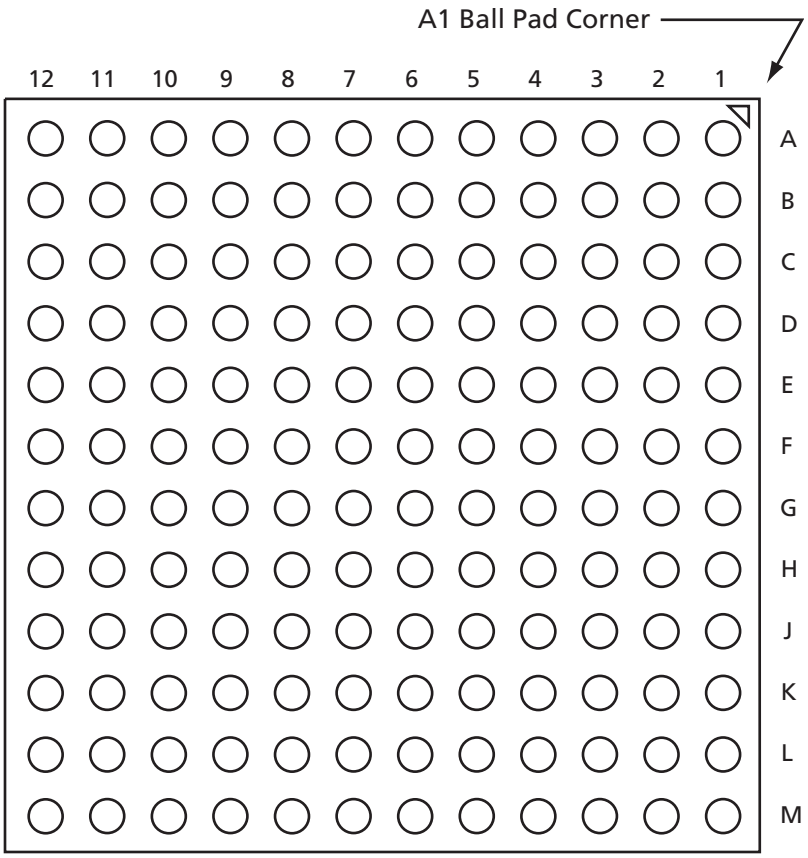

Figure B-1. 144-Pin FBGA (Bottom View)

Note: Full pin list data for the 144-Pin FBGA package is available in the ProASIC3 datasheet, at http://www.actel.com/documents/PA3_DS.pdf

Table B-1 · Subset of A3P250-FG144 Pin List Usage Specific to System Management Board

Pin Name	Pin Description
A3	dip[7]
A4	dip[6]
A5	dip[5]
A7	dip[4]
A9	dip[3]
A10	dip[2]
A11	dip[1]

Table B-1 · Subset of A3P250-FG144 Pin List Usage Specific to System Management Board

B5	rx
B6	tx
B7	lcd_blk
B9	led[7]-green
B10	dip[0]
B10	led[6]-green
C1	led[5]-green
C2	led[4]-green
C3	led[3]-red
C5	led[2]-red
C6	led[1]-red
C7	led[0]-red
C8	key[0]-select
C9	key[3]-right
C10	key[4]-left
C11	key[1]-down
C12	key[2]-up
D1	debug[10]
D2	debug[9]
D3	debug[8]
D4	debug[7]
D5	debug[6]
D6	debug[5]
D7	debug[4]
D8	debug[3]
D9	debug[2]
D10	debug[1]
D11	debug[0]
E2	gl_reset
E11	led_heater
E12	led_reg
F1	led_copper
F3	led_lcd

Table B-1 · Subset of A3P250-FG144 Pin List Usage Specific to System Management Board

F4	led_pci
F12	clk_50Mhz
G1	PCI_PRSNT1
G4	PCI_PRSNT2
G8	sram_ft
G9	lcd_tr
G10	lcd_re
G11	eth_rst
H2	eth_an_en
H3	eth_an1
H4	eth_an0
H6	lcd_db[7]
H7	lcd_db[6]
H8	lcd_db[5]
H9	lcd_db[4]
H11	lcd_db[3]
J1	lcd_db[2]
J2	lcd_db[1]
J4	lcd_db[0]
J5	lcd_rw
J6	lcd_rs
K1	debug[18]
K2	debug[19]
K3	debug[20]
K4	debug[21]
K5	debug[22]
K6	debug[23]
L3	clk_25Mhz
M2	debug[17]
M3	debug[16]
M4	debug[15]
M5	debug[14]
M6	debug[13]

Table B-1 · Subset of A3P250-FG144 Pin List Usage Specific to System Management Board

M7	debug[12]
M8	debug[11]

Table B-2 · Subset of A3P250-FG144 Pin List Usage Specific to System Management Board by Function Order

Clocks and Resets	Pin Name
clk_25Mhz	L3
clk_50Mhz	F12
gl_reset	E2
CoreUART(A3P-M1AFS)	**Pin Name**
rx	B5
tx	B6
DIP Switch	**Pin Name**
dip[0]	B10
dip[1]	A11
dip[2]	A10
dip[3]	A9
dip[4]	A7
dip[5]	A5
dip[6]	A4
dip[7]	A3
Ethernet	**Pin Name**
eth_an_en	H2
eth_an0	H4
eth_an1	H3
eth_rst	G11
KeyPads	**Pin Name**
key[0]-select	C8
key[1]-down	C11
key[2]-up	C12
key[3]-right	C9
key[4]-left	C10

Table B-2 · Subset of A3P250-FG144 Pin List Usage Specific to System Management Board by Function Order

LCD Display	Pin Name
lcd_blk	B7
lcd_db[0]	J4
lcd_db[1]	J2
lcd_db[2]	J1
lcd_db[3]	H11
lcd_db[4]	H9
lcd_db[5]	H8
lcd_db[6]	H7
lcd_db[7]	H6
lcd_re	G10
lcd_rs	J6
lcd_rw	J5
lcd_tr	G9
LEDs	**Pin Name**
led[0]-red	C7
led[1]-red	C6
led[2]-red	C5
led[3]-red	C3
led[4]-green	C2
led[5]-green	C1
led[6]-green	B10
led[7]-green	B9
led_copper	F1
led_heater	E11
led_lcd	F3
led_pci	F4
led_reg	E12
Miscellaneous	**Pin Name**
PCI_PRSNT1	G1
PCI_PRSNT2	G4
sram_ft	G8

Table B-2 · Subset of A3P250-FG144 Pin List Usage Specific to System Management Board by Function Order

Spare I/Os	Pin Name
debug[0]	D11
debug[1]	D10
debug[2]	D9
debug[3]	D8
debug[4]	D7
debug[5]	D6
debug[6]	D5
debug[7]	D4
debug[8]	D3
debug[9]	D2
debug[10]	D1
debug[11]	M8
debug[12]	M7
debug[13]	M6
debug[14]	M5
debug[15]	M4
debug[16]	M3
debug[17]	M2
debug[18]	K1
debug[19]	K2
debug[20]	K3
debug[21]	K4
debug[22]	K5
debug[23]	K6

C

Board Schematics

This section provides board schematics for the M1 System Management Board, which uses an ARM®-enabled Actel M1AFS1500-FG484 device, together with an Actel A3P250-FG144.

Note: The previous System Management Kit was exactly the same board, but fitted with the smaller CoreMP7-enabled M7AFS600-FG484 device, instead of the Cortex-M1-enabled M1AFS1500-FG484 device.

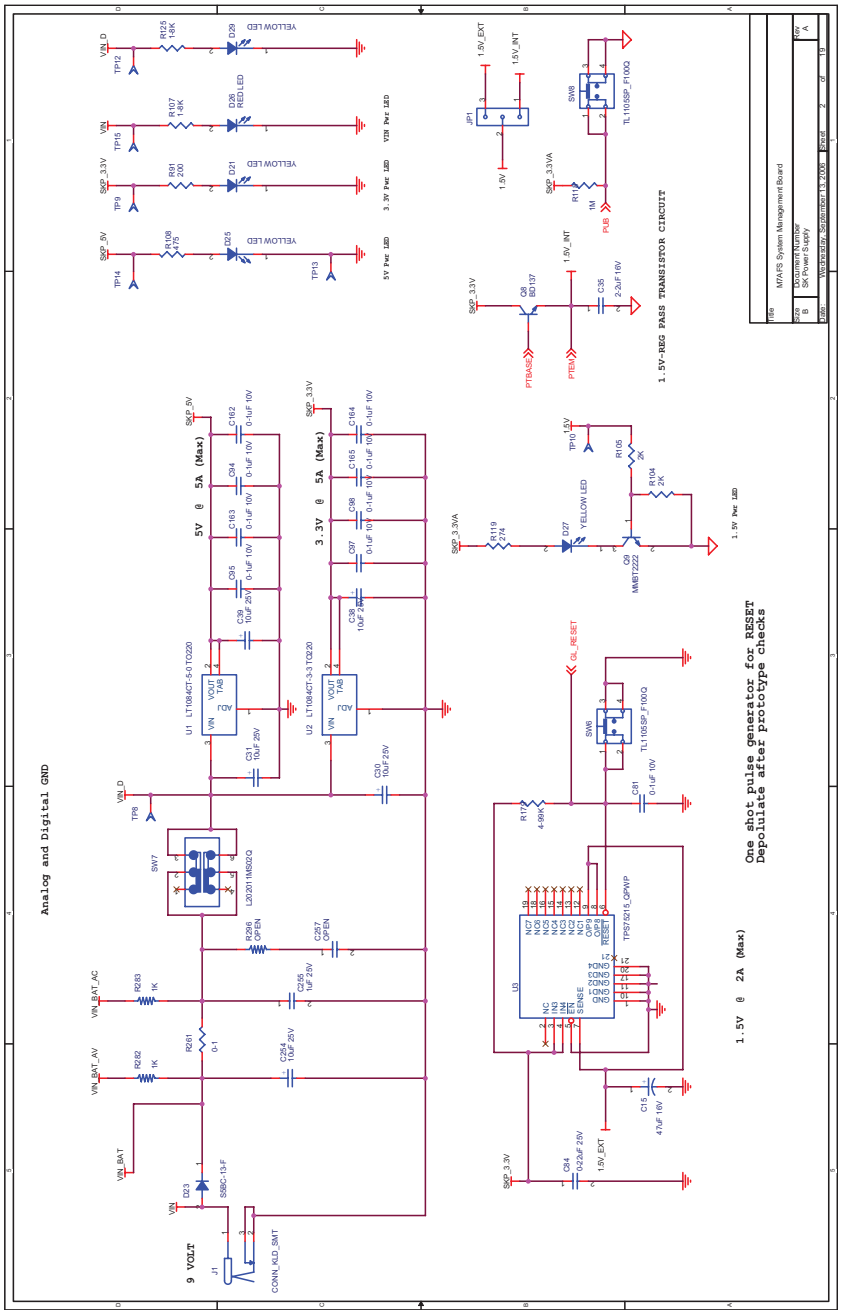

Figure C-1. SK Power Supply

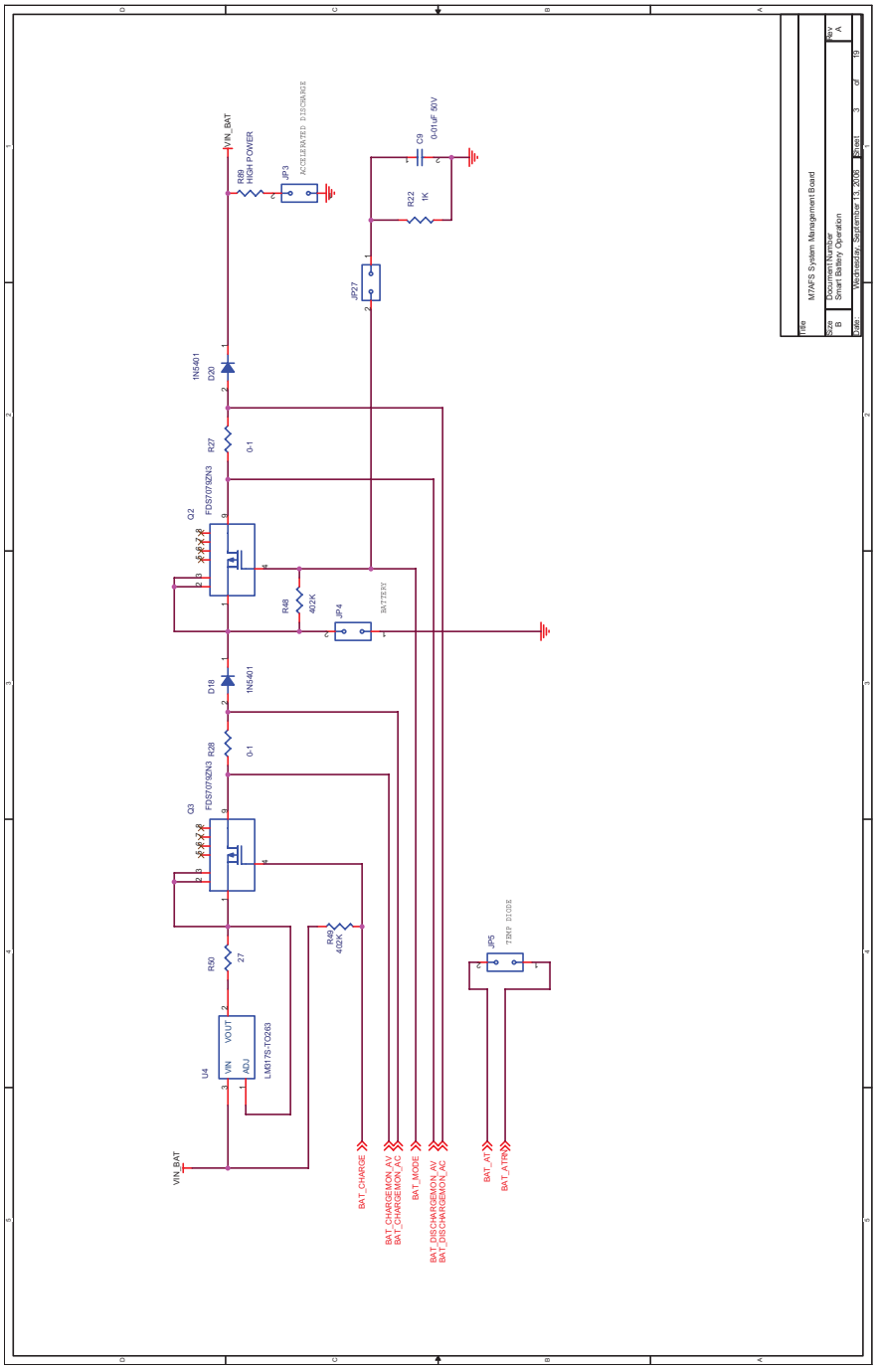

Figure C-2. Smart Battery Operation

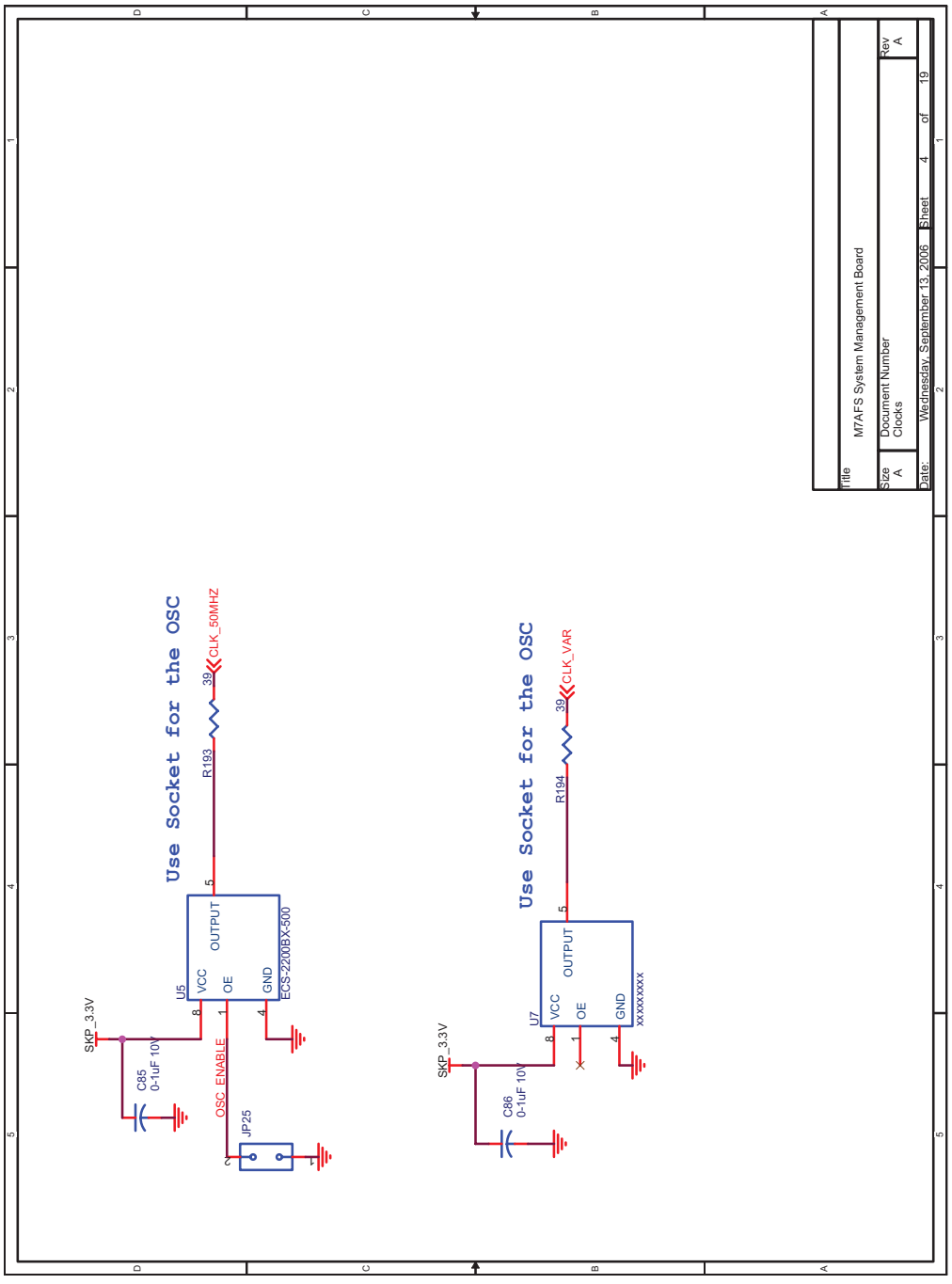

Figure C-3. Clocks

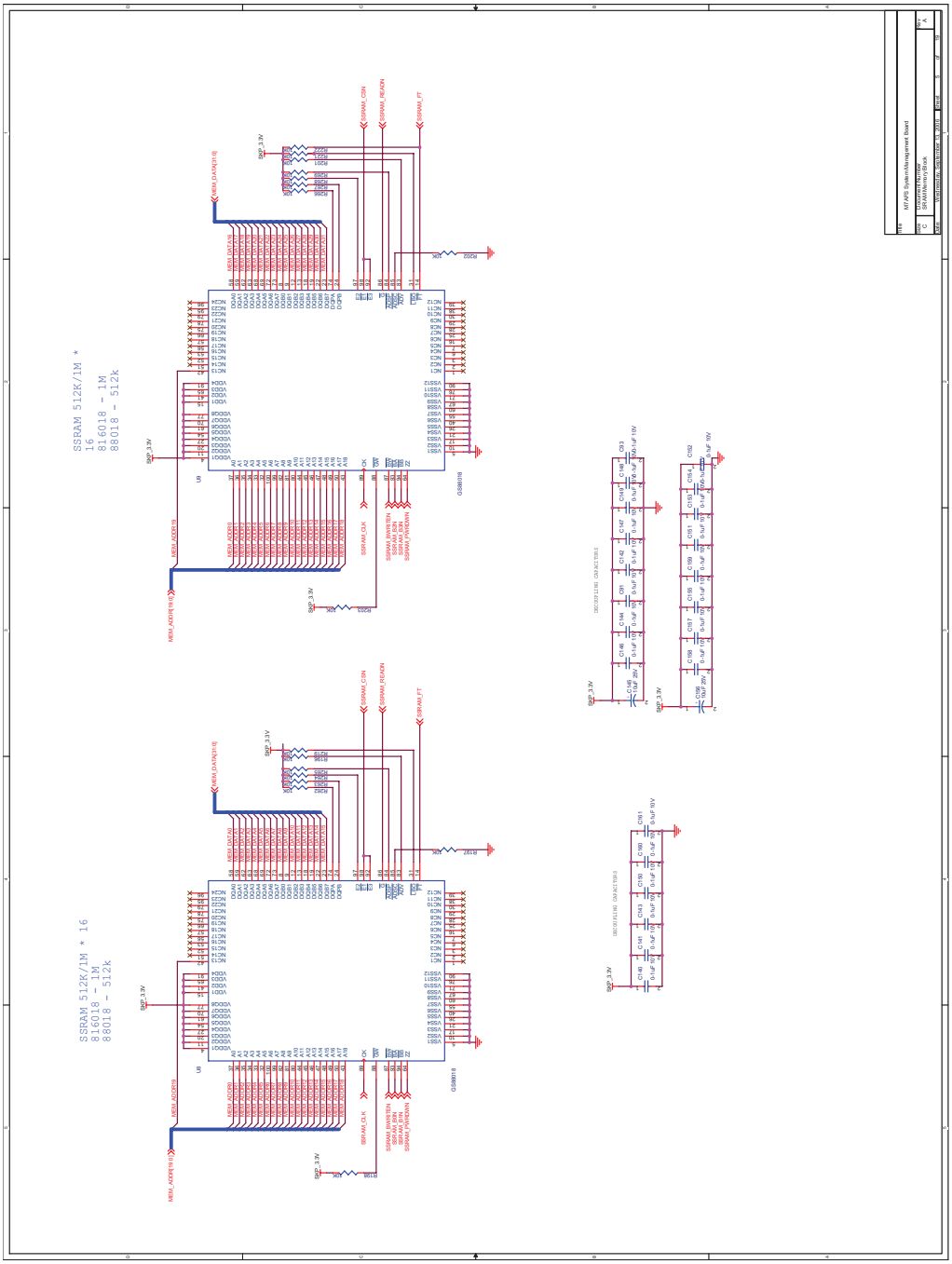

Figure C-4. SRAM Memory Block

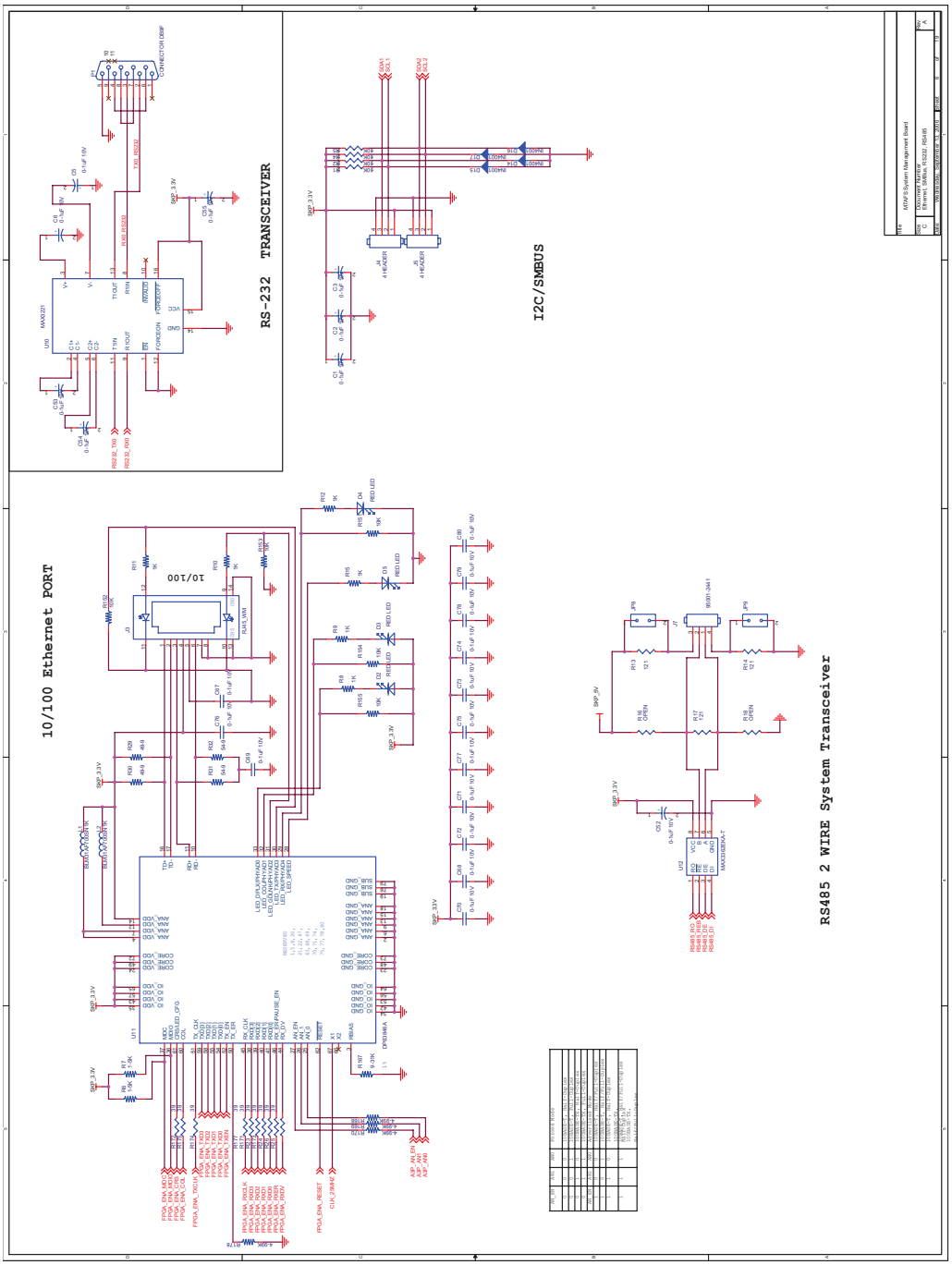

Figure C-5. Ethernet, SMBus, RS232, RS485

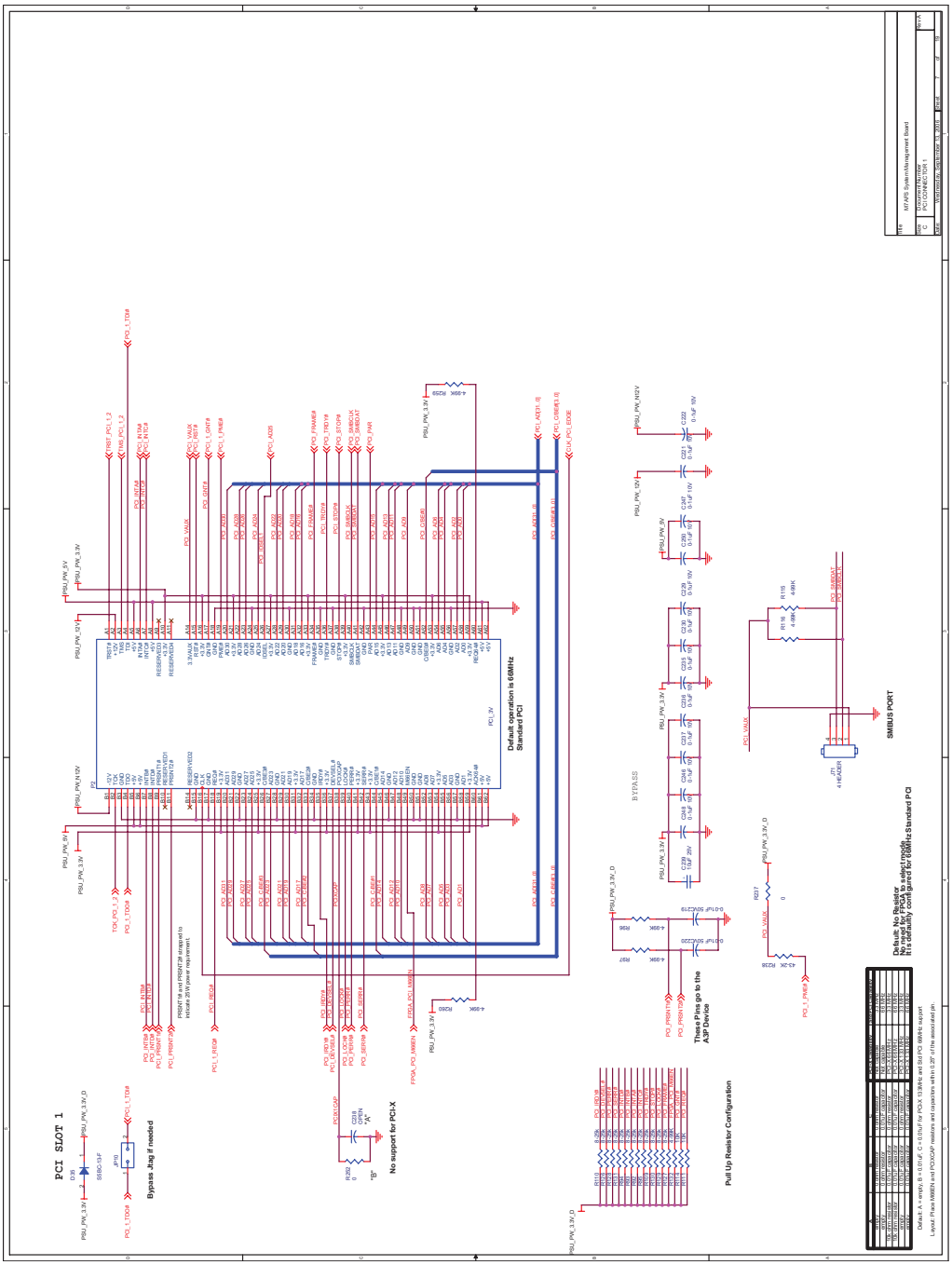

Figure C-6. PCI Connector 1

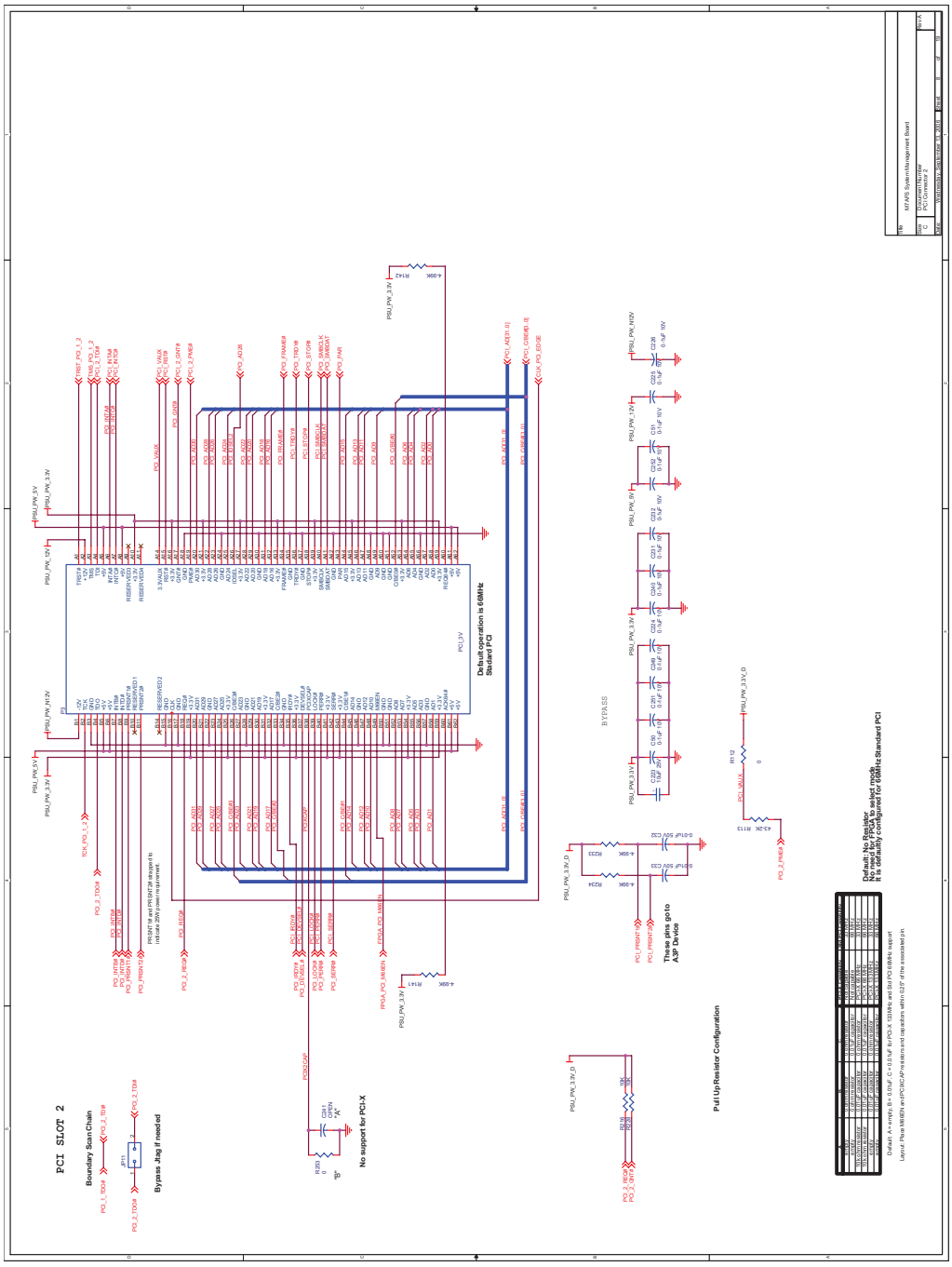

Figure C-7. PCI Connector 2

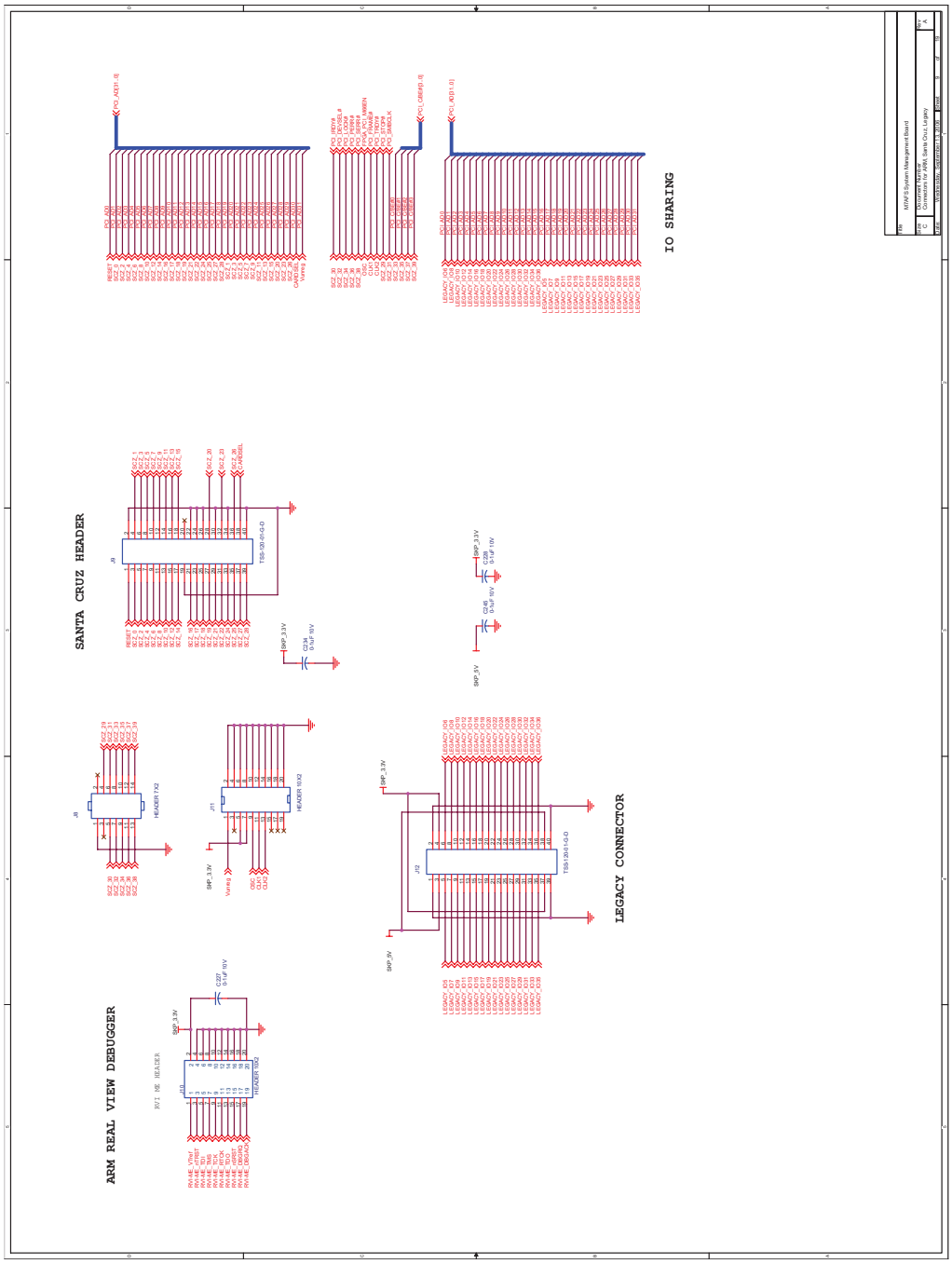

Figure C-8. Connections for ARM, Santa Cruz, Legacy

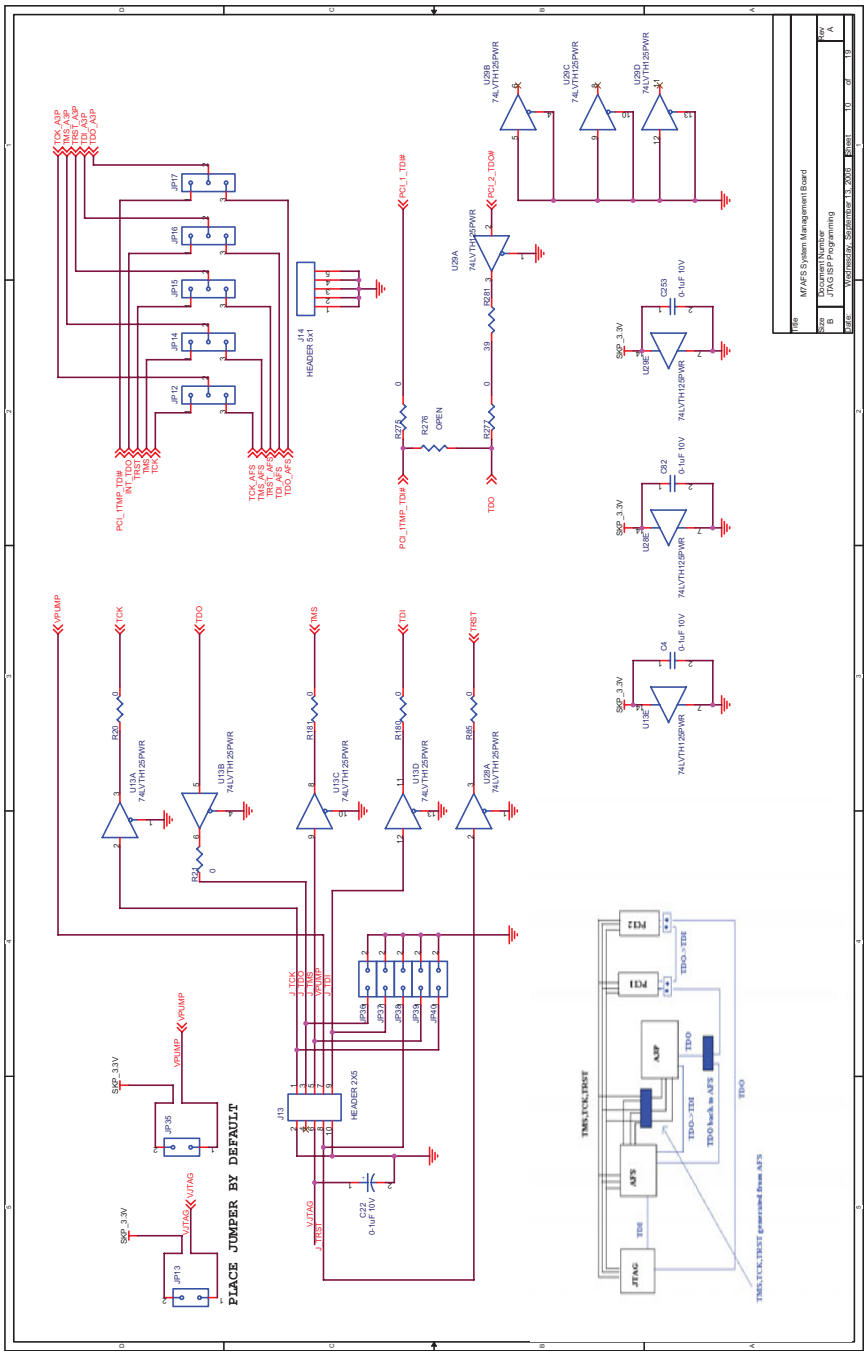

Figure C-9. JTAG ICE Programming

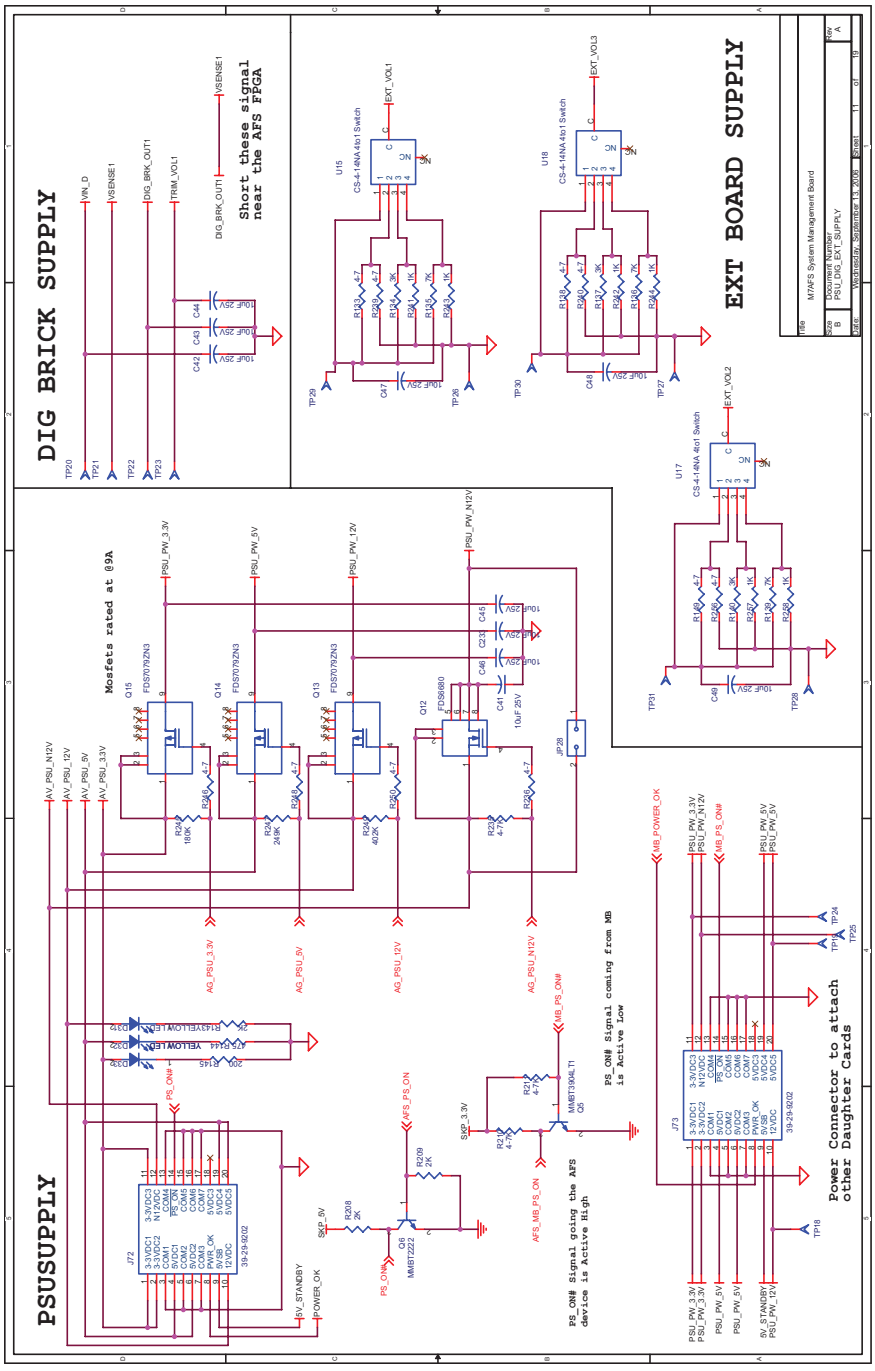

Figure C-10. PSU_DIG_EXT_SUPPLY

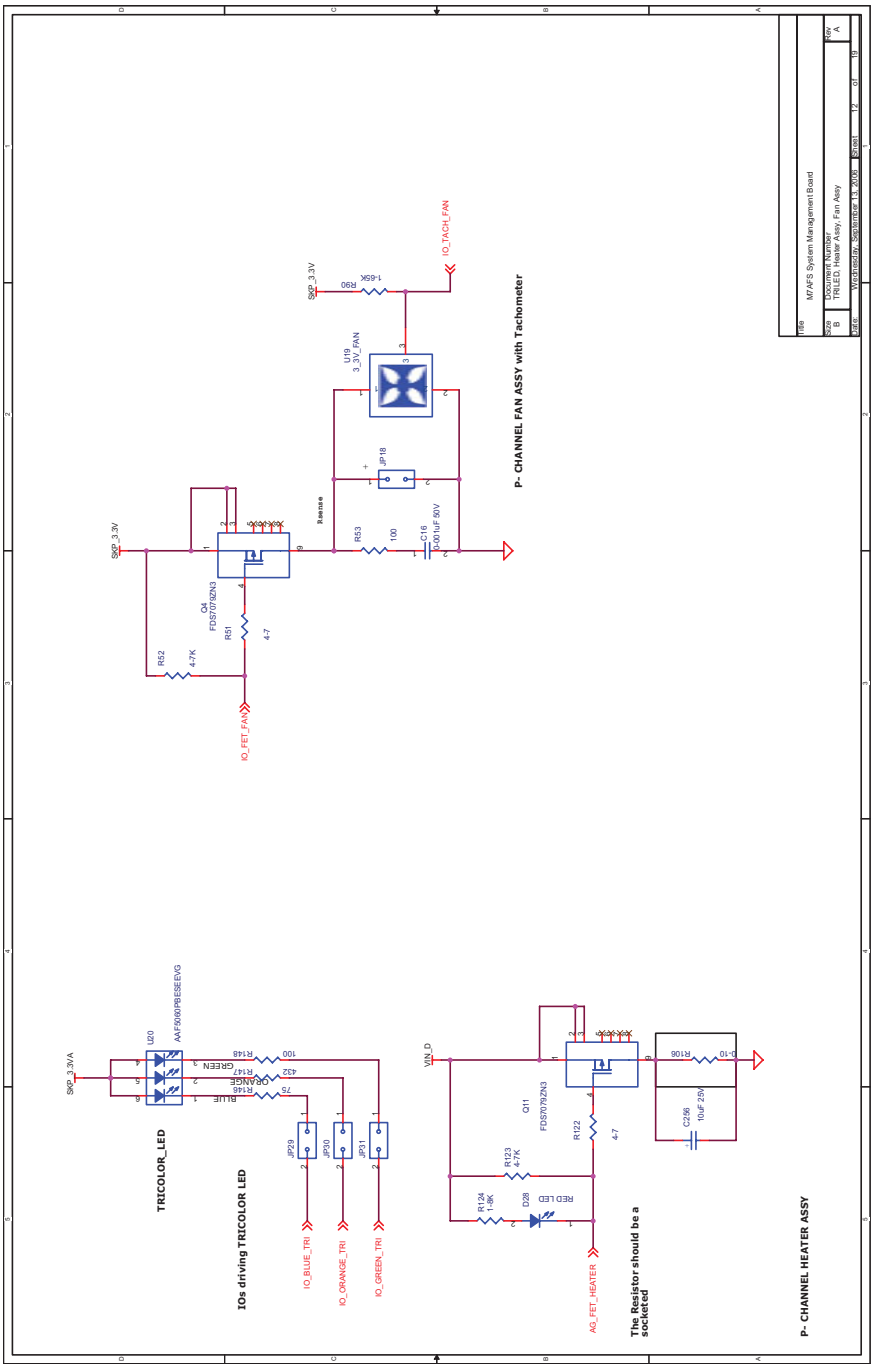

Figure C-11. Tri-Color LED, Heater and Fan Assembly

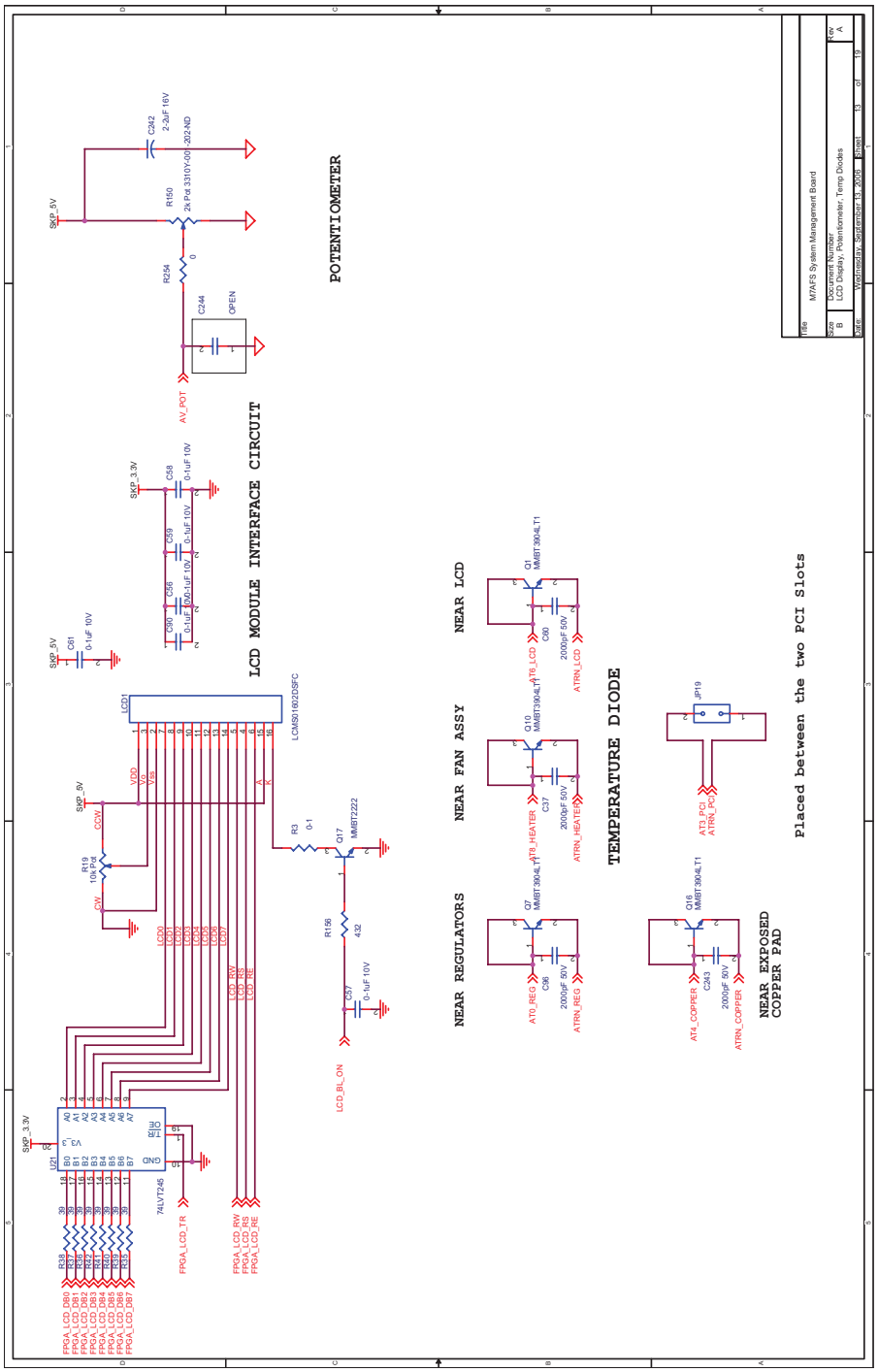

Figure C-12. LCD Display, Potentiometer, Temperature Diodes

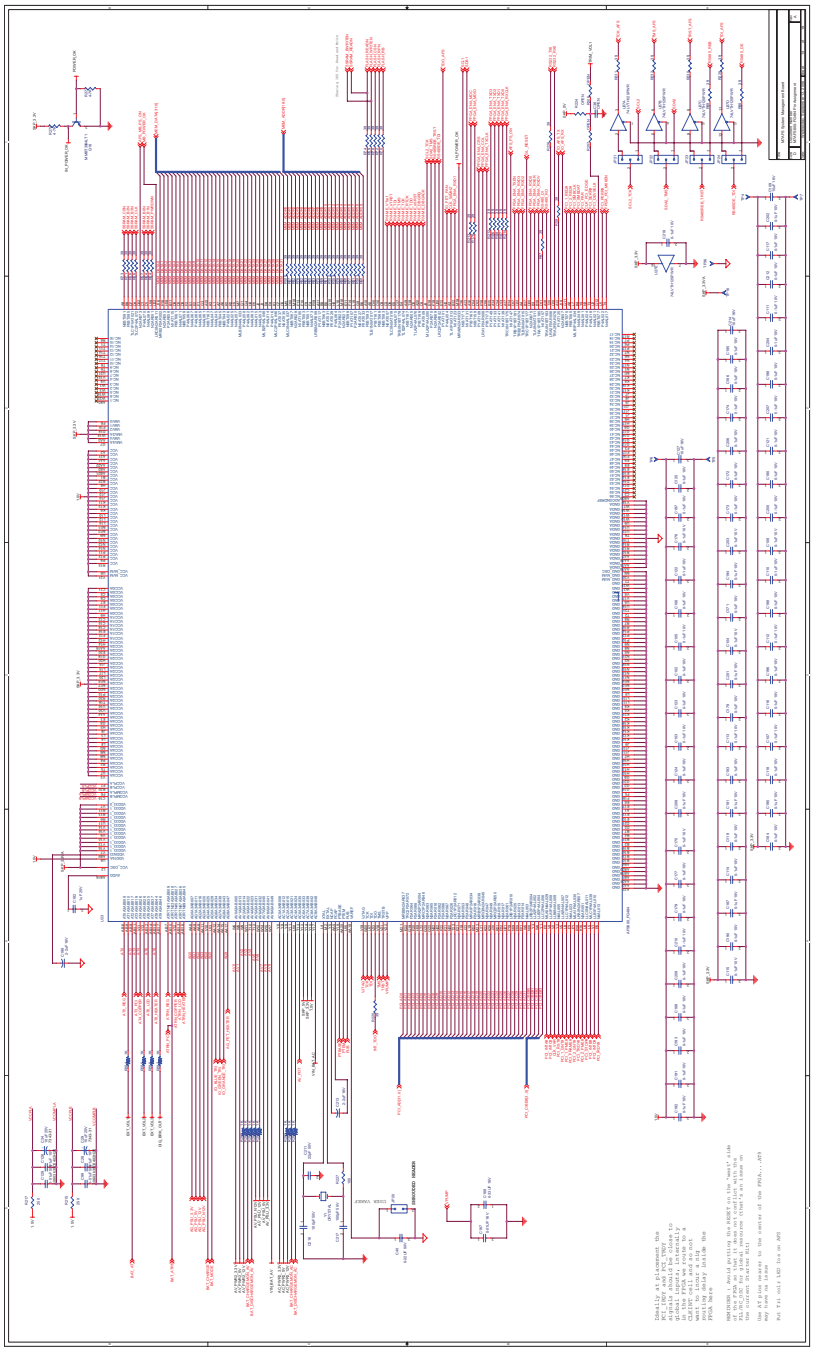

Figure C-13. M1AFS1500-FG484 Pin Assignment

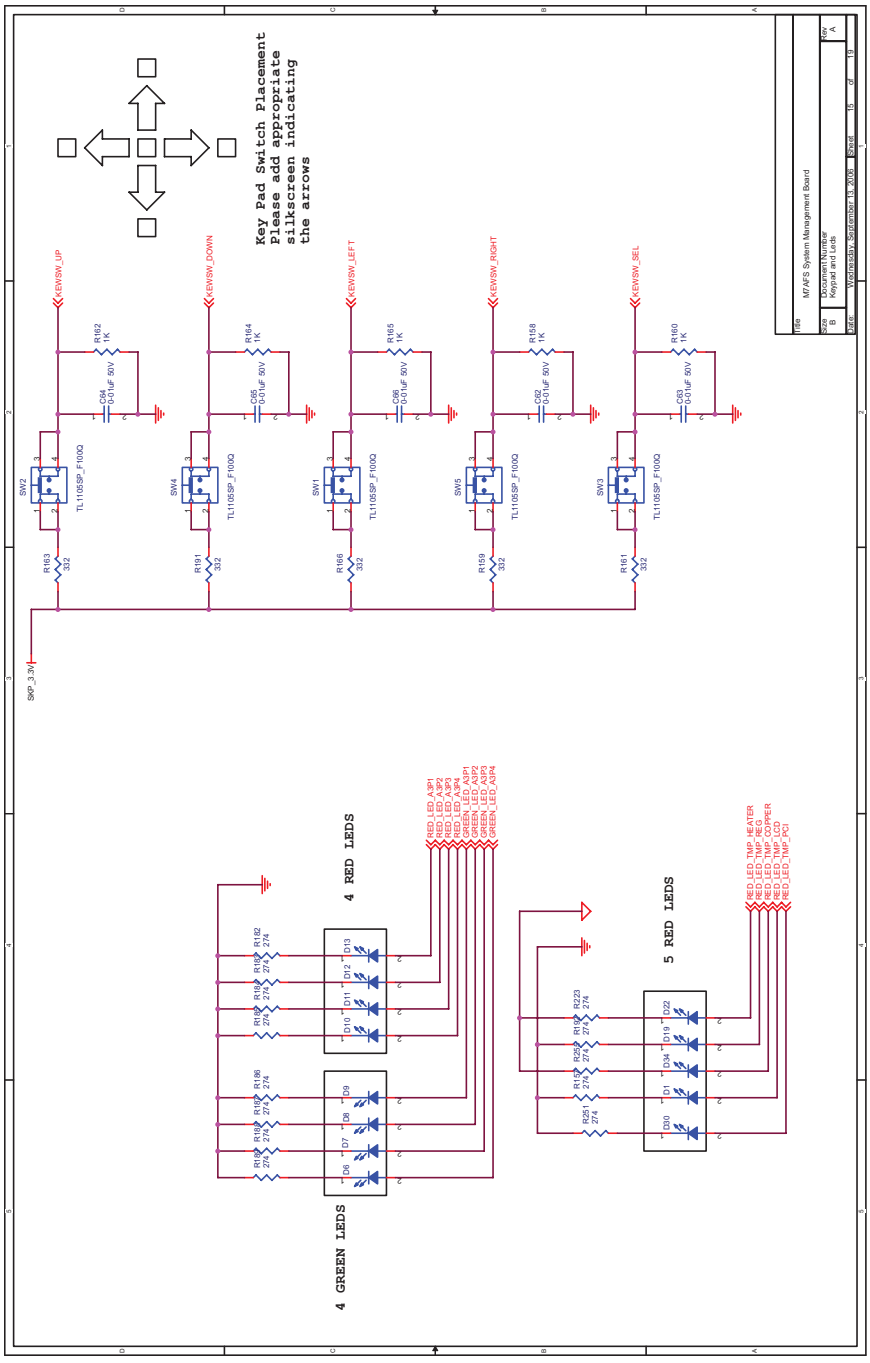

Figure C-14. Keypad and LEDs

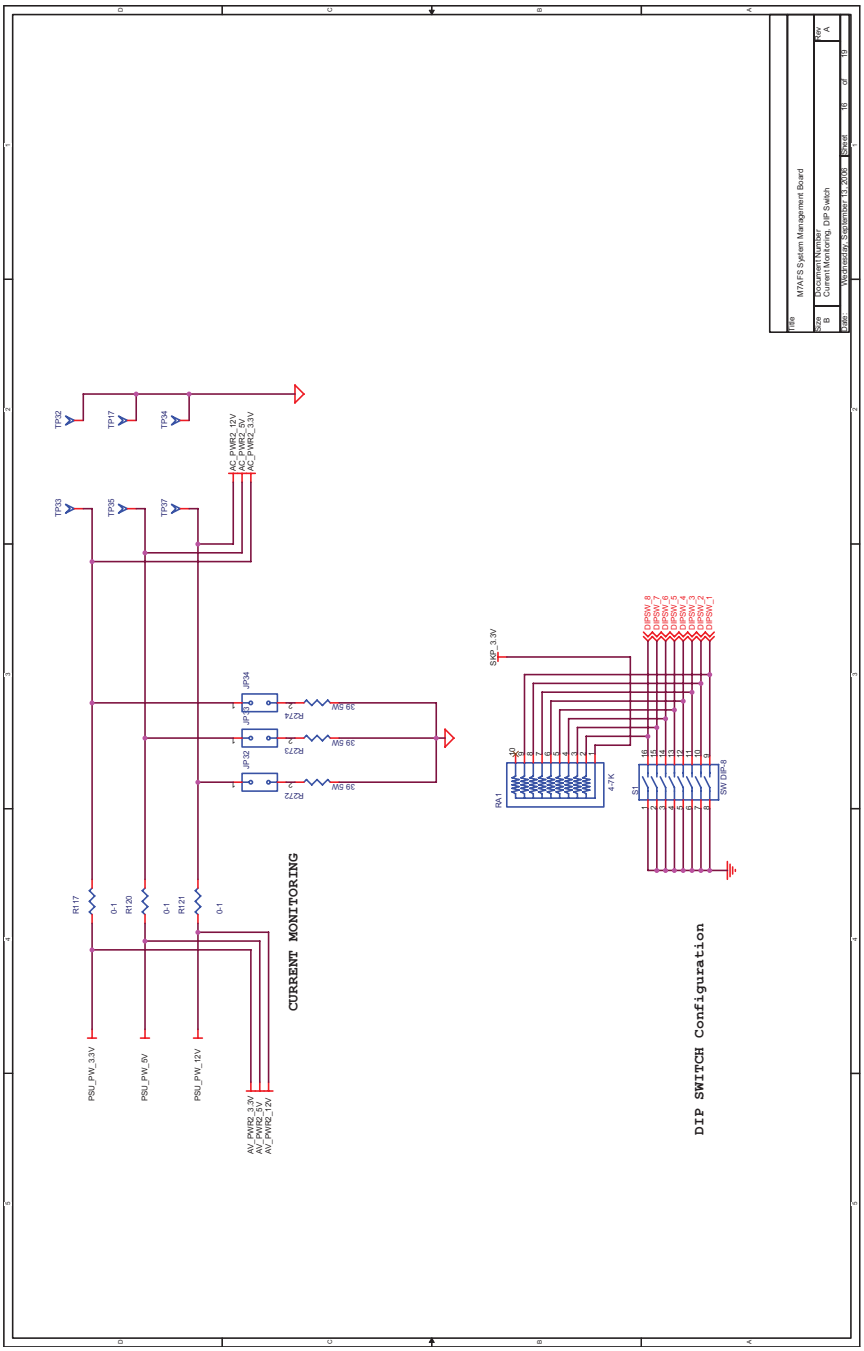

Figure C-15. Current Monitoring, DIP Switch

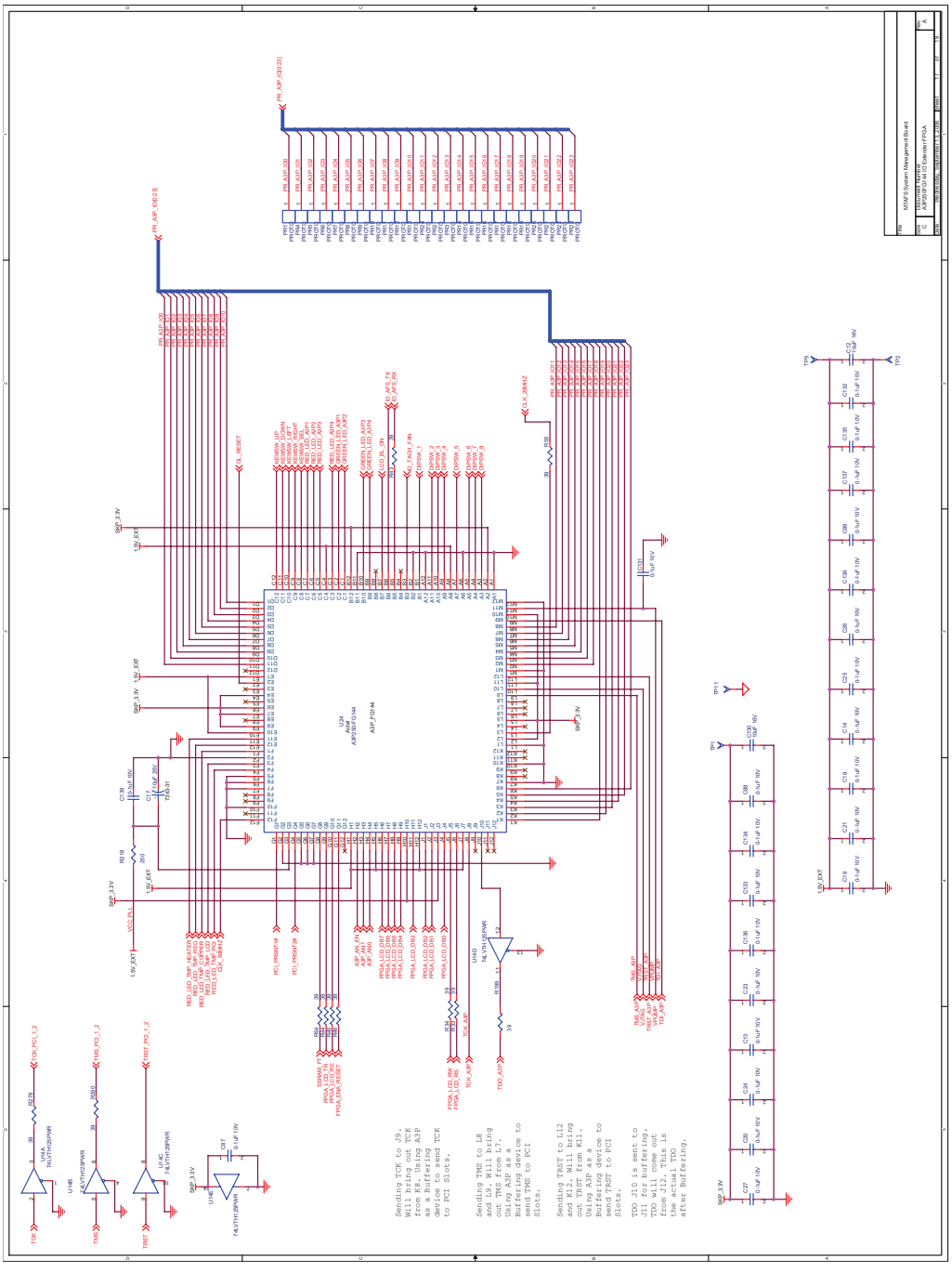

Figure C-16. A3P250-FG144 IO Extender FPGA

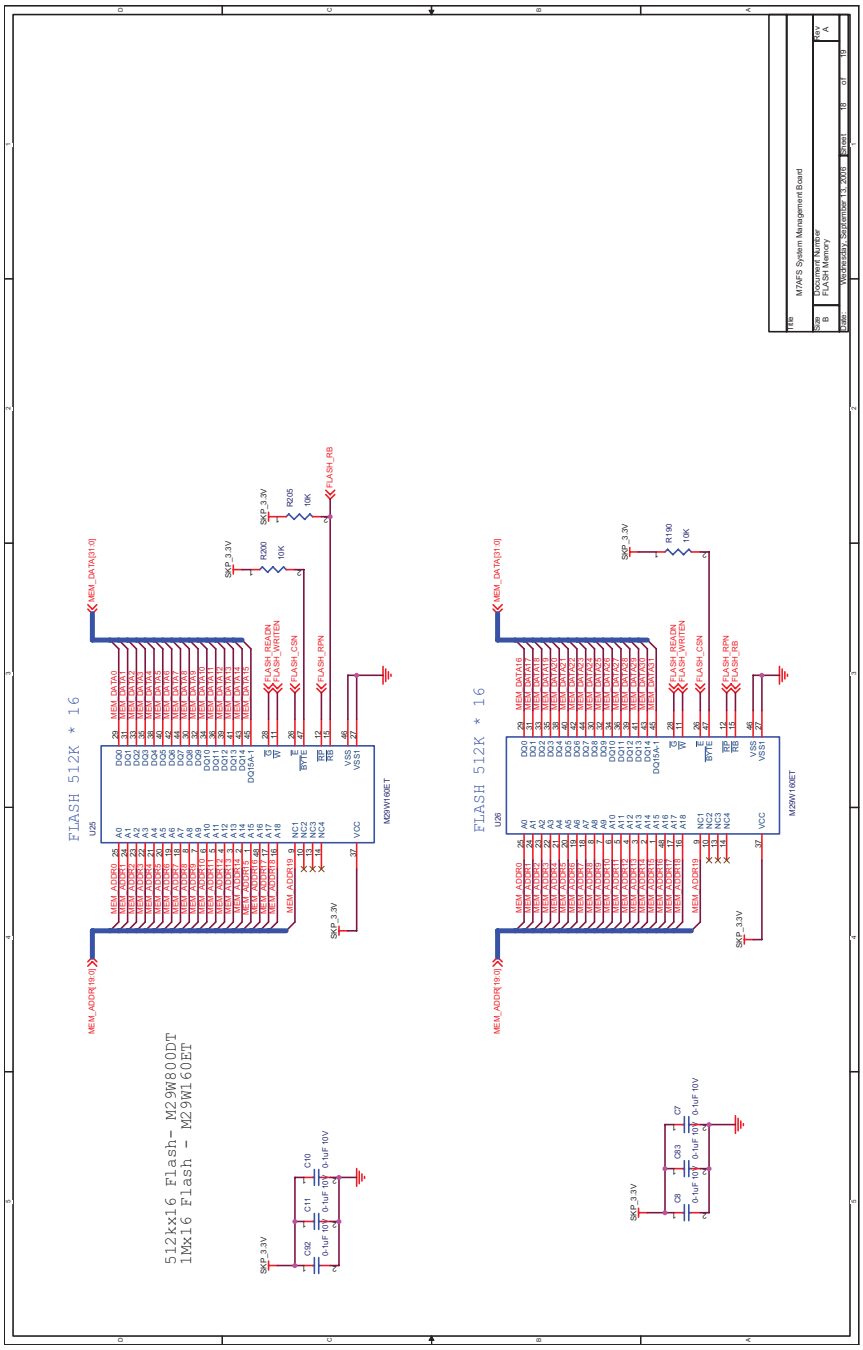

Figure C-17. Flash Memory

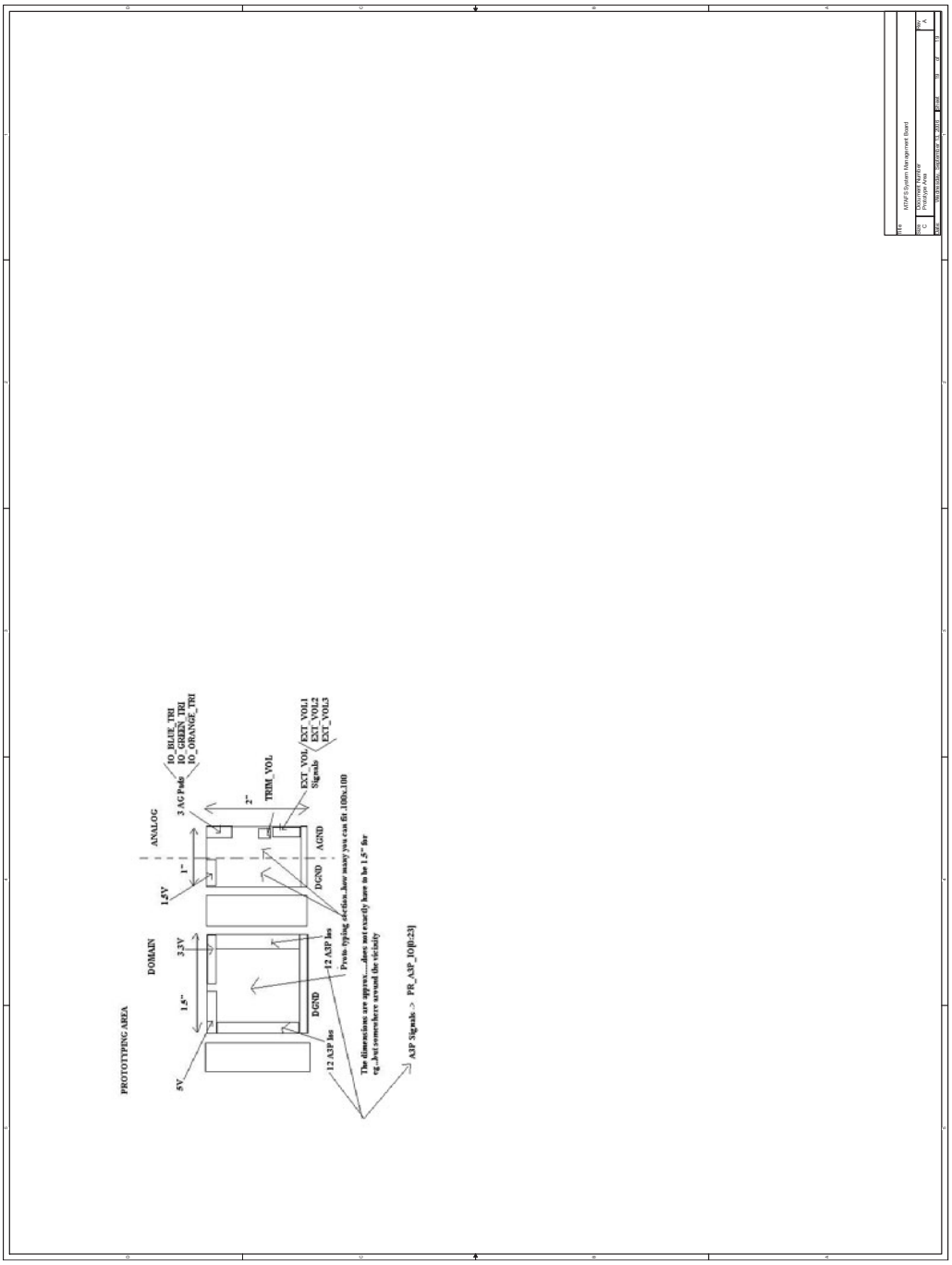

Figure C-18. Prototype Area

D

Board Stackup

The Fusion evaluation board is a 14-layer board. The stackup of each layer of copper is shown in Figure D-1. Some layers use 2 oz. weight copper to allow for higher currents to be passed; other layers use 1 oz. or 0.5 oz. weight copper. The thicknesses of the copper layers is shown in mils (thousandths of an inch) next to each layer.

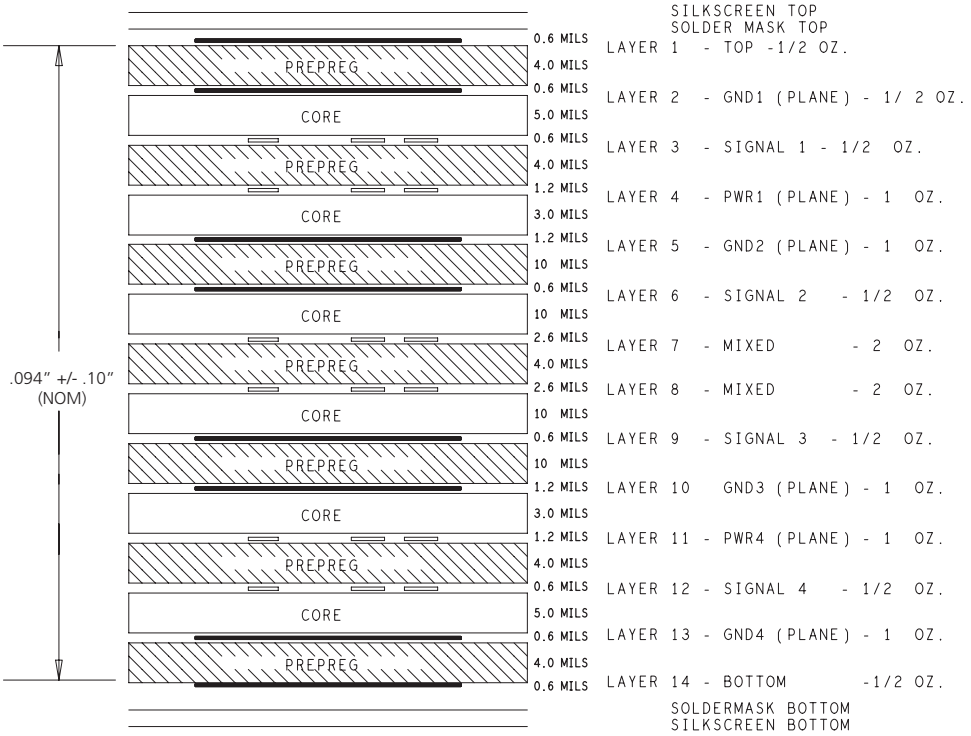

Figure D-1. Board Stackup

Analog signals require good grounding when used for temperature and current monitoring due to the very small signal values involved. The board stackup allows the best possible signal integrity. Use of the same layer by split analog and digital ground planes stops digital ground bounce from affecting analog ground bounce, which would occur if an entire layer of digital ground was placed above an entire layer of analog ground.

The M1 System Management Board has multiple ground planes, one for each signal layer, and a power plane above each signal layer to allow construction of microstrip and stripline for impedance control. Each ground layer is split into a digital ground and an analog ground. There are four separate ground planes used in the M1 System Management Board. The geometry of the analog section and the digital section in each ground plane is the same across ground planes (the digital areas overlap only other digital areas, and the analog areas overlap only other analog areas) to minimize cross-coupling between analog and digital grounds between the layers. To prevent earth loops, each layer has the analog and digital grounds connected at only one point, which is common between all layers.

E

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

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