MachXO™ Standard Evaluation Board - Revisions 001 & 002

User's Guide

March 2008
Revision: EB21_01.6

Introduction

The MachXO Standard Evaluation board provides a convenient platform to evaluate electrical characteristics of the MachXO device, and to evaluate, test and de-bug custom logic designs. The board features a MachXO device in a 256-ball fpBGA package. The MachXO I/Os are connected to a rich variety of interfaces, including an 8-bit input switch, LEDs, PCB test points, 0.10" general purpose headers and optional high-speed SMA connectors. The board includes selectable power for mixed core I/O voltage operation. A 33MHz oscillator, as well as an ispClock™ PLL synthesis device are also included on the board.

Features

- MachXO in 256-ball fine pitch Ball Grid Array package (MachXO640 or MachXO2280)
- Single printed circuit board solution
- Eight LEDs for visual feedback
- 8-bit input switch
- General purpose push-button
- 1149.1 JTAG programming/boundary-scan interface
- Built-in power supply operating with an DC input between 5V and 20V
- Selectable CORE voltage for the MachXO
- Selectable voltages for a portion of the I/O banks
- Built-in adjustable oscillator for reference clocking source
- Lattice ispClock5610 multiple output PLL
- SMA connector landing pads (SMA connectors not populated) to MachXO clock input/general purpose I/O pins
- RJ-45 connector (not populated)
- LCD/GPIO footprint
- 100mil center-center test point grid
- Impedance controlled Mictor (not populated)

General Description

The heart of the board is the MachXO programmable logic device in a 256-ball fpBGA package. The board is designed to cover a broad range of core and I/O voltage requirements. The MachXO "C" grade devices require a core voltage supply between 1.5V to 3.3V and an auxiliary 3.3V supply. The "E" grade devices require a core voltage supply at 1.2V and an auxiliary I/O supply at 3.3V. The MachXO Standard Evaluation Board provides three supply voltages, all sourced from a 5V to 20V external source (or sourced individually via the banana jack inputs). The board provides fixed 1.2V and 3.3V power rails and a single adjustable voltage that ranges from 1.2V to 3.3V. It is possible to use external power supplies to override the fixed output levels if desired. The voltage supplied to the MachXO core is selectable. The core voltage is changed by moving a single current sense resistor.

Once a correct set of supply voltages has been applied to the MachXO, the device can be programmed. The MachXO can be programmed and verified with a Lattice JTAG download cable, which should be connected to the 1x10 SIP header on the board (1149.1 JTAG interface). The ispVM® System software controls the programming and verification process. The ispVM System software is available for download from www.latticesemi.com/software.

The evaluation board also includes a Lattice ispClock5610. This part is also programmed using the same JTAG interface. The ispClock5610 can be used to generate synthesized clock inputs to the MachXO device.

The evaluation board includes additional components to aid in evaluating the MachXO PLD. These are described in the following sections in more detail.

Additional Resources

Additional resources related to this board can be downloaded from the web at www.latticesemi.com/boards. Click on the appropriate evaluation board, then see the blue "Resources" box on the right of the screen for items such as: updated documentation, downloadable software, sample designs and more.

Getting Started

In order to use the MachXO Standard Evaluation Board, it must first be powered. Follow the guidelines in the Power Supply section below for details.

The MachXO Standard Evaluation Board is shipped from the factory pre-configured with a sample program loaded in both the MachXO and ispClock devices. The source code and programming files are available for download from the Lattice web site at: www.latticesemi.com/boards. The sample programs operate as follows.

MachXO: Setting all of the 8-bit input switches to ON causes the associated LEDs to count in one direction (8-bit binary counter). Setting all of the 8-bit input switches to OFF reverses the direction of the count. If the switches are not all ON or all OFF, the LEDs for the switches that are ON will light up. Additionally, other I/Os on the MachXO device are also toggled using the internal counter outputs. See the source code and preference file available on-line for more information.

ispClock5610: The ispClock5610 sample program generates a 33MHz clock input to the MachXO device.

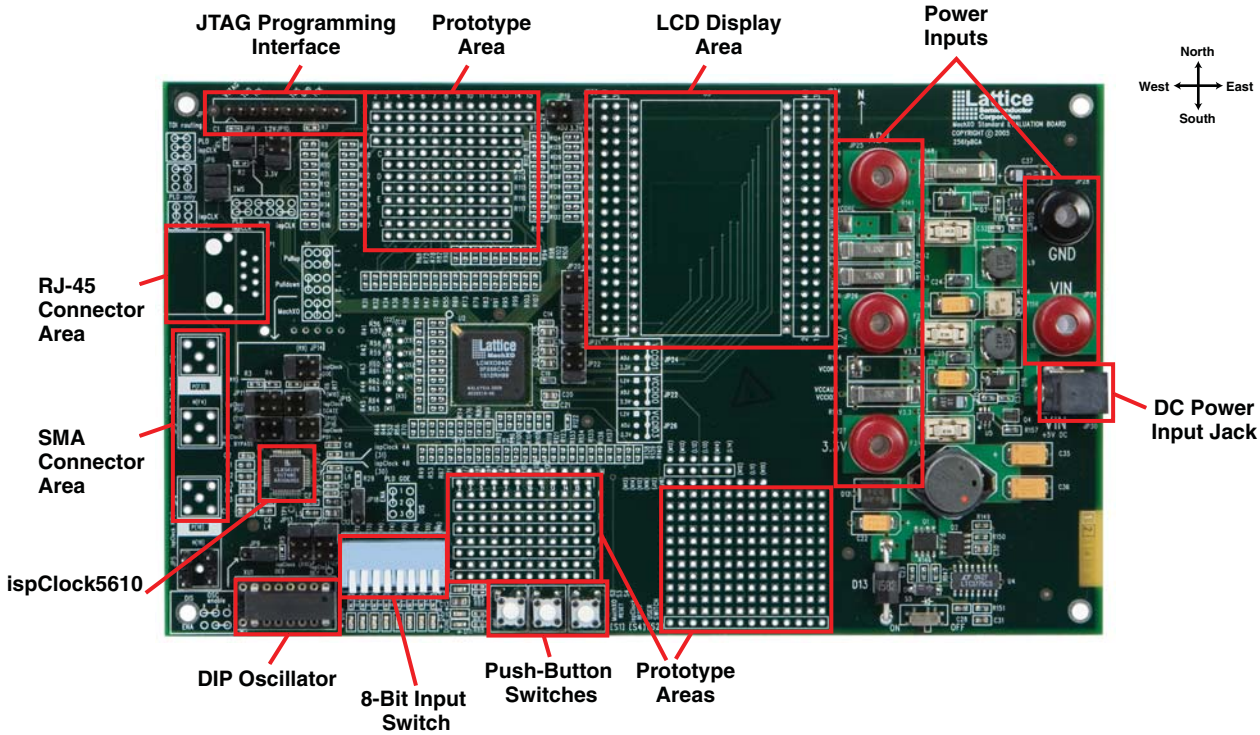
To reprogram the board, you will need the following items:

- **ispLEVER Software:** HDL design support for the MachXO device is included in both ispLEVER 5.0 SP1 and downloadable ispLEVER-Starter 5.0 SP1 (or later) software tools
- **ispVM System:** This is the Lattice programming management tool which is used to download custom ispLEVER designs from your PC to the MachXO device via an ispDOWNLOAD® cable. The ispVM System software is available for download from the Lattice web site at: www.latticesemi.com/ispvm.
- **ispDOWNLOAD Cable:** An ispDOWNLOAD Cable is required to connect your PC to the MachXO Standard Evaluation Board. ispDOWNLOAD Cables are available for purchase separately from the Lattice on-line store (www.latticesemi.com/store) or any Lattice distributor. For more information see: www.latticesemi.com/products/devtools/hardware/ispdownload/

MachXO Standard Evaluation Board Functional Description

The MachXO Standard Evaluation Board is comprised of several primary functional blocks as shown in Figure 1. In the descriptions below, locations of components and board features are described relative to a compass symbol placed adjacent to the Lattice Semiconductor logo. For example, the DIP oscillator is on the southwest corner of the board, and the Lattice logo is on the northeast corner of the board.

Figure 1. MachXO Standard Evaluation Board



Power Supply

The MachXO Standard Evaluation Board includes two locations to apply power. On the east side of the board are a pair of banana jacks (JP28 and JP29) and a coaxial DC connector (JP30), which receive power from either a bench power supply or a brick style power supply. A DC source between 5.0V and 28.0V must be applied in order to power the board. The coaxial DC connector uses a 2.5mm central pin, with a 6.3mm outer diameter barrel.

The output from the DC system is controlled by switch S5. Switch S5 is in the southeast corner of the board. This is a small surface mount switch that enables and disables the LTC1775 DC-DC conversion chip. The output voltages from the power supply are enabled when the switch is in the "on" position.

The 5.0V to 28.0V DC input voltage is converted by DC-DC converters and switching power supplies to provide 3.3V, 1.2V, and an adjustable DC source on the board. The output from these supplies travels through surface mounted fuse holders. Fuses are supplied and prevent over-current conditions from damaging the components on the board (Vendor: Littlefuse, Make: Nano SMF Very Fast Acting, 1.5A or 3A).

Due west of the fuse blocks are more banana plug connectors. These connectors provide an alternate means for applying DC voltage levels to the board. To apply voltages not supplied by the on-board power section, **first remove the appropriate fuse from the fuse holder**. Then connect an alternate DC supply to the banana plug connector associated with that fuse.

Table 1. Power Supply Fuses

Fuse Number	Supply Rail Enabled/Disabled	Banana Connector Input
F1	V_{ADJ}	JP25
F2	1.2V	JP26
F3	3.3V	JP27

Adjacent to JP25-27 are current sense resistors. These permit the measurement of the current flowing from each of the power supplies. A single resistor can be moved to permit 1.2V, 3.3V, or V_{ADJ} to supply V_{CORE} to the MachXO.

Table 2. MachXO Core Voltage Selection

Resistor	Voltage Supplied to the MachXO Core
R141	V_{ADJ}
R142	1.2V
R144	3.3V

The remaining current sense resistors permit the measurement of the V_{CCIO} current draw.

Table 3. MachXO I/O Voltage Rails

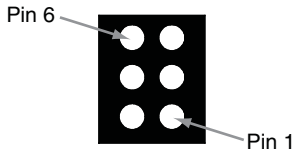
Resistor	I/O Bank Voltage
R143	1.2V
R145	3.3V
R148	V_{ADJ}

Four V_{CCIO} banks are available on the MachXO Standard Evaluation board. Three of the four I/O banks can be selected. V_{CCIO2} is always powered at 3.3V. This forces the JTAG interface to run at 3.3V. V_{CCIO0}, V_{CCIO1}, and V_{CCIO3} can be altered using jumpers.

Table 4. MachXO I/O Voltage Selection

Jumper Block	V_{CCIO} Controlled
JP20	1-2: V_{CCIO1} = 3.3V 3-4: V_{CCIO1} = V_{ADJ} 5-6: V_{CCIO1} = 1.2V
JP21	1-2: V_{CCIO0} = 3.3V 3-4: V_{CCIO0} = V_{ADJ} 5-6: V_{CCIO0} = 1.2V
JP22	1-2: V_{CCIO3} = 3.3V 3-4: V_{CCIO3} = V_{ADJ} 5-6: V_{CCIO3} = 1.2V

Figure 2. MachXO Standard Evaluation Board



Programmability

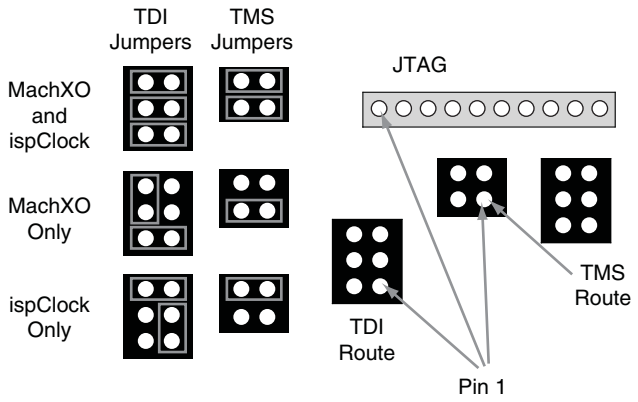
The programming interface for the MachXO (and ispClock5610) is located in the northwest corner of the board. The 1x10 header, JP7, is the connection point for the JTAG download cable. Jumpers JP6 and JP8 determine how the TDI/TDO chain and TMS pins behave.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the MachXO device and render the board inoperable.*

The default configuration for jumper JP6 is to configure the TDI from JP7 to be routed to the MachXO first. The TDO from the MachXO is routed to the ispClock device. TDO from the ispClock is connected to the JTAG header JP7. However Figure 3 shows the board can be configured to only have the MachXO accessible by the JTAG header. It can also be configured to only have the ispClock accessible by the JTAG header.

Jumper JP8 controls the TMS routing to the MachXO and the ispClock. The default configuration connects TMS to both the MachXO and the ispClock. When the MachXO is the only device in the JTAG chain, the ispClock TMS is pulled high, causing it to always go into Test-Logic-Reset mode. The MachXO has its TMS pin pulled high when the ispClock is the only device in the JTAG chain.

Figure 3. Programming Interface



Push Buttons and Status LEDs

There are three push-buttons and three LEDs in the south portion of the MachXO Standard Evaluation Board. Switch S2, the westernmost, asserts the Global Set/Reset input on the MachXO. When the button is pressed, LED D9 (red), illuminates. This gives clear visual evidence the GSR input has toggled. In order for the GSR to operate, it is necessary to instantiate the GSR macro in the VHDL/Verilog HDL source.

Immediately adjacent to the MachXO reset switch is the ispClock reset switch (S3). Pressing this button asserts RESET to the ispClock chip.

Finally, there is a general use push-button (S4). S4 is routed to T11 on the MachXO device. It is normally pulled high, and when pressed is asserted to ground. When pressed, LED D10 (yellow) illuminates.

Adjacent, westward, to S2 is diode D11 (green). This is a LED tied to a general purpose I/O on the MachXO. This LED signals that the MachXO is done being programmed. However, it can be used to signal any status desired. Evaluation bitstreams will tie output pin T6 to drive low, turning D11 on.

Global Output Enable

The MachXO device features a global output enable control. The GOE is routed to JP18, and the factory default setting on JP18 is to enable the MachXO outputs. The jumper on JP18 can be moved from the default setting to disable (tri-state) all of the MachXO I/Os.

Table 5. Global Output Enable

Jumper Block JP18	Output Enable State
1-2	Outputs disabled (tri-state)
2-3	Outputs enabled

MachXO and Support Interfaces

The MachXO Standard Evaluation Board includes basic support features for evaluating the performance and functionality of the MachXO device. This includes a prototyping area permitting arbitrary logic functions to be placed on

board. There are also locations to insert connectors and resistors. These connections are useful for performing I/O characterization.

The silk screen markings on the evaluation board are designed to make it easy to locate resources on the board and related connections to the MachXO.

- Parts are numbered in a consistent fashion. Each part starts at reference designator '1' in the northwest corner of the board (i.e. R1, C1, U1, L1…). The component number increases by one in a columnar fashion (i.e. southward). When the south edge of the board is reached, the count resumes slightly east, and at the north side of the board. Thus the highest numbered components will always be in the southeast corner of the board. This same numbering sequence is applied to the reverse side of the evaluation board.
- The alphanumeric pin position of the MachXO 256-ball fpBGA is indicated adjacent to most of the switch inputs, LED outputs, SMA connectors, and test points on the board. For example, the designator (F3) is located next to the SMA connector JP2. Thus MachXO pin F3 is connected to the center post of JP2.
- A solid white rectangle area near the SMA connectors denotes the positive side of a matched pair. The negative side of the matched pair has a white outline rectangle area.

Prototype Grids
The board includes five 100-mil center-center prototype grid areas consisting of plated through holes with various connections.

It is important to note the board conventions used to identify the through hole types:

- Any through hole with a square-shaped plated area is not connected to any device on the board, and provided for your convenience.

- Any round through-hole outlined with a thin white silkscreen rectangle is connected to ground.

- All other round through-holes are connected to the MachXO pin as indicated by the silkscreen.

Note: Some prototype grid test points may be connected to "no-connect" (NC) pin locations on the MachXO device. Consult the MachXO device datasheet for further details regarding the MachXO pinout.

Prototype Grid 1 and 2: Grid 1 is located in the northwest portion of the board. Grid 2 is due south of the MachXO device. Both areas have an alphanumeric grid located in the silkscreen indicating which plated through hole is attached to which MachXO pin.

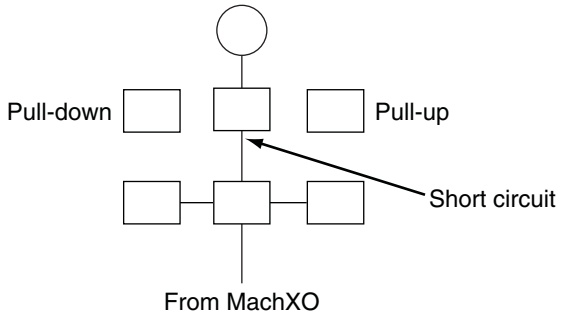
Both grids are intermixed with through holes attached to the ground plane. These ground holes are marked with a white silkscreened rectangle.

Both grids are also intermixed with unconnected locations. These are indicated with a square-shaped plated area.

For example, starting in the upper-left of Grid 1; location A2 and A3 are unconnected, location A4 is connected to the MachXO I/O pin A4, etc.

Both grids also have a series of pull-up/pull-down/inline resistors connected to the through holes. Figure 4 shows how these resistors may be arrayed around the prototype area.

Figure 4. Prototype Grid 1 and 2 Resistor Pad Configuration



The resistor pads are 0603 surface mount form factor. The 0603 resistor in the center has a short-circuit trace between the resistor pads. This permits the signal to be driven to the prototype area without the addition of a SMT zero ohm resistor. If a series resistor with a non-zero value is needed, this short-circuit trace can be removed.

The pull-up resistors within this grid can be configured to be pulled to one of the three available voltage rails on the board. Table 6 shows how the voltage rails are assigned. Refer to the schematic to determine which resistor pads connect to which MachXO I/O. The schematic also indicates which jumper block controls the pull-up voltage on each resistor. The schematic is included in Appendix A.

Table 6. Pull-up Voltage Selection

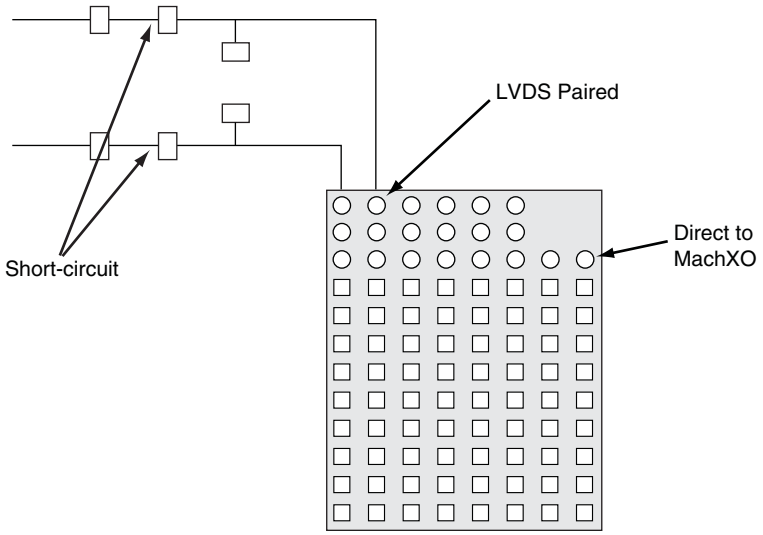
Jumper Block	Pull-up Voltage
JP10	1-2: 1.2V 3-4: V_{ADJ} 5-6: 3.3V
JP19	1-2: 1.2V 3-4: V_{ADJ} 5-6: 3.3V

Prototype Grid 3: Just west (left) of the MachXO is a small array of nine test points. The MachXO I/O pin connections are indicated in the silkscreen marking. For example, the top-left location connects to MachXO pin F5, etc. These test points are directly connected to the MachXO without any series resistors, and do not have any pull-up/pull-down resistors attached.

Prototype Grid 4: This grid is located in the south-east part of the board. This grid consists primarily of unconnected, square-plated through holes. The south edge of this grid has a row of through holes connected to ground. The north edge has a small quantity of through holes connected to the MachXO.

Figure 5 indicates how these test points are connected to the MachXO 256 fpBGA. The LVDS paired test points connect to a set of 0603 form factor resistors. These resistors permit series and parallel style terminations to be applied to the MachXO I/O. Note that some of these I/Os may be no-connects on the MachXO device depending on which MachXO device is populated on the board. Review the schematic and MachXO Family Data Sheet to determine which are available for use.

Figure 5. Prototype Grid 4



Prototype Grid 5: The last of the prototype grid is designed for use with an LCD display. U3 can be populated by a Lumex LCD-S501C39TR five-element, seven-segement LCD display. When this display is populated, it is mounted on the rows between U3 and JP23/JP24. JP23 and JP24 can then be populated with general-purpose headers. Jumpers can then be used to control connections between the MachXO device pins and the LCD.

When this LCD is not populated (default condition), the outer columns of JP23 and JP24 can be used as general-purpose I/O test points.

LED Displays

On the south edge of the board is a set of eight green 0603 form factor LEDs. These LEDs are connected to I/O pins dedicated to driving the LEDs. Table 7 shows which MachXO I/O controls each LED. The LEDs illuminate when the corresponding I/O is driven to V_{OL}.

Table 7. LED Pin Assignments

LED	MachXO I/O
D0	R11
D1	R12
D2	P11
D3	P12
D4	T13
D5	T12
D6	R13
D7	R14

Switches

The evaluation board includes an eight-bit input toggle switch at the south edge of the board. The MachXO I/O location for each bit in the switch is indicated on the PCB silkscreen. When in the up position, the switch is pulled to 3.3V via a 10K resistor. When in the down position, the switch is tied to ground.

Table 8. Switch Assignments

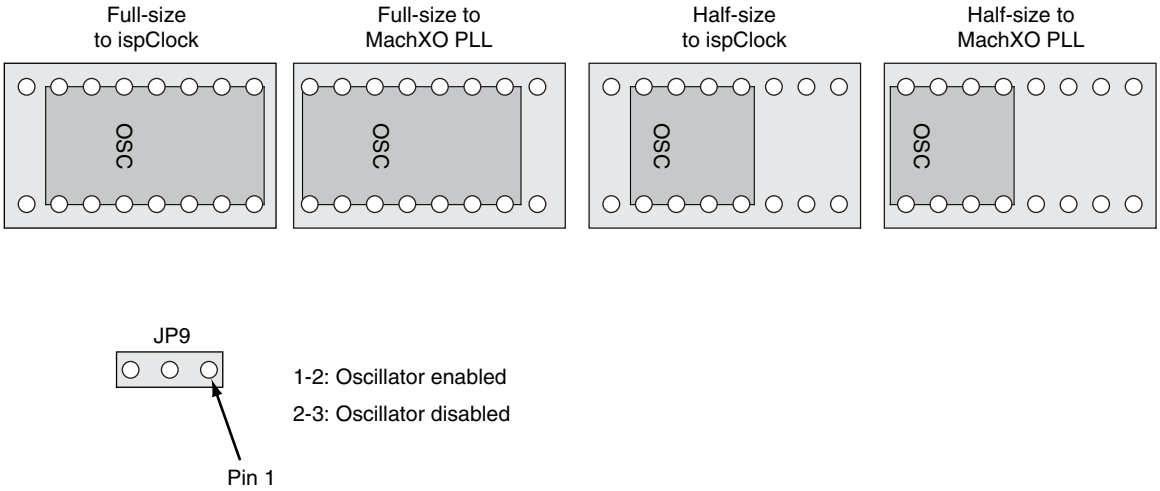
Switch	MachXO I/O
1	T3
2	R4
3	R5
4	P5
5	P6
6	T4
7	T5
8	R6

Oscillator and Clock Inputs

The MachXO Standard Evaluation Board provides the ability to supply selectable reference frequencies to the MachXO device. The board provides a unique clock source distribution method. A Lattice ispClock5610 is included on the board to provide a number of different clock frequencies to the MachXO device.

The ispClock5610 receives a reference clock from one of two sources on the board. The primary clock source for the ispClock5610 is the on-board DIP oscillator. In the southwest corner of the board is XU1. This is a socket for installing 300mil wide 3.3V DIP oscillators. Figure 7 shows how each type of oscillator can be placed in the DIP socket.

Figure 6. Oscillator Positions



Note: XU2 pin 9 is routed to one of the two PLLs included on larger MachXO devices. These MachXO PLLs are not available on the MachXO640 device. XU2 pin 9 provides input to the PLL_T input pin M5.

JP2 and JP3 are routed to the second set of PLL input pins on the MachXO device. On the MachXO640, these input pins are general purpose I/O. For larger MachXO devices, these same I/O pins are combination general purpose I/O and PLL inputs. The traces from JP2/JP3 are 50 ohm impedance, and have the same resistor pad structure described in Figure 6. JP2/JP3 provide the ability to insert differential clock sources. Review the schematic for the exact part reference numbers of the resistors.

The second way to provide a clock to the ispClock5610 is to use JP4 and JP5 SMA connectors. These SMA connectors are not installed by default. Also, by default the positive input from JP4 is disconnected from the ispClock5610. Beneath the ispClock5610 on the reverse side of the board are two resistor sites: R158 and R159. R158 connects XU2 pin 10 to the ispClock5610 positive clock input. R159 connects JP4 to the ispClock positive clock input. By default, R158 has a zero ohm resistor installed and R159 is left empty. This is done to prevent undesirable artifacts from appearing on the input clock due to trace stubs. R158 and R159 are placed in a way to reduce the length of any stub traces to an absolute minimum. When supplying a clock from JP4/JP5, R158 should be moved to R159 in order to connect JP4 to the ispClock5610.

Table 9. ispClock5610 Clock Source

Resistor	ispClock5610 Positive Source
R158	XU2 pin 10
R159	JP4

Once the clock source to the ispClock device has been defined, the ispClock can be programmed to generate clock frequencies for the MachXO. The ispClock5610 has five outputs from the internal PLL (0-4). The first four, 0-3, are applied directly to the MachXO clock input pins. The fifth output is brought out to TP2 and TP3, adjacent to the ispClock chip.

Table 10. Clock Connections

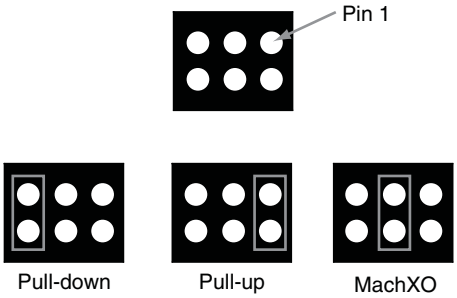
ispClock5610 Pin	MachXO Pin
CLK_OUT0	D7
CLK_OUT1	A9
CLK_OUT2	N9
CLK_OUT3	M9

See the ispClock5610 Family Data Sheet and the Lattice PAC-Designer® design software for information about programming the ispClock. More information and software downloads can be found on the Lattice web site at www.latticesemi.com/ispclock.

ispClock Configuration

The ispClock5610 has multiple configuration pins. The evaluation board includes a number of headers on the board allowing these configuration pins to be asserted, deasserted, or controlled from the MachXO. The headers have a general format as shown in Figure 7.

Figure 7. ispClock Configuration Headers



JP11 - JP17 configure all of the ispClock features. Table 11 shows which jumper block controls which ispClock pin. Refer to the ispClock5610 Family Data Sheet to understand what function each pin performs.

Table 11. ispClock5610 Clock Source

Jumper Block	IspClock Control	Factory Default Setting
JP11	PS0	5-6
JP12	PLL Bypass	5-6
JP13	OEx	5-6
JP14	GOE	5-6
JP15	SGATE	1-2
JP16	PS1	5-6
JP17	OEy	5-6

The ispClock has the ability to be programmed with four separate profiles. The profiles are selected using the PS1:0 input pins. The ispClock is programmed with a unique personality in profile 0. None of the remaining profiles provide additional frequencies.

Profile 0 is configured to use the ispClock PLL to generate several output frequencies from the base 33MHz input frequency. The outputs are:

- Output 0: 4x input
- Output 1: 2x input
- Output 2: 1x input
- Output 3: 0.5x input
- Output 4: 0.25x input

Some applications may not require the ispClock to use the PLL to generate higher frequency clocks. It is possible to turn the ispClock into a clock buffer chip. This is done by moving the PLL Bypass jumper from the default location. The PLL will no longer be included in the clock frequency generation. If Profile 0 is still selected the post PLL clock dividers will still be active, causing the output frequencies to drop dramatically. If a 1:1 input to output frequency ratio is desired the PS1:0 jumpers can be used to select any profile other than Profile 0.

RJ-45 Connection

The west edge of the board provides a place to insert an RJ-45 connector. This connector is not installed at the factory. The traces to the RJ-45 connector have the same resistor network scheme as shown in Figure 5, described above. The traces are 50 ohm impedance, and on larger MachXO devices are connected to true LVDS I/O.

Mictor Header

The left-side I/Os on the MachXO which are not used for the RJ-45 and small prototype test points are routed to a AMP/Tyco Mictor connector for additional off-board expansion. This connector can be mounted on the bottom side of the board. The connector is not populated by the manufacturer. Review the schematic for the board to determine which I/O pins are routed to the Mictor connector.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO 2280C Evaluation Board - Standard	LCMXO2280C-L-EV	
MachXO 640C Evaluation Board - Standard	LCMXO640C-L-EV	
ispLEVER Base with MachXO 2280 Standard Development Kit	LS-X2280-BASE-PC-N	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
June 2006	01.0	Initial release.
September2006	01.1	Updated schematic in Appendix A.
February 2007	01.2	Updated Switch Assignments table.
		Updated ispClock Configuration section.
March 2007	01.3	Added Ordering Information section.
April 2007	01.4	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.
June 2007	01.5	Updated Features bullets and General Description section to indicate the power supply will operate between 5V and 20V, instead of 5V to 28V.
March 2008	01.6	Changed document title from "MachXO Standard Evaluation Board Revision 001 User's Guide" to "MachXO Standard Evaluation Board Revision 001 & 002 User's Guide".

Appendix A. PCB Schematic

Figure 8. MachXO Control and Programming Interfaces

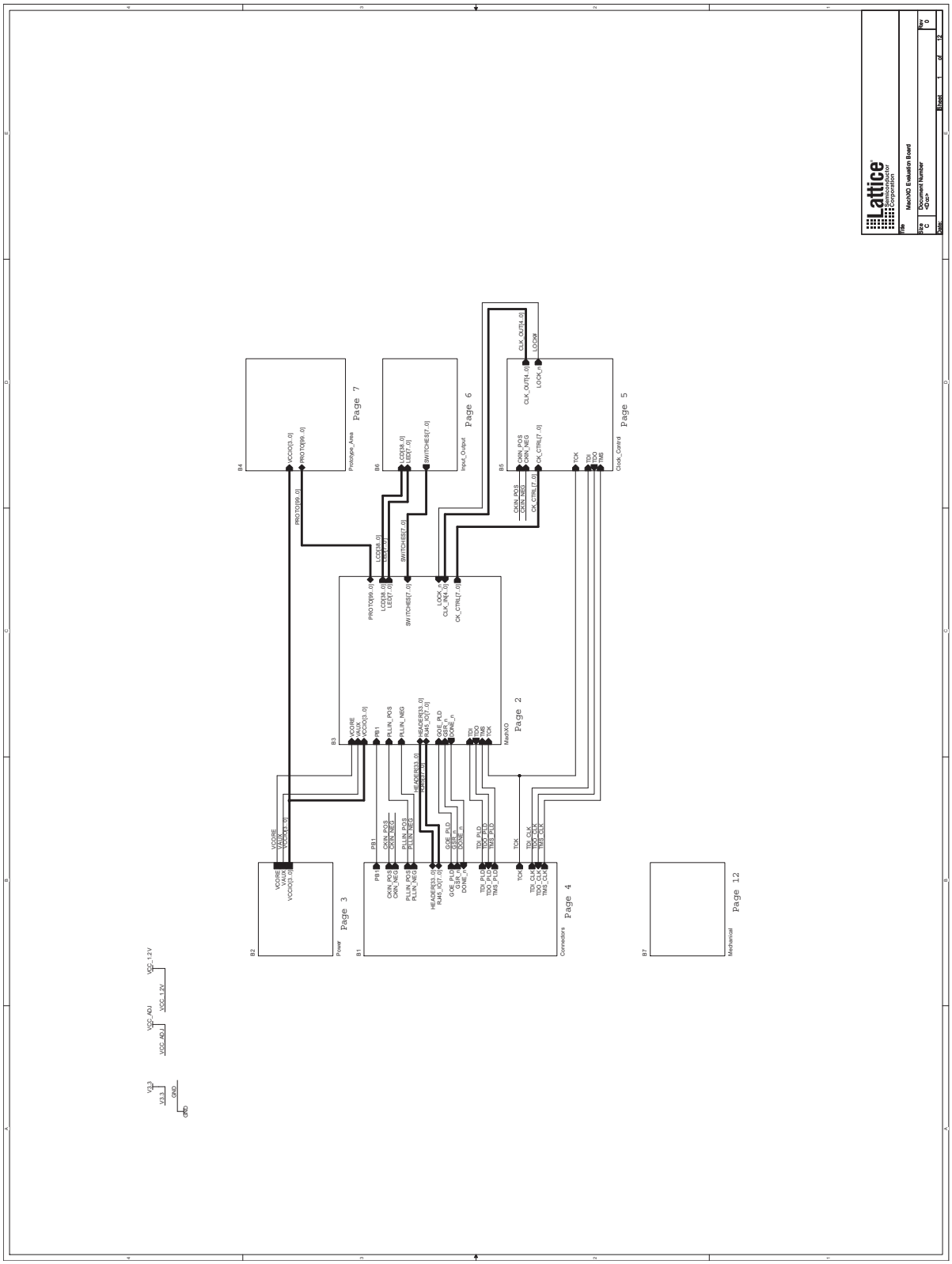


Figure 9. MachXO I/O Connections

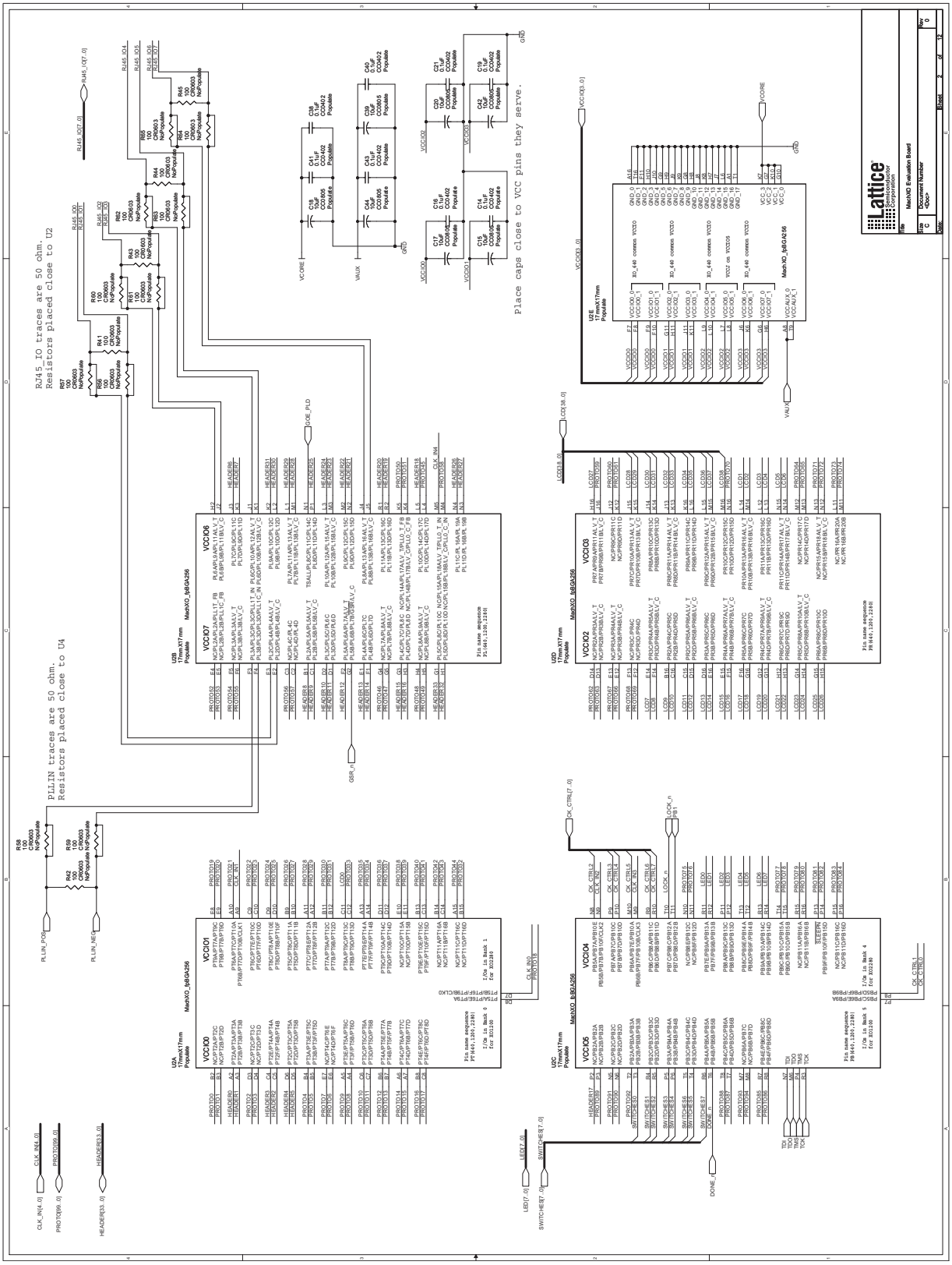


Figure 10. Power Section

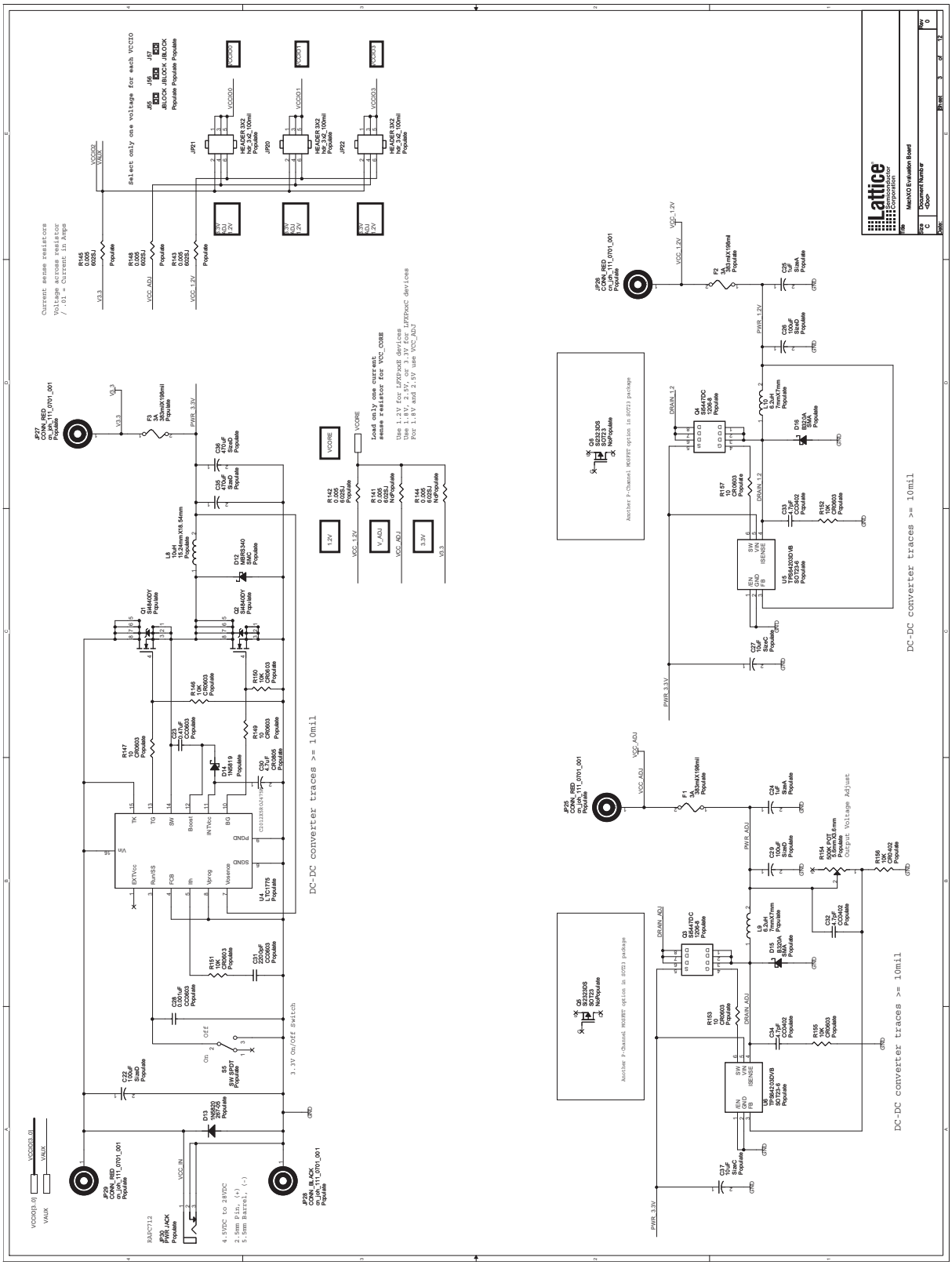


Figure 11. Miscellaneous Interfaces

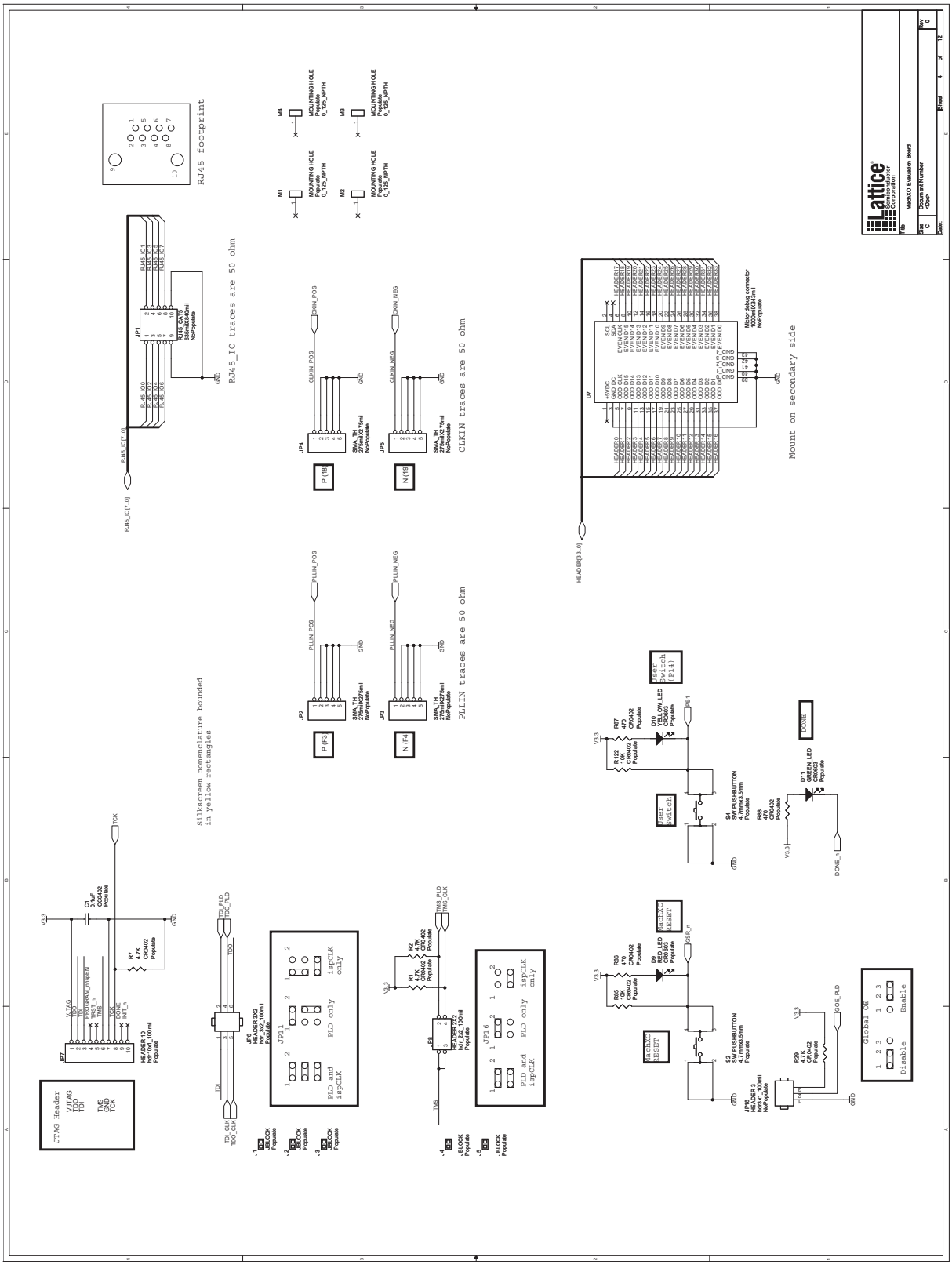


Figure 12. ispClock5610 Connections

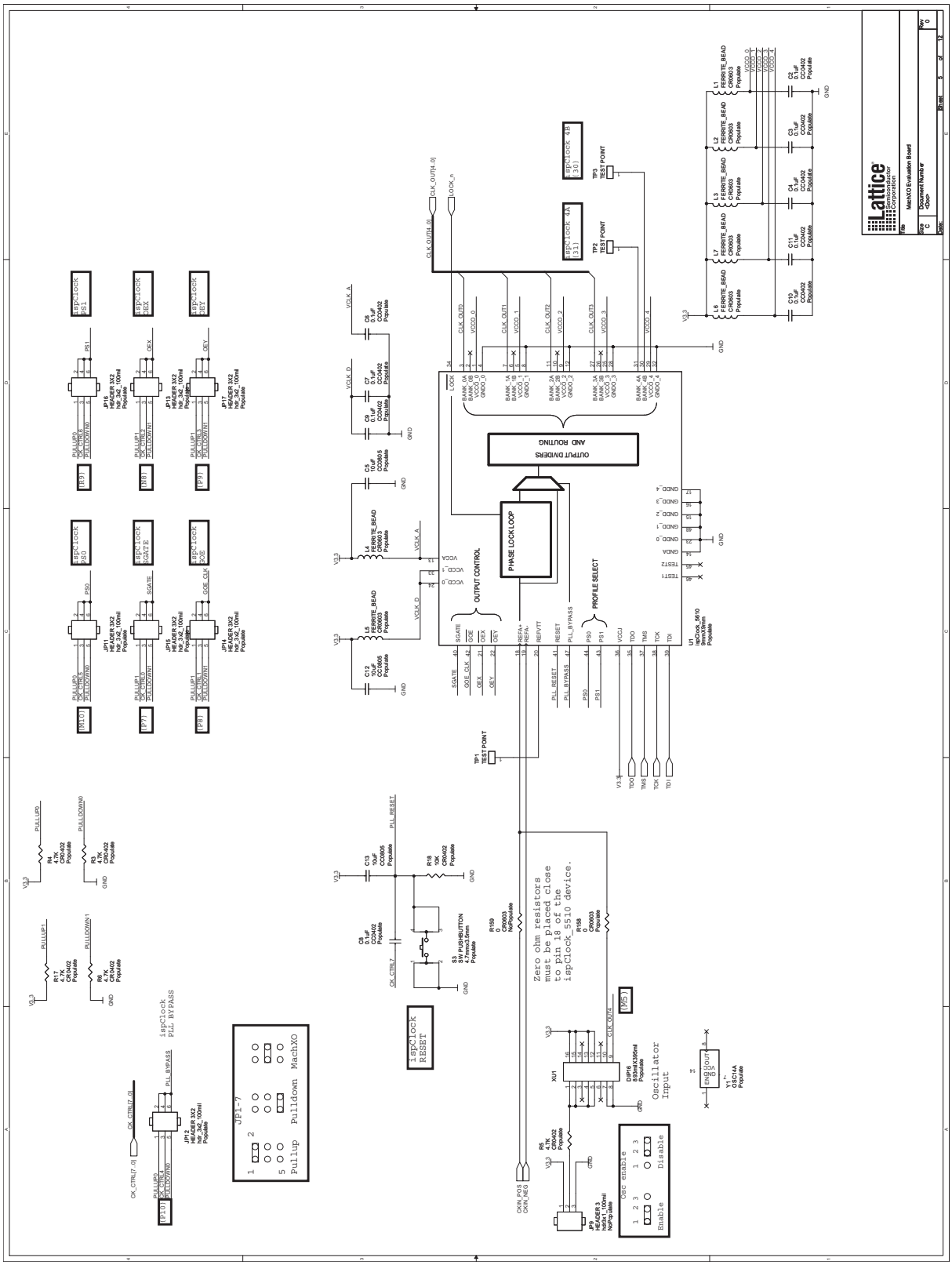


Figure 13. LED and LCD Connections

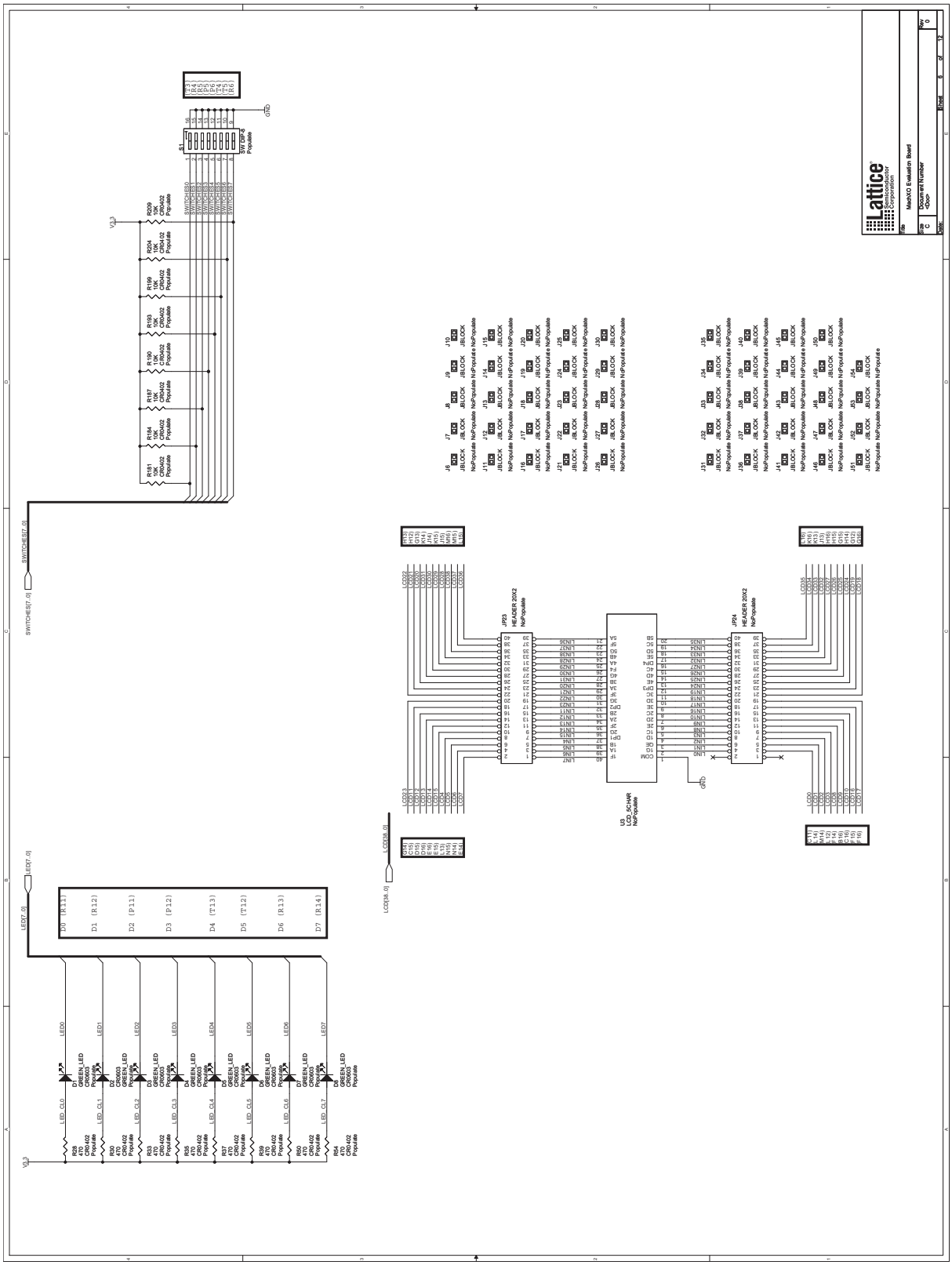


Figure 14. Miscellaneous

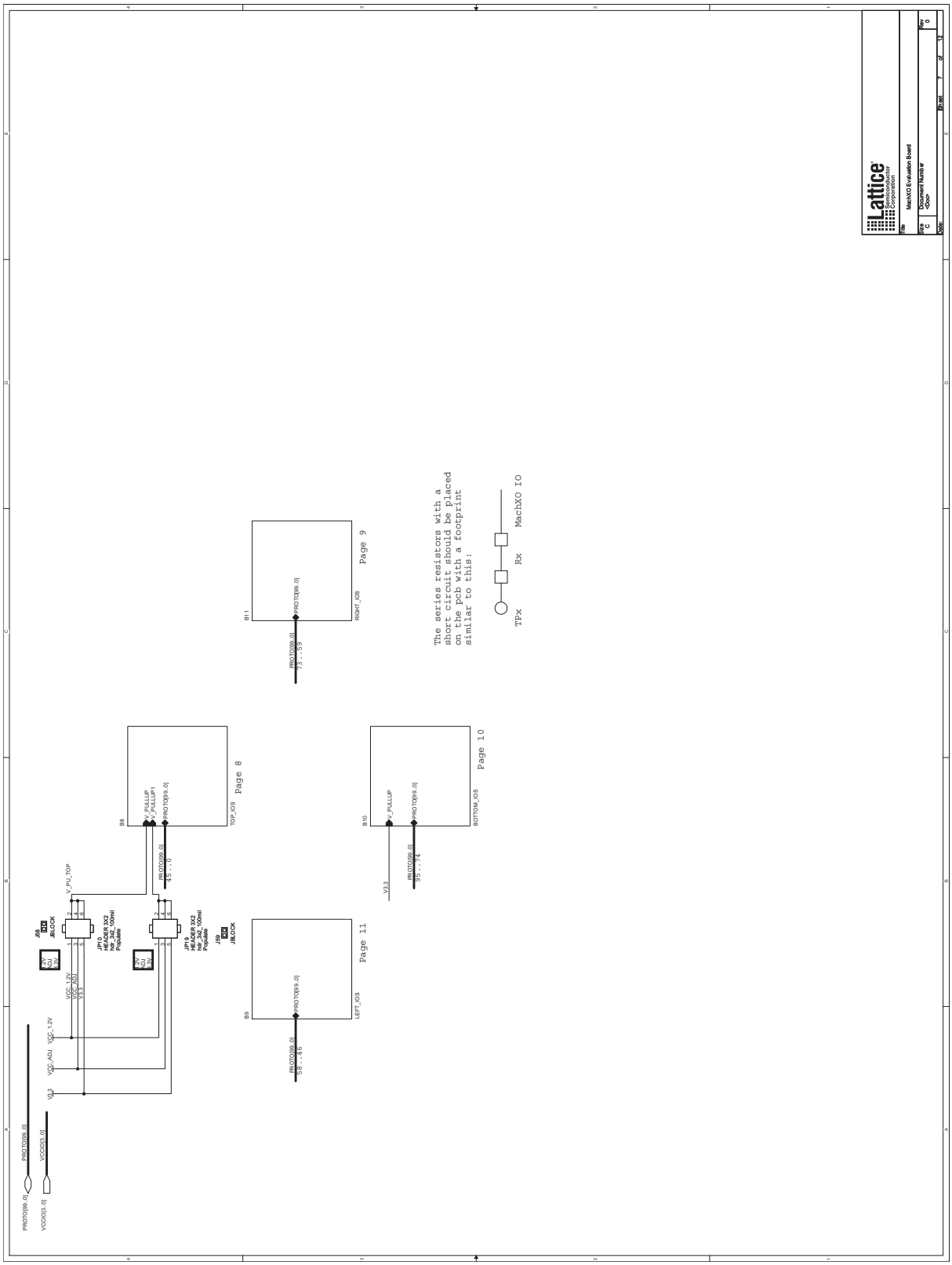


Figure 15. Prototype Area

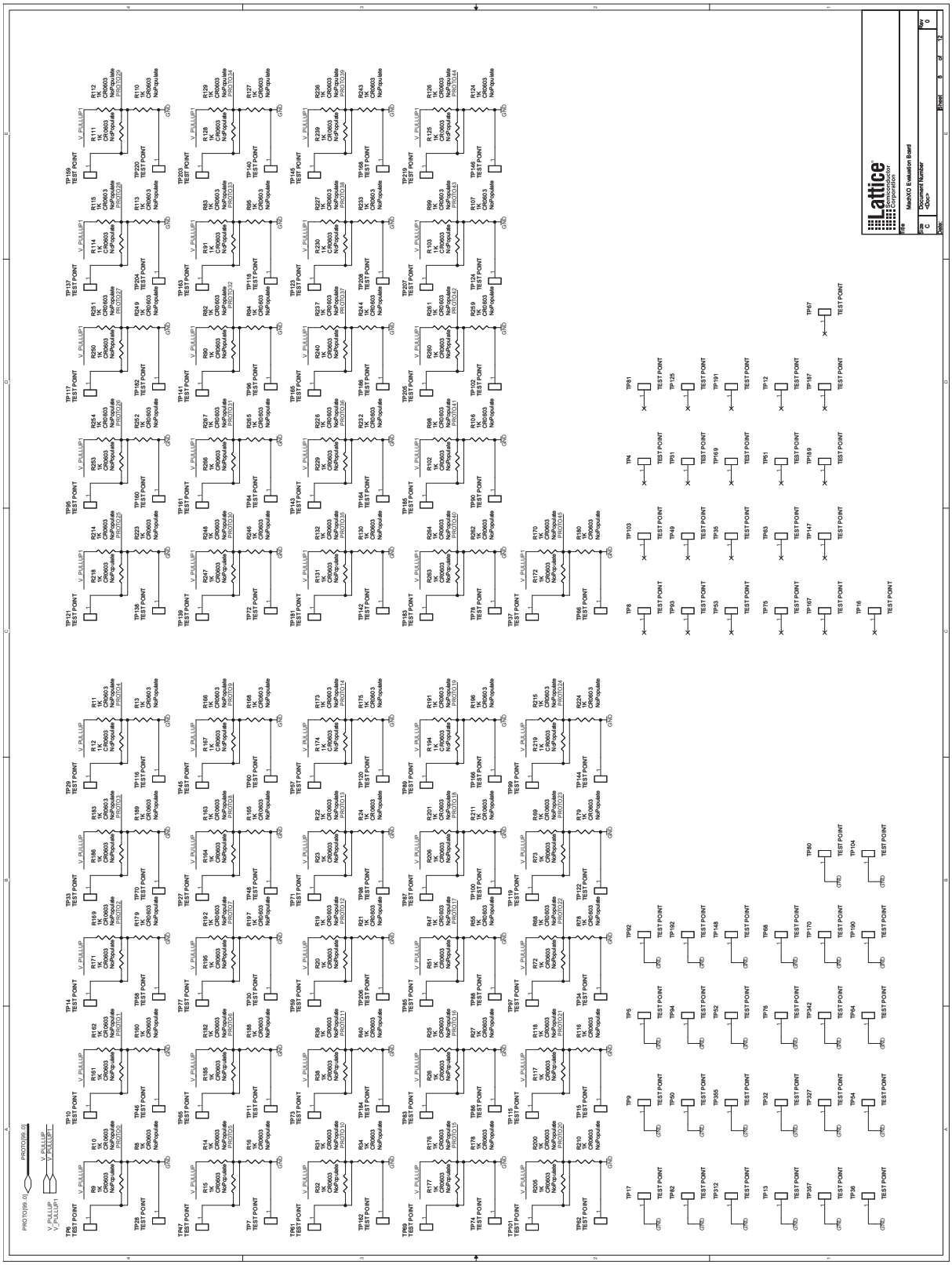


Figure 16. Prototype Area (Cont.)

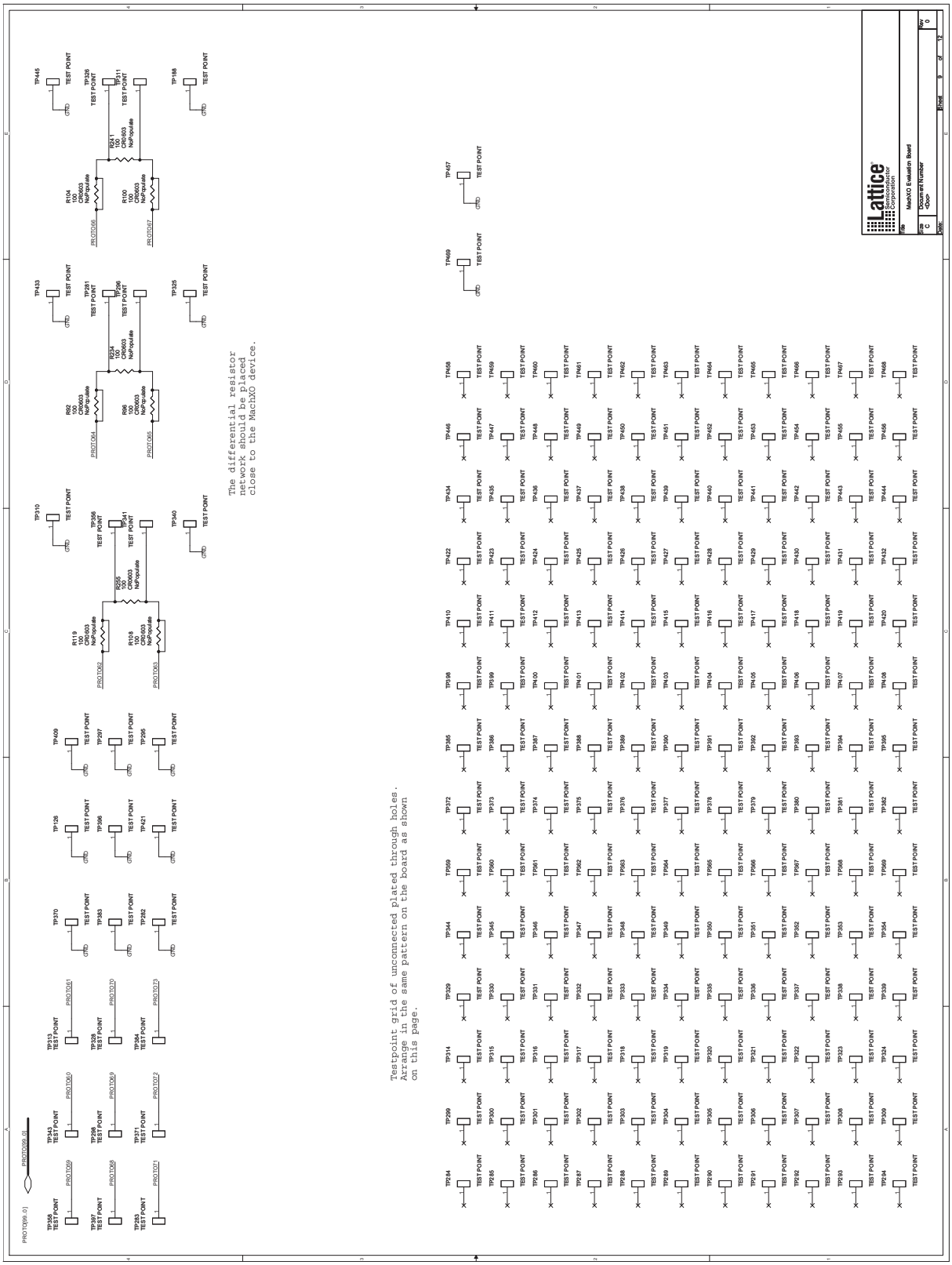


Figure 17. Prototype Area (Cont.)

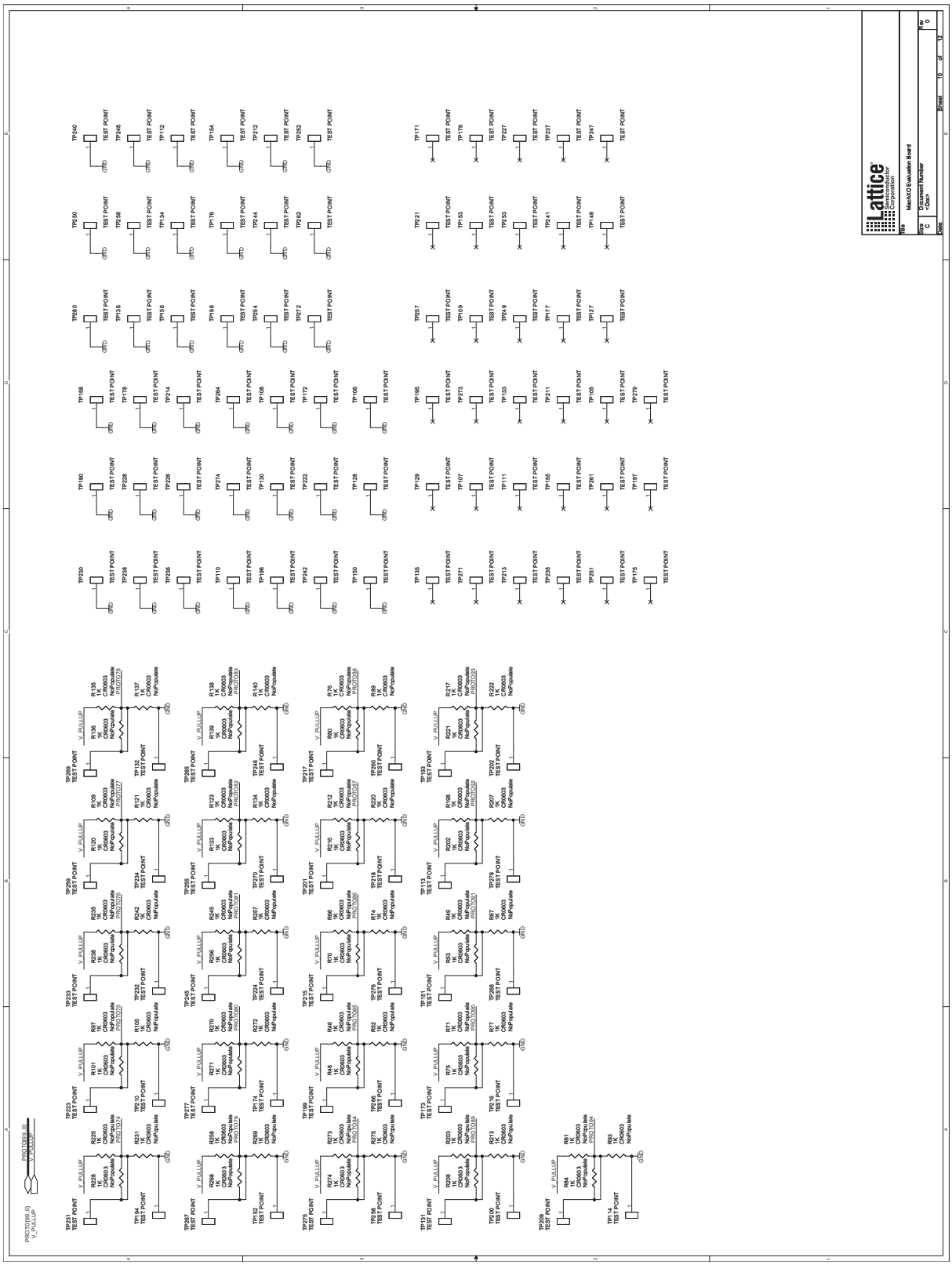


Figure 18. Prototype Area (Cont.)