PEMD48; PUMD48

NPN/PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

Rev. 05 — 13 April 2010 Product data sheet

1. Product profile

1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in small Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		Package configuration
	NXP	JEITA	
PEMD48	SOT666	-	ultra small and flat lead
PUMD48	SOT363	SC-88	very small

1.2 Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

1.3 Applications

- Low current peripheral driver
- Replacement of general-purpose transistors in digital applications
- Control IC inputs

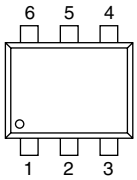
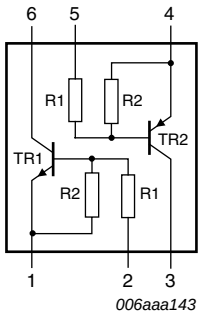
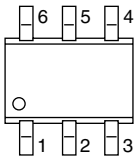
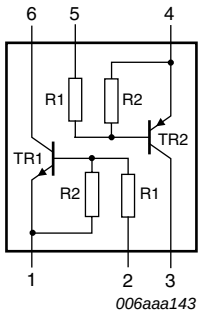
1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
Transistor TR1 (NPN)						
R1	bias resistor 1 (input)		33	47	61	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
Transistor TR2 (PNP)						
R1	bias resistor 1 (input)		1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		17	21	26	

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
PEMD48 (SOT666)			
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		
PUMD48 (SOT363)			
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PEMD48	-	plastic surface-mounted package; 6 leads	SOT666
PUMD48	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PEMD48	48
PUMD48	4*8

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage TR1					
	positive			-	+40	V
	negative			-	−10	V
	input voltage TR2					
	positive			-	+5	V
	negative			-	−12	V
I_O	output current			-	100	mA
I_{CM}	peak collector current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD48 (SOT666)		[1][2]	-	200	mW
	PUMD48 (SOT363)		[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD48 (SOT666)		[1][2]	-	300	mW
	PUMD48 (SOT363)		[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			−65	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25$ °C					
	PEMD48 (SOT666)		[1][2]	-	-	625	K/W
	PUMD48 (SOT363)		[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25$ °C					
	PEMD48 (SOT666)		[1][2]	-	-	416	K/W
	PUMD48 (SOT363)		[1]	-	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

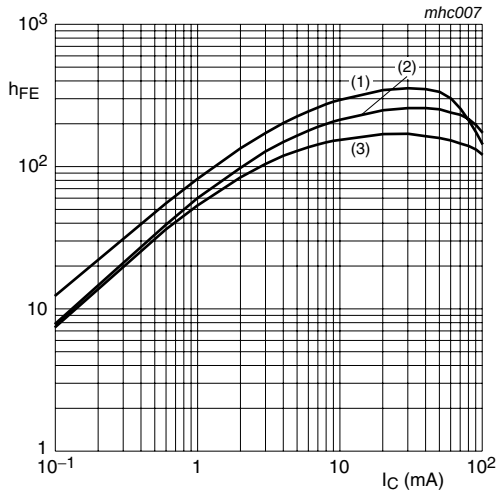
[2] Reflow soldering is the only recommended soldering method.

7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A	-	-	1	µA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C	-	-	50	µA
Transistor TR1 (NPN)						
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	-	-	90	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA	-	1.2	0.8	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 2 mA	3	1.6	-	V
R1	bias resistor 1 (input)		33	47	61	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz	-	-	2.5	pF
Transistor TR2 (PNP)						
I_{EBO}	emitter-base cut-off current	V_{EB} = −5 V; I_C = 0 A	-	-	−180	µA
h_{FE}	DC current gain	V_{CE} = −5 V; I_C = −10 mA	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = −5 mA; I_B = −0.25 mA	-	-	−100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = −5 V; I_C = −100 µA	-	−0.6	−0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = −0.3 V; I_C = −5 mA	−1.1	−0.75	-	V
R1	bias resistor 1 (input)		1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		17	21	26	
C_c	collector capacitance	V_{CB} = −10 V; I_E = i_e = 0 A; f = 1 MHz	-	-	3	pF



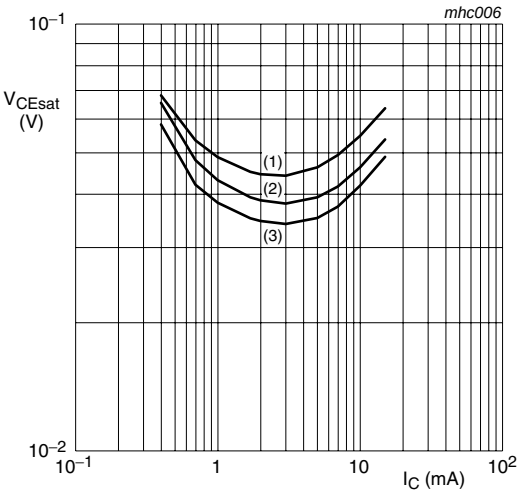
V_{CE} = 5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 1. TR1 (NPN): DC current gain as a function of collector current; typical values



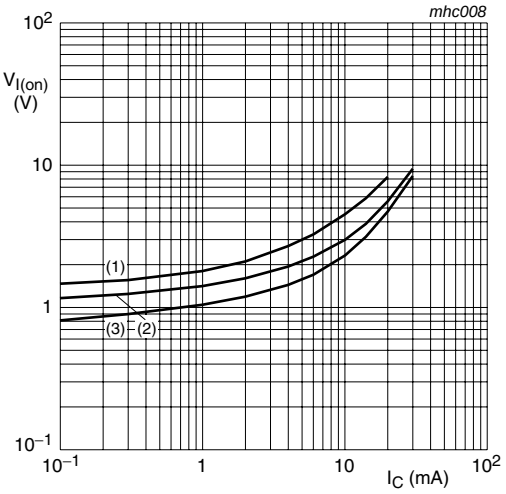
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 2. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



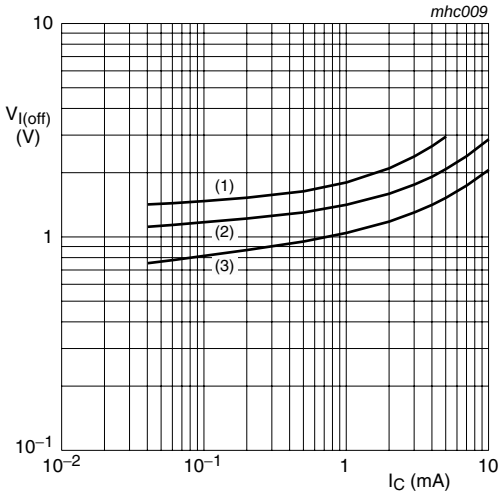
V_{CE} = 0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 3. TR1 (NPN): On-state input voltage as a function of collector current; typical values



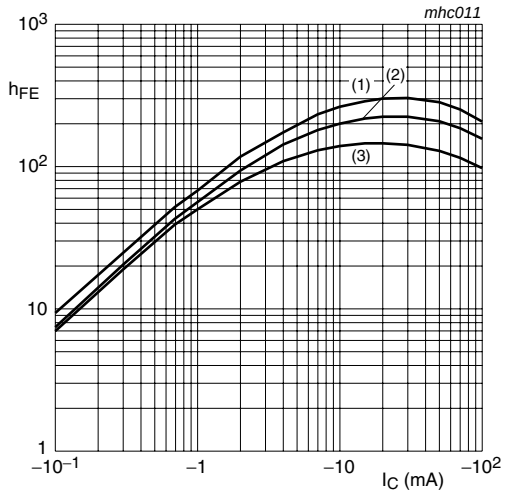
V_{CE} = 5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 4. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



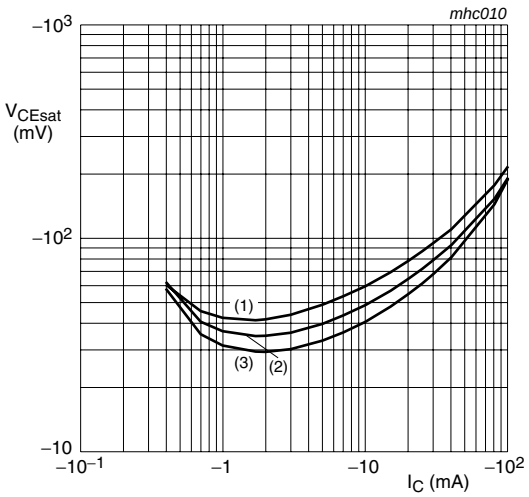
V_{CE} = −5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 5. TR2 (PNP): DC current gain as a function of collector current; typical values



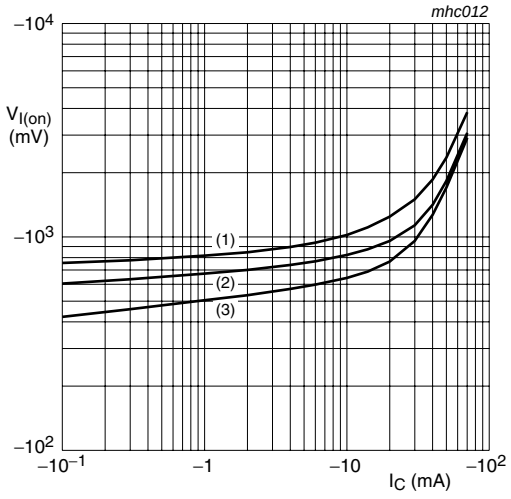
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 6. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



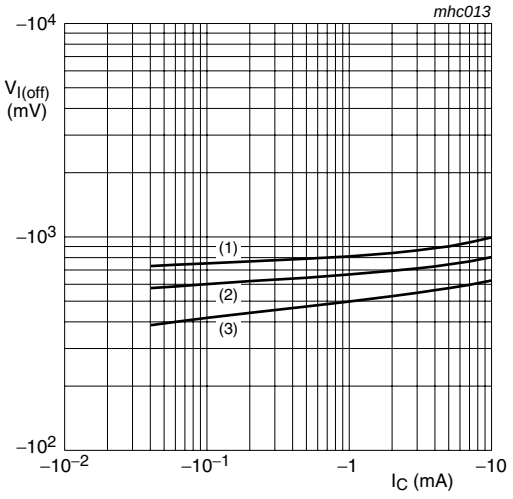
V_{CE} = −0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 7. TR2 (PNP): On-state input voltage as a function of collector current; typical values



V_{CE} = −5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 8. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

8. Package outline

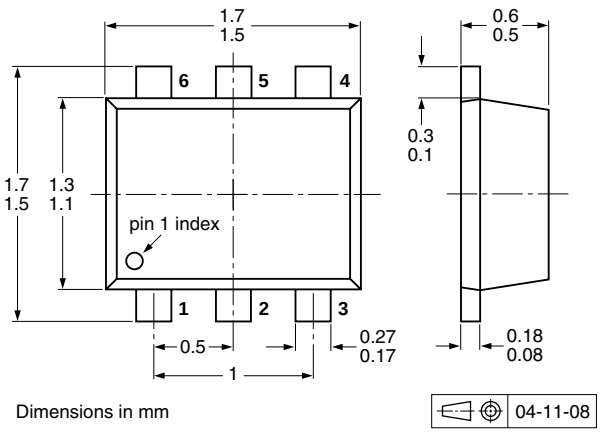


Fig 9. Package outline PEMD48 (SOT666)

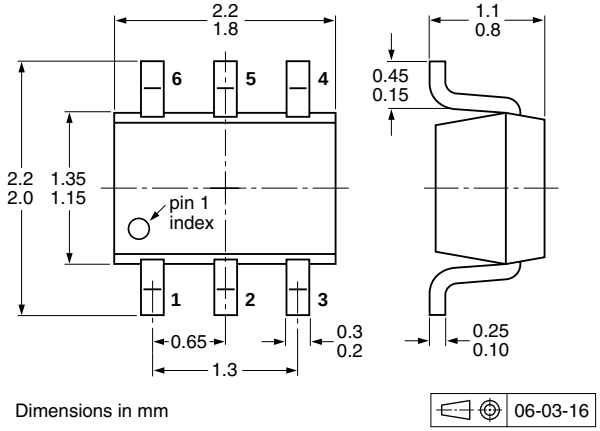


Fig 10. Package outline PUMD48 (SOT363)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMD48	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMD48	SOT363	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see Section 12.

[2] T1: normal taping

[3] T2: reverse taping

10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD48_PUMD48_5	20100413	Product data sheet	-	PEMD48_PUMD48_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 1 “Product profile”: amended • Table 3 “Pinning”: amended • Table 8 “Characteristics”: $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage and $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage • Figure 9 and 10: superseded by minimized package outline drawings • Section 9 “Packing information”: added • Section 11 “Legal information”: updated			
PEMD48_PUMD48_4	20040624	Product specification	-	PEMD48_PUMD48_3
PEMD48_PUMD48_3	20040602	Product specification	-	PEMD48_2 PUMD48_2
PUMD48_2	20010201	Product specification		PUMD48_1
PUMD48_1	19990422	Product specification		-
PEMD48_2	20011107	Product specification		PEMD48_1
PEMD48_1	20010924	Preliminary specification	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For more information, please visit: **http://www.nxp.com**

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13. Contents

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