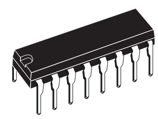
L6220

Quad Darlington switches

Features

- Four non inverting inputs with enable
- Output voltage up to 50 V
- Output current up to 1.8 A
- Very low saturation voltage
- TTL compatible inputs
- Integral fast recirculation diodes



Powerdip16 (12+2+2)

Description

The L6220 monolithic quad Darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common inhibit input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector Darlington transistor plus a fast diode for switching applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

The L6220 is mounted in a Powerdip 12 + 2 + 2 package.

Table 1. Order code

Order code	Package
E-L6220	Powerdip16

Figure 1. Block diagram

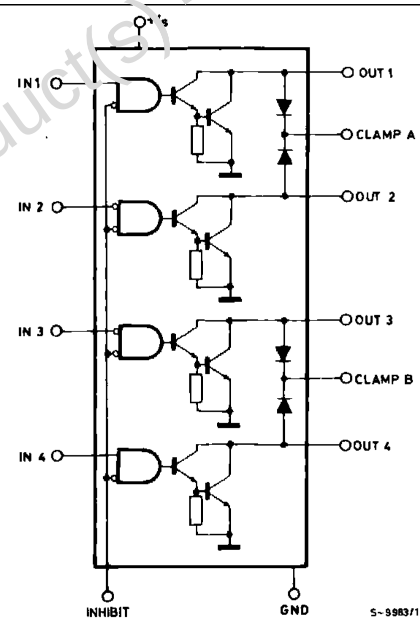


Table 2. **Pin description**

Pin N#	Pin name	Function
1	OUT 4	Output of driver 4
2	CLAMP B	Diode clamp to driver 3 and driver 4
3	OUT 3	Output of driver 3
4, 5, 12, 13	GND	Common ground
6	OUT 2	Output of driver 2
7	CLAMP A	Diode clamp to driver 1 and driver 2
8	OUT 1	Output of driver 1
9	IN 1	Input to driver 1
10	IN 2	Input to driver 2
11	V_S	Logic supply voltage
14	INHIBIT	Inhibit input to all drivers
15	IN 3	Input to driver 3
16	IN 4	Input to driver 4

Figure 2. **Pin connections**

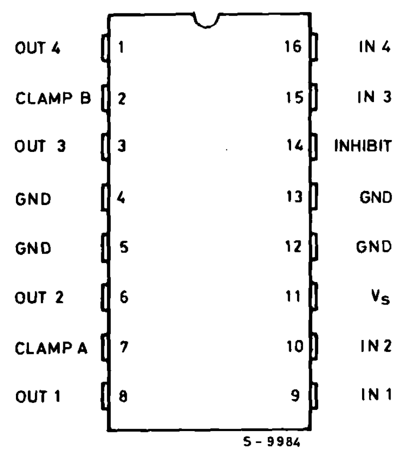


Table 3. **Truth table**

Enable	Inputs 1, 4	Power out	Enable	Inputs 2, 3	Power out
L	H	ON	L	L	ON
L	L	OFF	L	H	OFF
H	X	OFF	H	X	OFF

For each input : H = High level

L = Low level

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_o	Output voltage	50	V
V_s	Logic supply voltage	7	V
V_{IN}, V_{EN}	Input voltage, enable voltage	V_S	
I_C	Continuous collector current (for each channel)	1.8	A
I_C	Collector peak current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector peak current (non repetitive, t = 10 µ s)	3.2	A
T_{op}	Operating temperature range (junction)	– 40 to + 150	°C
T_{stg}	Storage temperature range	– 55 to + 150	°C
I_{sub}	Output substrate current	350	mA
P_{tot}	Total power dissipation at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient max.	80	°C/W

Table 6. Electrical characteristics

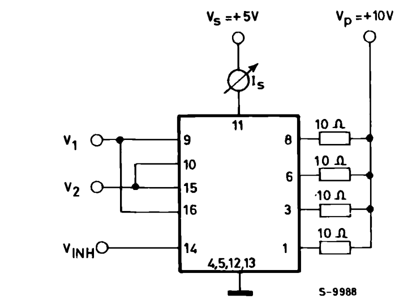
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Logic supply voltage		4.5		5.5	V
I_s	Logic supply current	All outputs ON, I_C = 0.7 A			20	mA
		All outputs OFF			20	mA
$V_{CE(sus)}$	Output sustaining voltage	I_C = 100 mA, $V_{IN} = V_{IN}H$	46			V
I_{CEX}	Output leakage current	V_{CE} = 50 V, $V_{IN\ 1.4} = V_{IN}H$			1	mA
$V_{CE(sat)}$	Collector emitter saturation voltage (one input on ; all others inputs off.)	V_s = 4.5 V $V_{IN\ 2.3} = V_{IN}L$, $V_{INH} = V_{INH}L$ I_C = 0.6 A I_C = 1 A I_C = 1.8 A			1 1.2 1.6	V
$V_{IN}L$, $V_{INH}L$	Input low voltage				0.8	V
$I_{IN}L$, $I_{INH}L$	Input low current	$V_{IN} = V_{INL}$, $V_{EN} = V_{ENL}$			- 100	µA
$V_{IN}H$, $V_{INH}H$	Input high voltage		2.0			V
$I_{IN}H$, $I_{INH}H$	Input high current	$V_{IN} = V_{IN}H$, $V_{INH} = V_{INH}H$			±10	µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_R	Clamp diode leakage current	V_R = 50 V, V_{INH} = V_{INH}H			100	µA
V_F	Clamp diode forward voltage	I_F = 1 A I_F = 1.8 A			1.6 2.0	V V
$t_{d\ (on)}$	Turn on delay time	V_p = 5 V, R_L = 10 Ω			2	µs
$t_{d\ (off)}$	Turn off delay time	V_p = 5 V, R_L = 10 Ω			5	µs
ΔI_s	Logic supply current variation	V_{IN} = 5 V, V_{EN} = 5 V I_{out} = – 300 mA for each channel			120	mA

1 Test circuits

Figure 3. Logic supply current



Set V_1 = 4.5 V, V_2 = 0.8 V, V_{INH} = 4.5 V or V_1 = 0.8 V, V_2 = 4.5 V, V_{INH} = 0.8 V for I_S (all outputs off)

Set V_1 = 2 V, V_2 = 0.8 V, V_{IN} = 0.8 V for I_S (all outputs on)

Figure 4. Output sustaining voltage

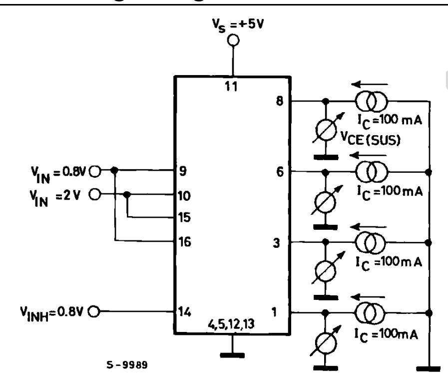


Figure 5. Output leakage current

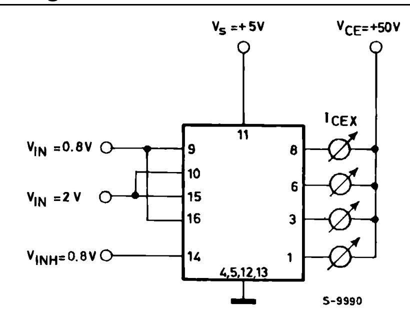


Figure 6. Collector-emitter saturation voltage

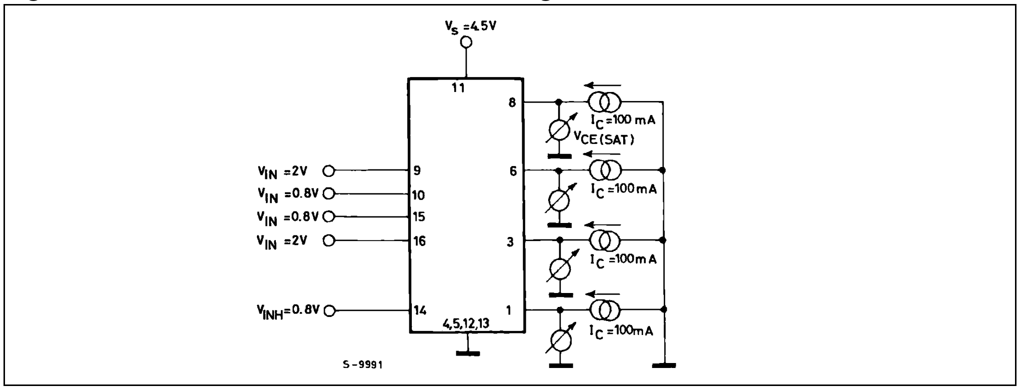
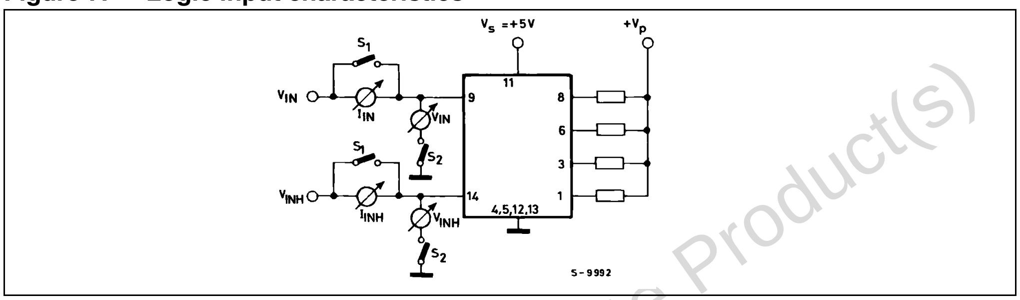


Figure 7. Logic input characteristics



Set S_1, S_2 open, V_{IN}, V_{INH} = 0.8 V for I_{IN} L, I_{INH} L

Set S_1, S_2 open, V_{IN}, V_{INH} = 2 V for I_{IN} H, I_{INH} H

Set S_1, S_2 close, V_{IN}, V_{INH} = 0.8 V for V_{IN} L, V_{INH} L

Set S_1, S_2 close, V_{IN}, V_{INH} = 2 V for V_{IN} H, V_{INH} H

Figure 8. Clamp diode leakage current.

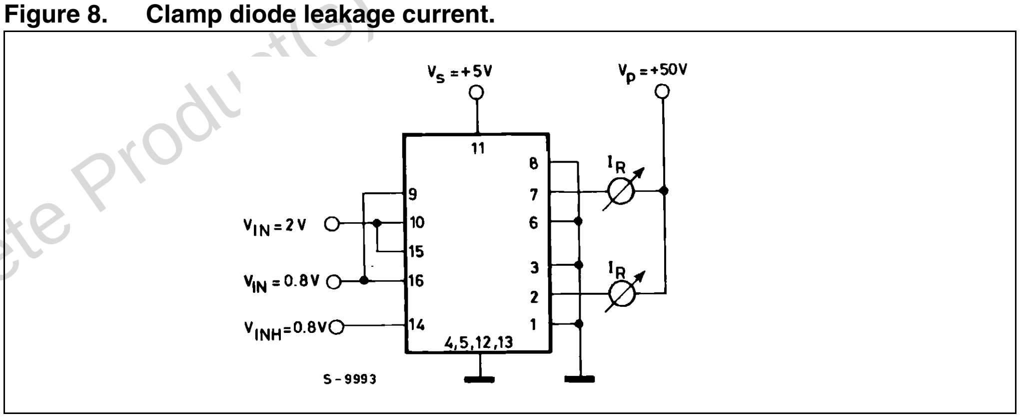


Figure 9. Clamp diode forward voltage

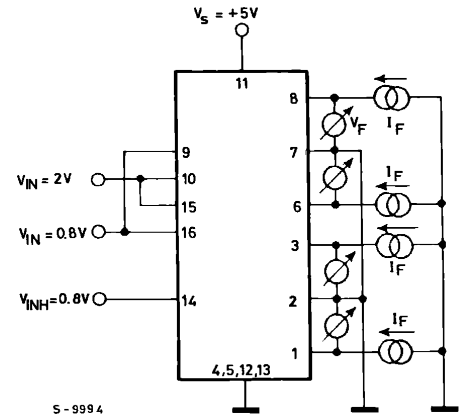


Figure 10. Switching times test circuit

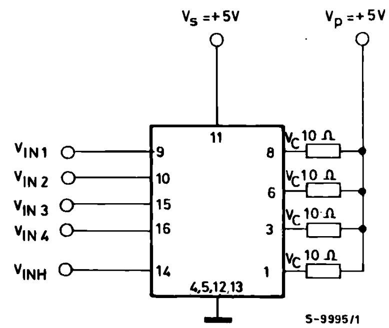


Figure 11. Switching times waveforms

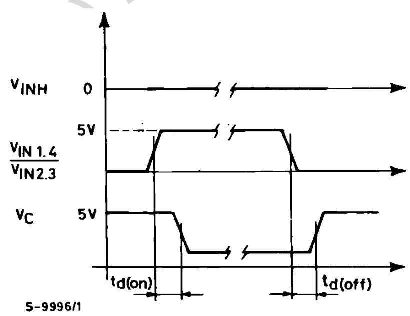


Figure 12. Collector saturation voltage versus collector current

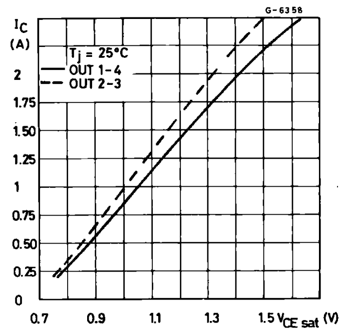


Figure 13. Free-wheeling diode forward voltage versus diode current

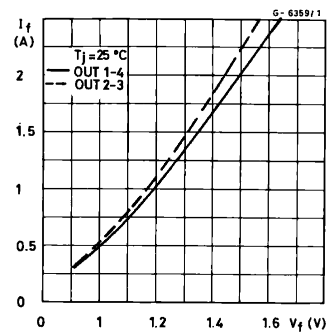


Figure 14. Collector saturation voltage versus junction temperature at IC = 1 A

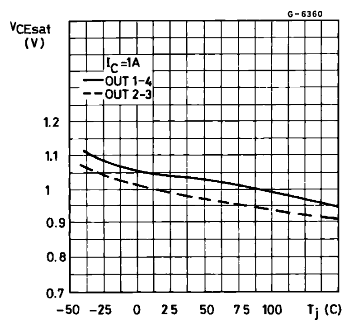


Figure 15. Free-wheeling diode forward voltage versus junction temperature at IF = 1 A

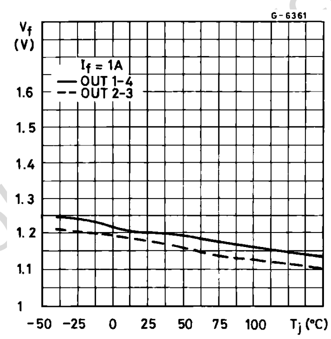


Figure 16. Collector saturation voltage versus junction temperature at IC = 8 A

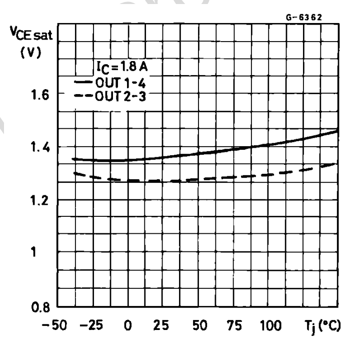
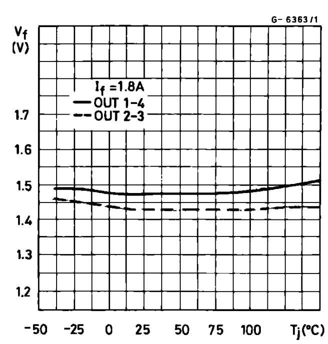


Figure 17. Free-wheeling diode forward voltage versus junction temperature at IF = 1 A



2 Application information

When inductive loads are driven by L6220, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay *Figure 18*.

Figure 18. Inductive load driver

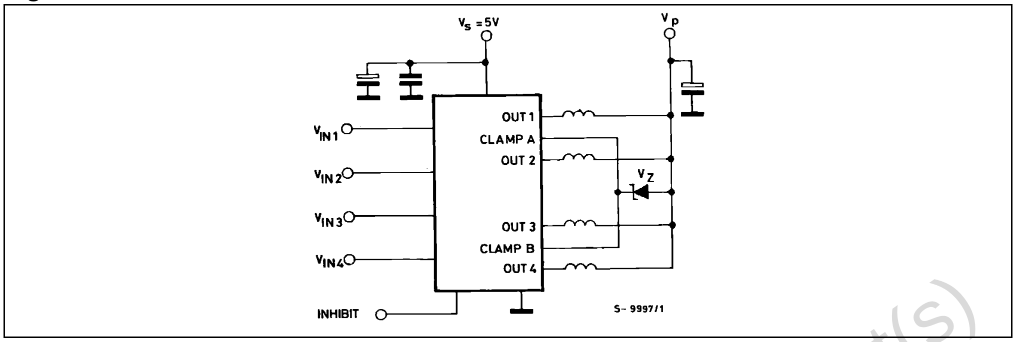
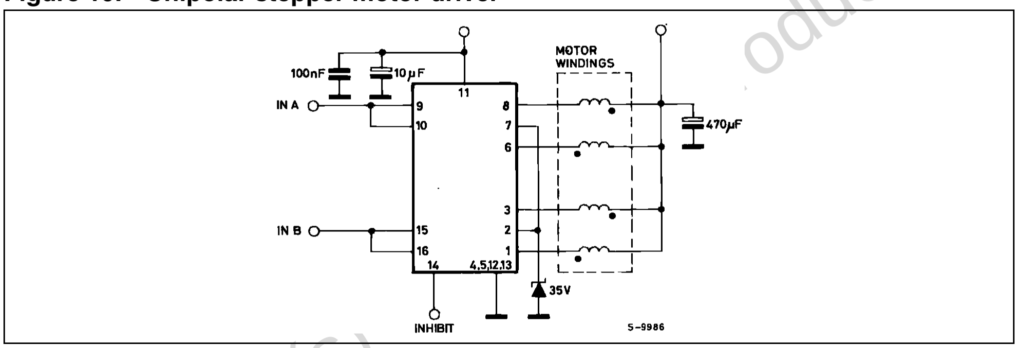


Figure 19. Unipolar stepper motor driver



For reliability it is suggested that the zener is chosen so that $V_p + V_z < 35$ V.

The reasons for this are two-fold :

1. The zener voltage changes in temperature and current.
2. The instantaneous power must be limited to avoid the reverse second breakdown.

The particular internal logic allows an easier full step driving using only two input signals.

Figure 20. Full step driving

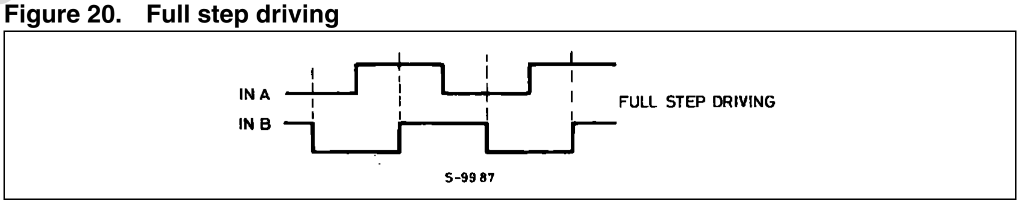
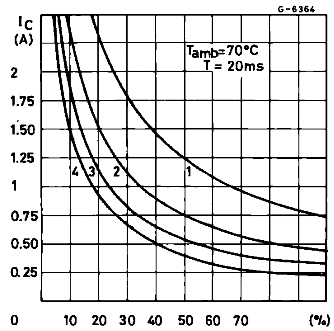


Figure 21. Allowed peak collector-current versus duty cycle for 1, 2, 3 or 4 simultaneously working outputs (L6220)



3 Mounting instructions

The Rth j-amb of the L6220 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (*Figure 22*) or to an external heatsink (*Figure 23*).

The diagram of *Figure 24* shows the maximum dis-sipable power Ptot and the Rth j-amb as a function of the side " a" of two equal square copper areas having a thickness of 35µ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 22. Example of P.C. board copper area which is used as heatsink

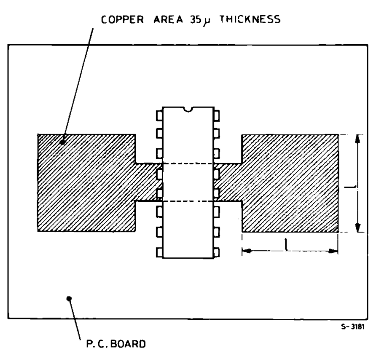


Figure 23. External heatsink mounting example

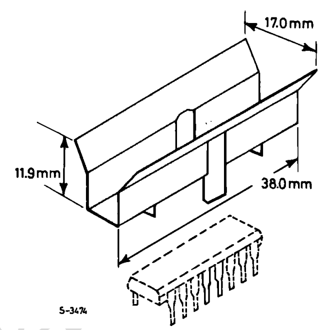


Figure 24. Maximum dissipable power and junction to ambient thermal resistance versus side "α"

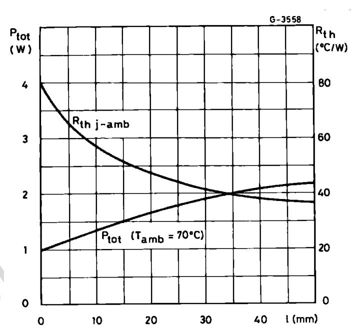


Figure 25. Maximum allowable power dissipation versus ambient temperature

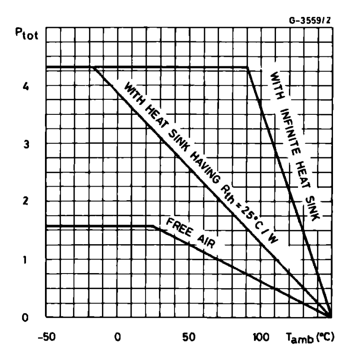
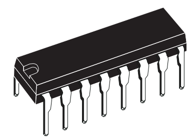


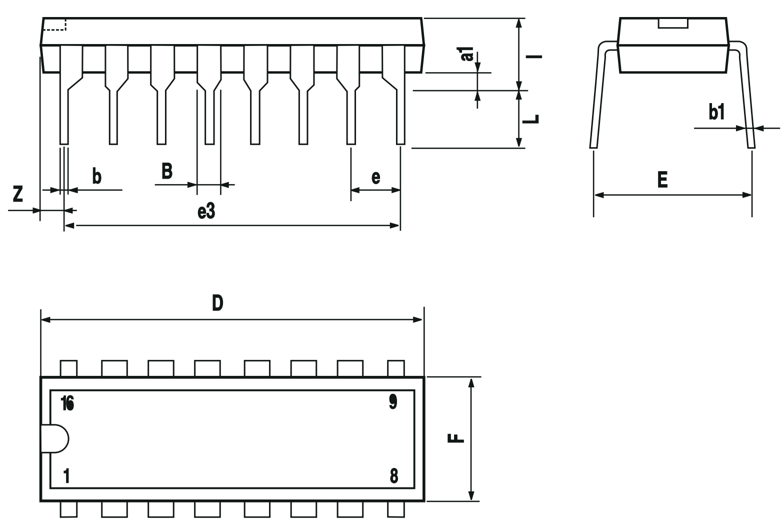
Figure 26. DIP16 mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



DIP16



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4 Revision history

Table 7. Document revision history

Date	Revision	Description of changes
01-Sep-2003	1	First issue
01-Jul-2004	2	Cancelled the L6220N part number and the relative references. Changed the style-look following the new “Corporate Technical Pubblications Design Guide” rules.
01-Jun-2010	3	Changed the order code to E-L6220 on page 1.

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