HV450

# **High-Voltage Ring Generator**

#### **Ordering Information**

Operating Voltage	Package Options			
V <sub>NN1</sub>	SOW-16			
-220V	HV450WG			

#### **Features**

- Integrated high voltage transistors
- 67V<sub>RMS</sub> ring signal
- Output over current protection
- Can drive external MOSFETs for larger loads

Absolute Maximum Ratings\*

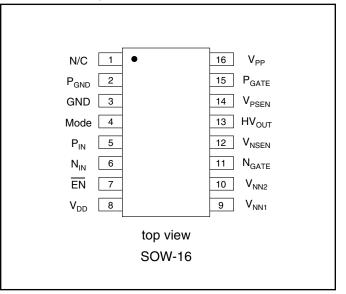
## Applications

- High voltage ring generator
- □ Set-top/Street box ring generator
- D Pair gain ring generator

# General Description

The Supertex HV450 is a PWM high voltage ring generator. The high voltage output P- and N-channel transistors are controlled independently by the logic inputs  $P_{IN}$  and  $N_{IN}$ . For application where a single control pin  $(N_{IN})$  is desired, the mode pin should be connected to Gnd. This adds a 200ns deadband on the control logic to avoid cross conduction on the high voltage output. A logic high on  $N_{IN}$  will turn the high voltage P-Channel on and the N-Channel off. The outputs can drive up to 5 RENs. The HV450 can drive external MOSFETs for applications requiring larger loads. The IC can be powered down by connecting the enable pin to  $V_{DD}$ . The high voltage outputs have pulse by pulse over current protection.

#### **Pin Configuration**



\* All voltages referenced to ground

V<sub>NN1</sub>, power supply voltage

V<sub>DD</sub>, logic supply

Power dissipation

Storage temperature

V<sub>PP</sub>, P-channel gate voltage supply

V<sub>NN2</sub>, N-channel gate voltage supply

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-240V

-20V

+7.5V

600mW

V<sub>NN1</sub>+20V

-65°C to +150°C

### **Electrical Characteristics**

(Over operating supply voltages unless otherwise specified,  $T_A = -40^{\circ}C$  to +85°C.)

Symbol	Parameters	Min	Тур	Max	Unit	Conditions
V <sub>PP</sub>	P-channel linear regulator output voltage	-10		-18	V	
V <sub>NN1</sub>	High voltage negative supply	- 220		-110	V	
V <sub>NN2</sub>	Negative linear regulator output voltage	V <sub>NN1</sub> + 6.0		V <sub>NN1</sub> + 10.0	V	
V <sub>DD</sub>	Logic supply voltage	4.5		5.5	V	
I <sub>NN1Q</sub>	V <sub>NN1</sub> quiescent current		300	500	μA	$P_{IN} = N_{IN} = \overline{EN} = L$
				25	μΑ	$P_{IN} = N_{IN} = L, \overline{EN} = H$
I <sub>DDQ</sub>	V <sub>DD1</sub> quiescent current		90	200	μΑ	$P_{IN} = N_{IN} = \overline{EN} = L$
			35	100		$P_{IN} = N_{IN} = L, \overline{EN} = H$
I <sub>NN1</sub>	V <sub>NN1</sub> operating current		1.4		mA	No load, $V_{\text{OUTP}}$ and $V_{\text{OUTN}}$ switching at 100KHz
I <sub>DD</sub>	V <sub>DD</sub> operating current			1.0	mA	
I	Mode logic input low current		25		μΑ	Mode = 0V
V <sub>IL</sub>	Logic input low voltage	0		1.0	V	$V_{DD} = 5.0 V$
V <sub>IH</sub>	Logic input high voltage	4.0		5.0	V	$V_{DD} = 5.0 V$

#### **High Voltage Output**

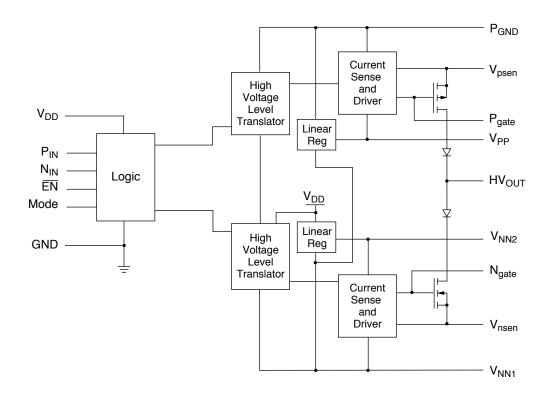
Symbol	Parameters	Min	Тур	Max	Unit	Conditions
R <sub>SOURCE</sub>	V <sub>OUT</sub> P source resistance		65		Ω	I <sub>OUT</sub> = 100mA
R <sub>SINK</sub>	V <sub>OUT</sub> P sink resistance		65		Ω	I <sub>OUT</sub> = -100mA
t <sub>d(ON)</sub>	HV <sub>OUT</sub> delay time		150		ns	$P_{IN}$ = high to low, Mode = high
t <sub>rise</sub>	HV <sub>OUT</sub> rise time		50		ns	P <sub>IN</sub> = high to low
t <sub>d(OFF)</sub>	HV <sub>OUT</sub> delay time		200		ns	$N_{IN}$ = low to high, Mode = high
t <sub>fall</sub>	HV <sub>OUT</sub> fall time		50		ns	N <sub>IN</sub> = low to high
t <sub>db</sub>	Logic deadband time		250		ns	Mode = low
V <sub>psen</sub>	HV <sub>OUT</sub> current source sense voltage	-1.2		-0.8	V	
V <sub>nsen</sub>	HV <sub>OUT</sub> current sink sense voltage	V <sub>NN1</sub> + 0.8		V <sub>NN1</sub> + 1.2	V	
t <sub>shortP</sub>	HV <sub>OUT</sub> off delay time when current source sense is activiated		70	150	ns	
t <sub>shortN</sub>	HV <sub>OUT</sub> off delay time when current sink sense is activated		70	150	ns	
t <sub>whout</sub>	Minimum pulse width for $HV_{OUT}$ at $P_{GND}$			500	ns	
t <sub>wlout</sub>	Minimum pulse width for $\mathrm{HV}_{\mathrm{OUT}}$ at $\mathrm{V}_{\mathrm{NN1}}$			500	ns	

#### **Truth Table**

N <sub>IN</sub>	P <sub>IN</sub>	Mode	ĒN	HV <sub>OUT</sub>
L	L	Н	L	Pgnd
L	н	Н	L	High Z
H*	L*	Н	L	*
Н	Н	Н	L	V <sub>NN1</sub>
L	Х	L	L	V <sub>NN1</sub>
н	Х	L	L	Pgnd
Х	Х	Х	Н	High Z

\*This state will short  $V_{_{\!N\!N\!1}}$  to Pgnd and should therefore be avoided.

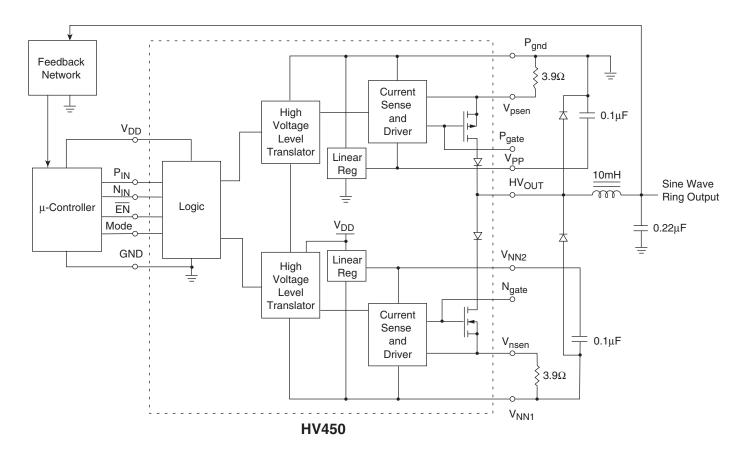
#### **Block Diagram**



#### **Pin Description**

V <sub>PP</sub>	P-channel gate voltage supply. Generated by an internal linear regulator. A $0.1\mu$ F capacitor should be connected between $P_{GND}$ and $V_{PP}$ .
V <sub>NN1</sub>	Negative high voltage supply.
V <sub>NN2</sub>	N-channel gate voltage supply. Generated by an internal linear regulator. A 0.1 $\mu$ F capacitor should be connected between V <sub>NN2</sub> and V <sub>NN1</sub> .
V <sub>DD</sub>	Logic supply voltage.
GND	Low voltage ground.
P <sub>GND</sub>	High voltage power ground.
P <sub>IN</sub>	Logic control input. When mode is high, logic input high turns OFF output high voltage P-Channel.
N <sub>IN</sub>	Logic control input. When mode is high, logic input high turns ON output high voltage N-Channel.
EN	Logic enable input. Logic low enables IC.
Mode	Logic mode input. Logic low activates 200nsec deadband. When mode is low, $N_{IN}$ turns on and off the high voltage N- and P-Channels. Pin is not used and should be connected to $V_{DD}$ or ground.
ΗV <sub>OUT</sub>	High voltage output. Voltage swings from P <sub>GND</sub> to V <sub>NN1</sub> .
V <sub>psen</sub>	Pulse by pulse over current sensing for P-Channel MOSFET.
V <sub>nsen</sub>	Pulse by pulse over current sensing for N-Channel MOSFET.
P <sub>gate</sub>	Gate drive for external P-channel MOSFET.
N <sub>gate</sub>	Gate drive for external N-channel MOSFET.

# **Typical Application Circuit**





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