

AVR- M32 development board

Users Manual



Rev. C, January 2005 Copyright(c) 2009, OLIMEX Ltd, All rights reserved

INTRODUCTION

AVR-M32 is header board with JTAG connector and Atmega32 – 8-bit Microcontroller with 16K Bytes In-System Programmable Flash.

BOARD FEATURES

- JTAG 5x2 pin connector for in-circuit programming and debugging with AVR-JTAG-L or AVR-JTAG-USB
- pin to pin compatible to AT90S8535 and may be used with AVR-P40B-8535xMhz prototype boards
- ATMega32-16AC avr microcontroller
- power supply filtering capacitors
- extension pin headers for each uC pin
- FR-4, 1.5 mm (0,062"), green soldermask, white silkscreen component print
- dimensions 51x19 mm (2"x0.73")

ELECTROSTATIC WARNING

The AVR-M32 board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

BOARD USE REQUIREMENTS

Cables: The cable you will need depends on the programmer/debugger you use. If you use AVR-JTAG you will need RS232, if you use AVR-USB-JTAG you will need 1.8 m A-B USB cable.

Hardware: One of OLIMEX Programmers/Debuggers – <u>AVR-JTAG</u>, <u>AVR-USB-JTAG</u>, or other compatible Programmer/Debugger.

Software: AVR C compiler.

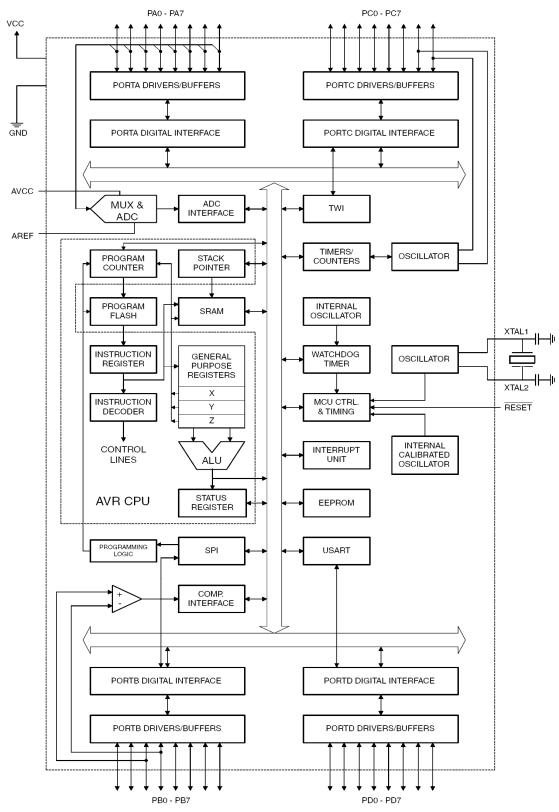
PROCESSOR FEATURES

AVR-M32 board use High-performance, Low-power AVR® 8-bit Microcontroller

- ATmega32 from Atmel Corporation with these features:
- Advanced RISC Architecture
 - 131 Powerful Instructions Most Single-clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 16 MIPS Throughput at 16 MHz
 - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
 - 32K Bytes of In-System Self-programmable Flash program memory
 - 1024 Bytes EEPROM
 - 2K Byte Internal SRAM
 - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
 - Data retention: 20 years at 85°C/100 years at 25°C
 - Optional Boot Code Section with Independent Lock Bits
 In-System Programming by On-chip Boot Program
 True Read-While-Write Operation
 - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
 - Boundary-scan Capabilities According to the JTAG Standard
 - Extensive On-chip Debug Support
 - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
 - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
 - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
 - Real Time Counter with Separate Oscillator
 - Four PWM Channels
 - 8-channel, 10-bit ADC
 - 8 Single-ended Channels
 - 7 Differential Channels
 - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
 - Byte-oriented Two-wire Serial Interface
 - Programmable Serial USART

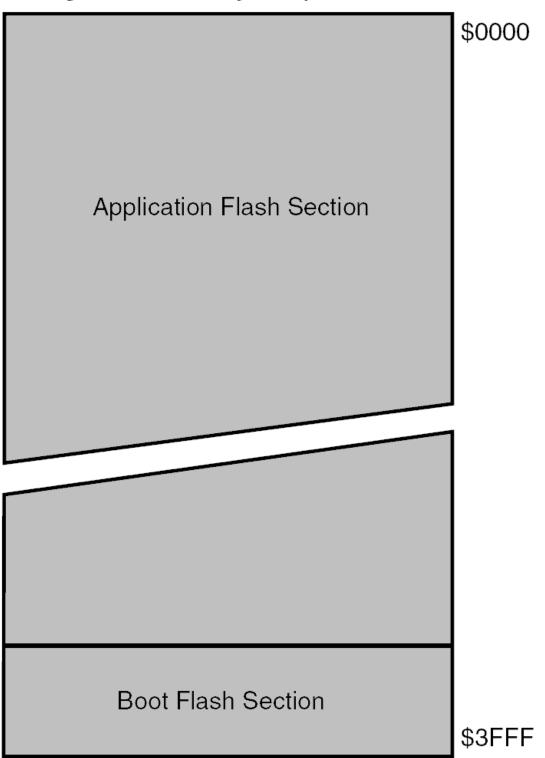
- Master/Slave SPI Serial Interface
- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated RC Oscillator
 - External and Internal Interrupt Sources
 - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Powerdown, Standby and Extended Standby
- 32 Programmable I/O Lines
- Operating Voltages
 - 4.5 5.5V
- Speed Grades
 - 0 16 MHz

BLOCK DIAGRAM



MEMORY MAP:





Data Memory Map

Register File

R0	
R1	
R2	
R29	
R30	
R31	
I/O Registers	
\$00	
\$01	
\$02	
\$3D	
\$3E	
\$3F	

Data Address Space

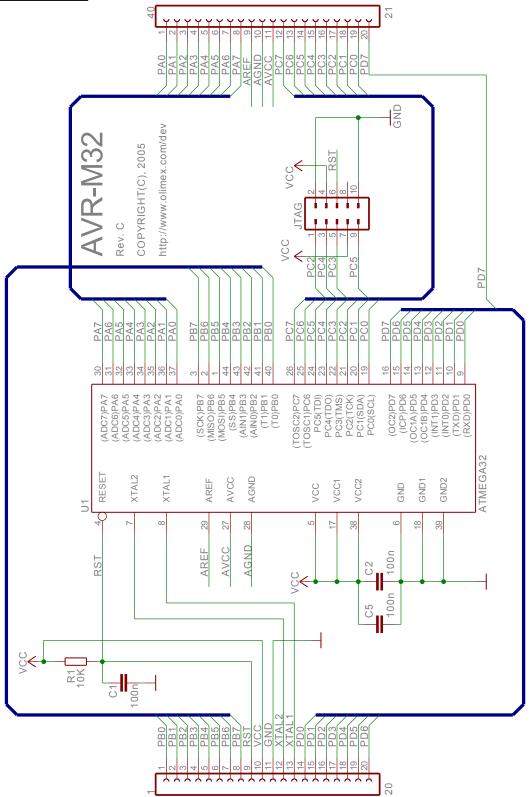
\$0000	
\$0001	
\$0002	
\$001D	
\$001E	
\$001F	

\$0020	
\$0021	
\$0022	
\$005D	
\$005E	
\$005F	

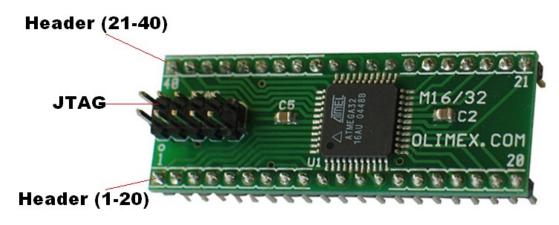
Internal SRAM

\$0060
\$0061
\$085E
\$085F

SCHEMATIC



BOARD LAYOUT



POWER SUPPLY CIRCUIT

The board is power supplied from header connector (1-20) pin 10 and pin 11 with 5V DC.

RESET CIRCUIT

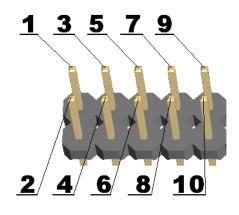
AVR-M32 reset circuit is made with RC group (R1 and C1) and includes pin 6 of JTAG connector, pin 9 of header connector (1-20), and ATmega32 pin 4.

JUMPER DESCRIPTION

There are no jumpers on this board.

CONNECTOR DESCRIPTIONS <u>JTAG</u>

Pin #	Signal Name
1	PC2
2	GND
3	PC4
4	+5V
5	PC3
6	RST
7	+5V
8	NC
9	PC5
10	GND



HEADER CONNECTOR (1-20)

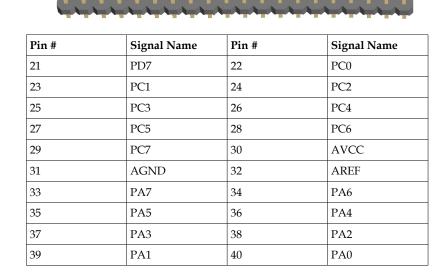
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20



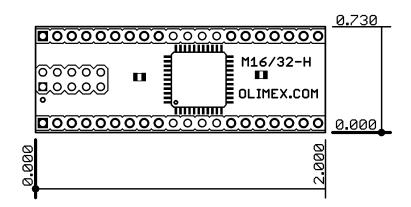
Pin #	Signal Name	Pin #	Signal Name
1	PB0	2	PB1
3	PB2	4	PB3
5	PB4	6	PB5
7	PB6	8	PB7
9	RST	10	+5V
11	GND	12	XTAL2
13	XTAL1	14	PD0
15	PD1	16	PD2
17	PD3	18	PD4
19	PD5	20	PD6

HEADER CONNECTOR (21-40)

21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40



MECHANICAL DIMENSIONS



All measures are in Inches.

AVAILABLE DEMO SOFTWARE

n. a.

ORDER CODE

AVR-M32 - Fully assembled and tested with ATmega32-16AC microcontroller

How to order? You can order to us directly or by any of our distributors. Check our web <u>www.olimex.com/dev</u> for more info.

Revision history:

REV. C - create January 2005

Disclaimer:

© 2009 Olimex Ltd. All rights reserved. Olimex®, logo and combinations thereof, are registered trademarks of Olimex Ltd. Other terms and product names may be trademarks of others.

The information in this document is provided in connection with Olimex products. No license, express or implied or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Olimex products.

Neither the whole nor any part of the information contained in or the product described in this document may be adapted or reproduced in any material from except with the prior written permission of the copyright holder.

The product described in this document is subject to continuous development and improvements. All particulars of the product and its use contained in this document are given by OLIMEX in good faith. However all warranties implied or expressed including but not limited to implied warranties of merchantability or fitness for purpose are excluded.

This document is intended only to assist the reader in the use of the product. OLIMEX Ltd. shall not be liable for any loss or damage arising from the use of any information in this document or any error or omission in such information or any incorrect use of the product.