

Enpirion EP53x2Q family of DCDC Converter Module Evaluation Board

Introduction

Congratulations! You are evaluating a new class of DCDC converter product, a complete power system on silicon:

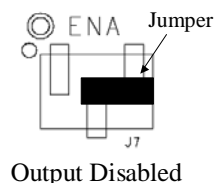
- The EP53x2Q is a complete module including magnetics and requiring only ceramic input and output capacitors.
- The evaluation board is designed to offer a wide range of engineering evaluation capabilities. This includes the base configuration of an 0805 2.2uF input capacitor for EP5352QI and EP5362QI models and 4.7uF input capacitor for EP5382QI models, and an 0805 10uF output capacitor.
- Pads are available to add up to one additional input capacitor and up to two additional output capacitors to allow for evaluation of performance over a wide range of input/output capacitor combinations.
- Pads are available to populate an external divider if desired.
- Easy jumpers are provided for the following signals:
 - Enable
 - VS0-VS2 output voltage select
- Numerous test points are provided as well as clip leads for input and output connections
- The board comes with input decoupling and reverse polarity protection to protect the device from common setup mishaps.

Quick Start Guide

Figure 1 shows a top view of the evaluation board.

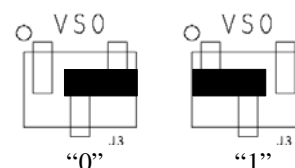
STEP 1: Set the “ENA” jumper to the Disable Position.

CAUTION: the signal pins, ENA, VS0, VS1, and VS2 must be connected to a “high” or a “low”. If left floating the state is indeterminate.



STEP 2: Set the output voltage select pins for the desired output voltage setting. Refer to the section on output voltage select to determine the setting.

CAUTION: the external divider is not populated. Choosing this option will force the device to 100% duty cycle.



STEP 3: Connect Power Supply to the input power connectors, VIN (+) and GND (-) as indicated in Figure 1.

CAUTION: be mindful of the polarity. Even though the evaluation board comes with reverse polarity protection diodes, it is rarely a good idea to reverse the input polarity.

STEP 4: Connect the load to the output connectors VOUT (+) and GND (-), as indicated in Figure 1.

STEP 5: Power up the board and move the ENA jumper to the enabled position. The EP53x2Q is now powered up.

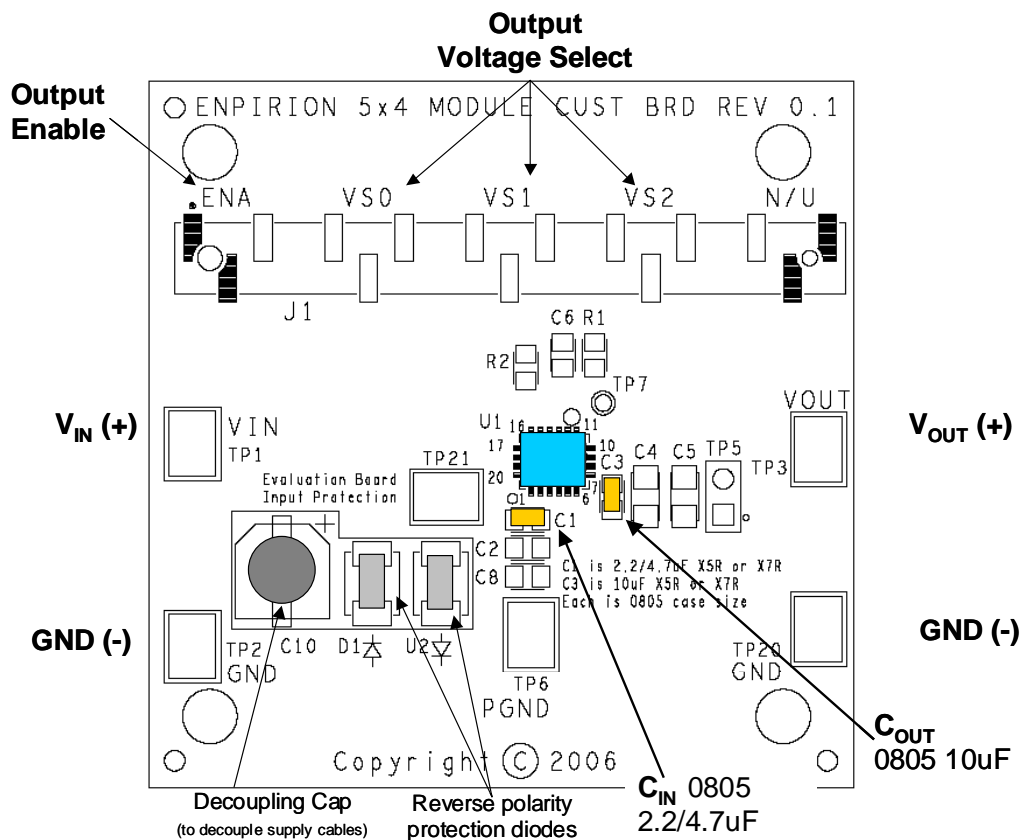


Figure 1. Evaluation Board Layout.

Output Voltage Select

The EP53x2Q utilizes a 3 pin output voltage select scheme. The output voltage is programmed by setting the VSx jumpers to either a logic “1” or a logic “0” as described in the Quick Start section

Table 1 shows the truth table for V_{OUT} selection. There are seven preset output voltage levels which can be chosen via the VSx jumpers.

Table 1. Output Voltage Select Truth Table

VS0	VS1	VS2	V _{out}
0	0	0	3.3
0	0	1	3.0
0	1	0	2.8
0	1	1	2.7
1	0	0	2.5
1	0	1	1.8
1	1	0	1.2
1	1	1	External

CAUTION: the standard evaluation board configuration does not populate the external divider. Selecting the external divider option without populating the external divider will result in unpredictable behavior but can result in the device going into 100% duty cycle and delivering the input rail voltage to the output.

CAUTION: All signal pins must be connected to either a logic “1”, jumper to the left, or to a logic “0”, jumper to the right. Leaving the jumper open will result in an indeterminate state.

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided. This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a balanced impedance probe tip to measure switching signals to avoid noise coupling into the probe ground lead.

Using The External Voltage Divider

The EP53x2Q-E evaluation board is designed to provide a great deal of flexibility in evaluating the performance of the Enpirion DCDC module.

Pre-tinned pads are provided to place 0402 sized 1% resistors on the board to implement an external resistor divider to choose an output voltage other than one of the seven pre-set voltages available on the VID.

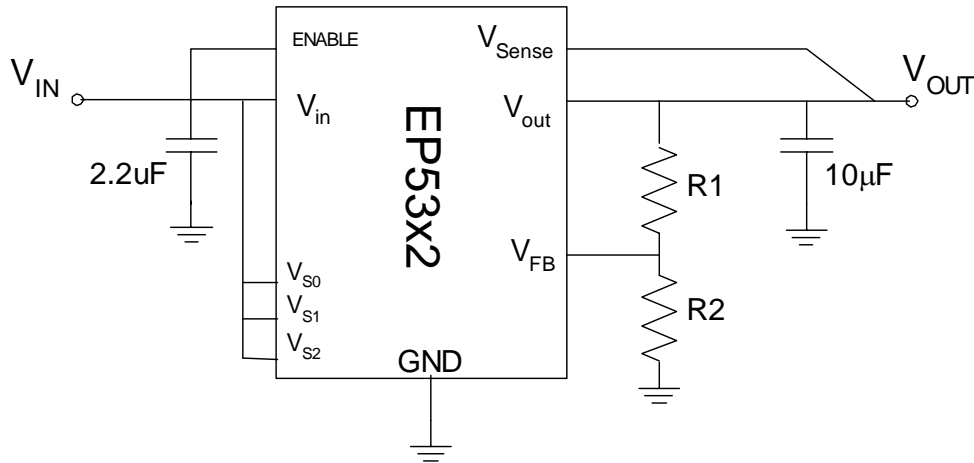


Figure 2. External divider schematic.

Figure 3 demonstrates the placement of the R1 and R2 resistors.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V \left(1 + \frac{R1}{R2} \right)$$

R₁ must be chosen as 200KΩ to maintain loop gain. Then R₂ is given as:

$$R_2 = \frac{1.2 \times 10^5}{V_{OUT} - 0.6} \Omega$$

The external voltage divider option is chosen by setting the jumpers VS0, VS1, and VS2 to a logic "high".

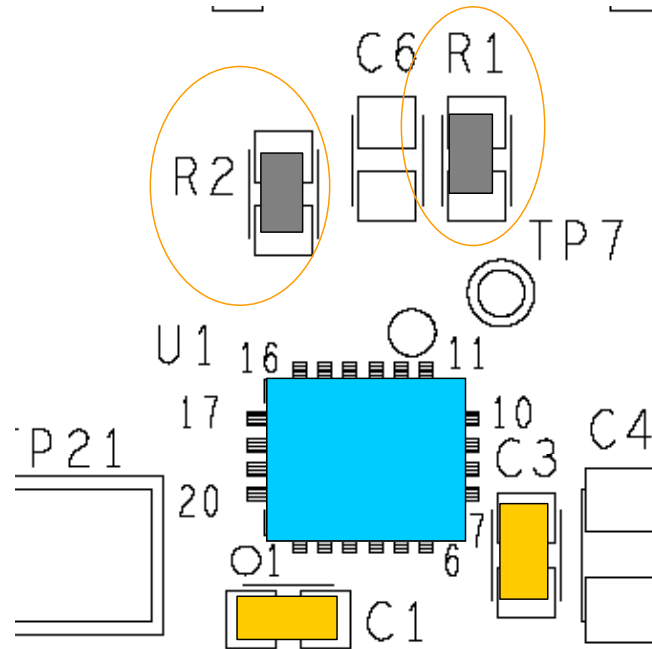


Figure 3. Placement of external divider resistors

Dynamically Adjustable Output

The EP53x2Q is designed to allow for dynamic switching between the predefined voltage levels, or between the predefined output levels and an external divider. The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is 4mV/uS.

This feature can be tested by connecting the VSx jumper center pins to logic driver to toggle between the various V_{OUT} states.

Input and Output Capacitors

The **input** capacitance requirement is 2.2 μF for the EP5352QI and the EP5362QI, and 4.7 μF for the EP5382QI. Enpirion recommends that a low ESR MLCC capacitor be used. The EP53x2Q-E is populated with a 2.2 μF 0805 capacitor. There are pre-tinned pads that allows for additional 0805 capacitors to experiment with input filter performance.

The **output** capacitance requirement is a minimum of 10 μF . The control loop is designed to be stable with up to 60 μF of total output capacitance. The evaluation board comes populated with a single 10 μF 0805 capacitor.

The board has pre-tinned pads for up to 2 additional output capacitors with either 0805 or 1206 footprint.

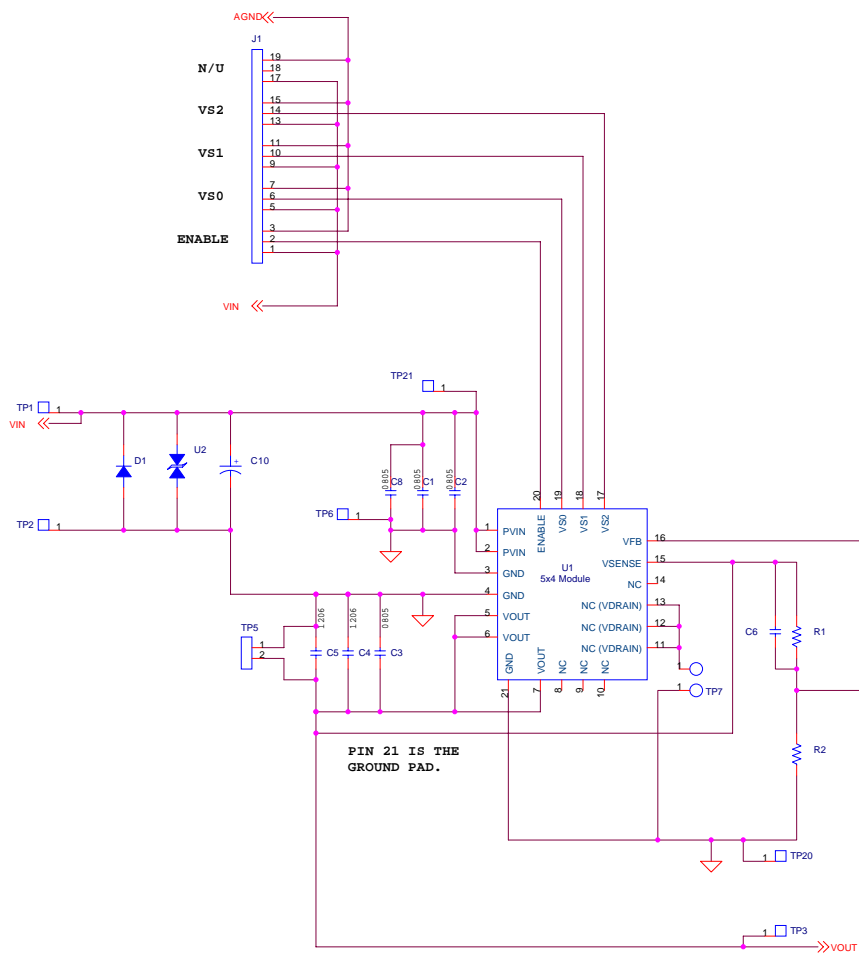
Capacitance above the 10 μF minimum can be added if the transient performance is not sufficient using the 10 μF . Enpirion recommends a low ESR MLCC type capacitor be used.

NOTE: Capacitors must be X5R or X7R dielectric formulations.

Contact Information

Enpirion, Inc.
685 Route 202/206
Suite 305
Bridgewater, NJ 08807
Phone: 908-575-7550
Fax: 908-575-0775

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Revision	Description	Date	Approved
p1	PRELIMINARY RELEASE	3/2/2006	CJR
p2	Added TP4, TP7. Removed FPM connection.	3/21/2006	CJR
p3	Removed PGND	4/5/2006	CJR
p4	Removed component values, AGND, connections to pins 8-10, & FPM.	7/5/2006	CJR

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Enpirion 5x4 Module Customer Evaluation Board

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Date		Sheet		C. Romano	p4
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