User's Manual

MPC852TADSRM/D
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MPC852TADS

User's Manual

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1 - Hardware Preparation

1•1 Jumpers and Dip-Switches

Ensure the following jumpers are in place:

TABLE 1-1. Default Jumpers and dip switches settings

Reference Name	Description	Default
J1	Clock Oscillator source: 1-2: 10MHz on board clock oscillator. 2-3: External clock oscillator.	1-2: 10MHz on board clock oscillator.
SW1	Power Switch ON/OFF	Power Switch OFF
SW4	Modin Selector: Modin[1..2] = 'OFF,ON'	Modin[1..2] : 'OFF,ON' = '1,0'
SW5	S/W Options[4..1]: 'ON,ON,ON,ON'	S/W Option[4..1]: 'ON,ON,ON,ON'='0000'

1•2 Connections

Connect the following connectors :

- P16 - Power Supply 5.0V DC.
- P13 - Power Supply 12.0V DC for PCMCIA channel or for Flash Programming.
- P12 - BDM Connector via External Command Converter to Host Computer Parallel Port.
- P17A (Down) - RS232-1 Connector to Host Computer COM1 Port.

1•3 Run

- Turn on the 5V power supply and verify LD8, LD14, LD15, LD17, LD18 Leds on board lit up.

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1 - General Information

1•1 MPC852TADS Introduction and Goals

This operation guide for the MPC852TADS board contains operational, functional and general information. The MPC852T is a Power PC architecture based derivative of Motorola MPC860 Quad Integrated Communication Controller (PowerQuicc™). As such the MPC852TADS board is a derivative of the MPC866ADS. It is designed to serve as a platform for both software and hardware development using the MPC852T processor.

On-board resources and the associated debugger enable developers to perform a variety of tasks: download and run code; set breakpoints; display memory and registers; and, connect proprietary h/w via the expansion connectors. All these features may be incorporated into a selected system using the MPC852T processor.

The MPC852TADS board may be used as a demonstration tool. For example, the application software may be burned[A] into its flash memory and run in exhibitions.

1•2 List of Abbreviations

- ADS - MPC852TADS, the document subject
- BCSR - Board Control & Status Register
- BGA - Ball Grid Array
- GPCM - General Purpose Chip-Select Machine
- GPL - General Purpose Line (associated with UPM)
- SIMM - Single In-line Memory Module
- UPM - User Programmable Machine

1•3 Related Documentation

- MPC866 Family User Manual
- Davicom 10/100Mbps Fast Ethernet DM9161E Transceiver
- IEEE Std. 1284-1994 Standard

1•4 SPECIFICATIONS

The MPC852TADS specifications are given in TABLE 1-1.

TABLE 1-1. MPC852TADS Specifications

CHARACTERISTICS	SPECIFICATIONS
Power requirements (no other boards attached)	+5V DC @ 1.4 A (typical), 3 A (maximum) +12V DC@1A.
Microprocessor	MPC852T running @ 66 MHz bus speed

A. Either on-board or off-board.

General Information

TABLE 1-1. MPC852TADS Specifications

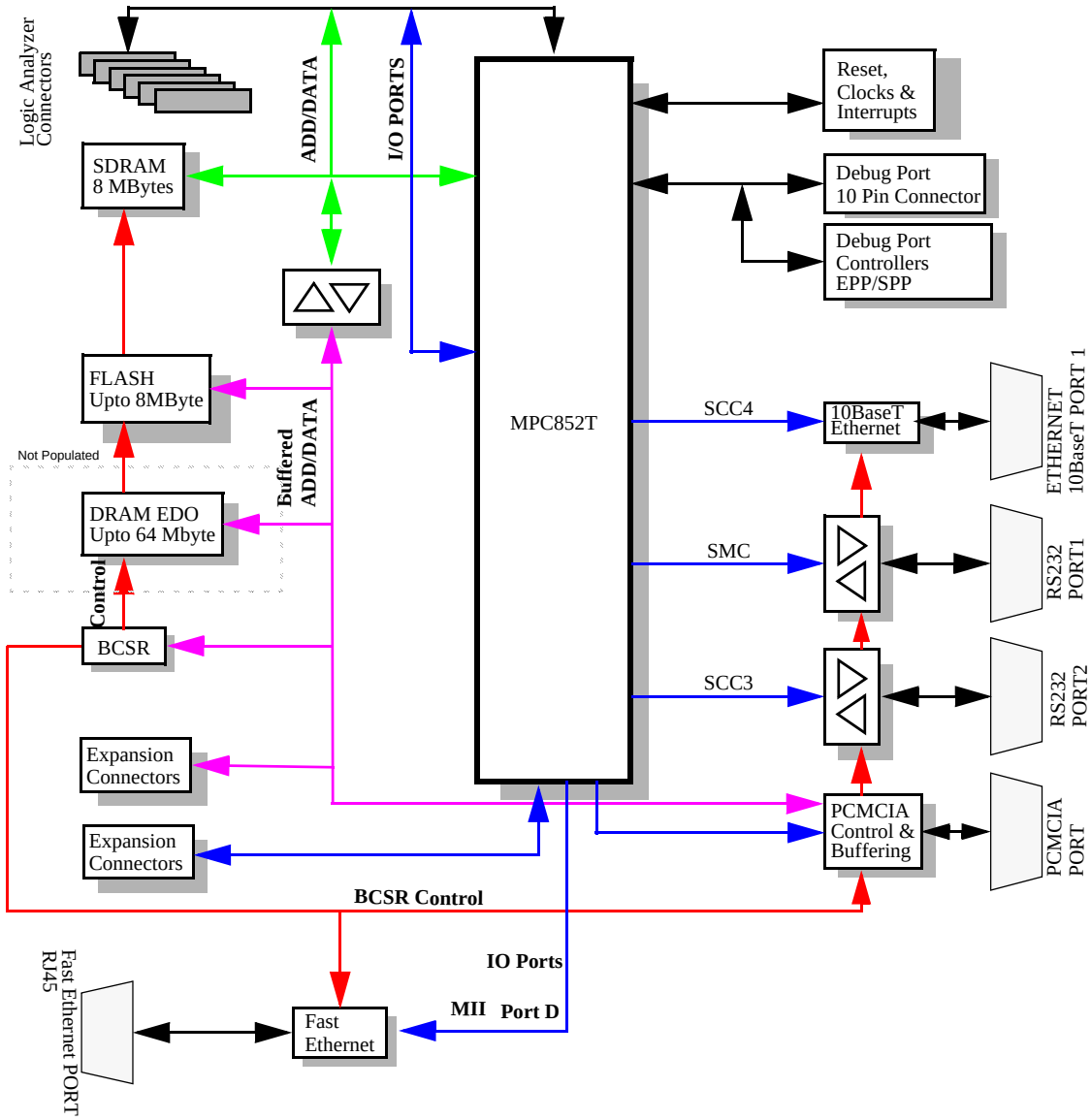
CHARACTERISTICS	SPECIFICATIONS
Addressing Total Address Range: Flash Memory Dynamic RAM optional not populated. Synchronous DRAM	 4 GB 2 MB, 32-bit wide expandable to 8 MB 4 MB, 32-bit wide EDO SIMM, optional support for up to 32 MB, EDO or FPM SIMM 8 MB, SDRAM
Operating temperature	0^{O}C - 30^{O}C
Storage temperature	-25^{O}C to 85^{O}C
Relative humidity	5% to 90% (non-condensing)
Dimensions: Length Width Thickness	 9.173" (233 mm) 5.9" (150 mm) 0.063" (1.6 mm)

1•5 MPC852TADS Features

- ***The MPC852TADS is compatible with the old MPC86xADS board.***
- The MPC852T, when mounted on a BGA socket, runs at 66 MHz bus frequency.
- 8 MB, unbuffered, synchronous DRAM.
- 4 MB EDO 60nsec delay DRAM SIMM. Support for 4 - 32 MB FPM or EDO DRAM SIMM with Automatic DRAM SIMM identification. 16-bit data - bus width support. The optional EDO DRAM will not be populated on-board.
- 2 MB Flash SIMM. Support for up to 8 MB. 5V or 12V Programmable with Automatic Flash SIMM identification. Can be changed up to 8MB.
- Optional Hard-Reset Configuration Burned in Flash[A].
- Dual RS232 port.
- Fast Ethernet connection to Port-D using Davicom DM9161E.
- 10-Base-T Port On-board using Davicom DM9161E.
- Memory Disable Option for every local memory map slave.
- Board Control & Status Register - 5 BCSR controlling board operation.
- External Tool Identification Capability via BCSR.
- Programmable Hard-Reset Configuration via BCSR.
- 5V only PCMCIA Socket with full buffering, power control and port disable options. Complies with PCMCIA 2.1+ Standard.
- Module Enable Indications in order to control external peripherals, expansion connectors include all the CPM ports & bus signals.
- On-board Debug Port Controller & EPP/SPP Interface.
- Push button for Soft- / Hard-[B] Reset.
- ABORT button.
- Single[C] 5V supply.
- Reverse / Over Voltage Protection for Power Inputs.
- 3.3V VDDH and 1.8V VDDL are supplied for MPC852T.

A. Flash burning available only if also supported on the MPC852T.
B. To activate hard-reset, press BOTH the soft-reset & ABORT buttons.
C. Use 5V single supply unless a 12V supply is required for a PCMCIA card or a 12V programmable Flash SIMM.

FIGURE 1-1 MPC852TADS Block Diagram



2 - Hardware Preparation and Installation

2•1 INTRODUCTION

This chapter describes unpacking instructions, hardware preparation and installation instructions for the MPC852TADS.

2•2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton arrives damaged request that the carrier agent be present at the time of equipment unpacking and inspection.

Remove equipment from the shipping carton. Consult the packing list and verify that all listed items are present. Save the packing material in the instance that either storage or reshipment of the equipment should become necessary.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY AS STATIC DISCHARGE CAN DAMAGE CIRCUITS.

2•3 HARDWARE PREPARATION

Prior to installation it may be necessary to change the DIP switch settings or jumpers in order to achieve both the desired configuration and ensure proper operation of the MPC852TADS board. FIGURE 2-1 "MPC852TADS Top-Side Part Location Diagram" illustrates the location of the switches, LEDs, DIP switches, jumpers and connectors. The factory tested boards are delivered with default DIP switch settings. The default settings are described in the paragraphs below.

Parameters relating to the below listed features may be changed:

- MPC Clock Source
- Host Controlled Operation
- PCMCIA Enable
- MPC I/O port connected to Expansion Connector

FIGURE 2-1 MPC852TADS Top-Side Part Location Diagram

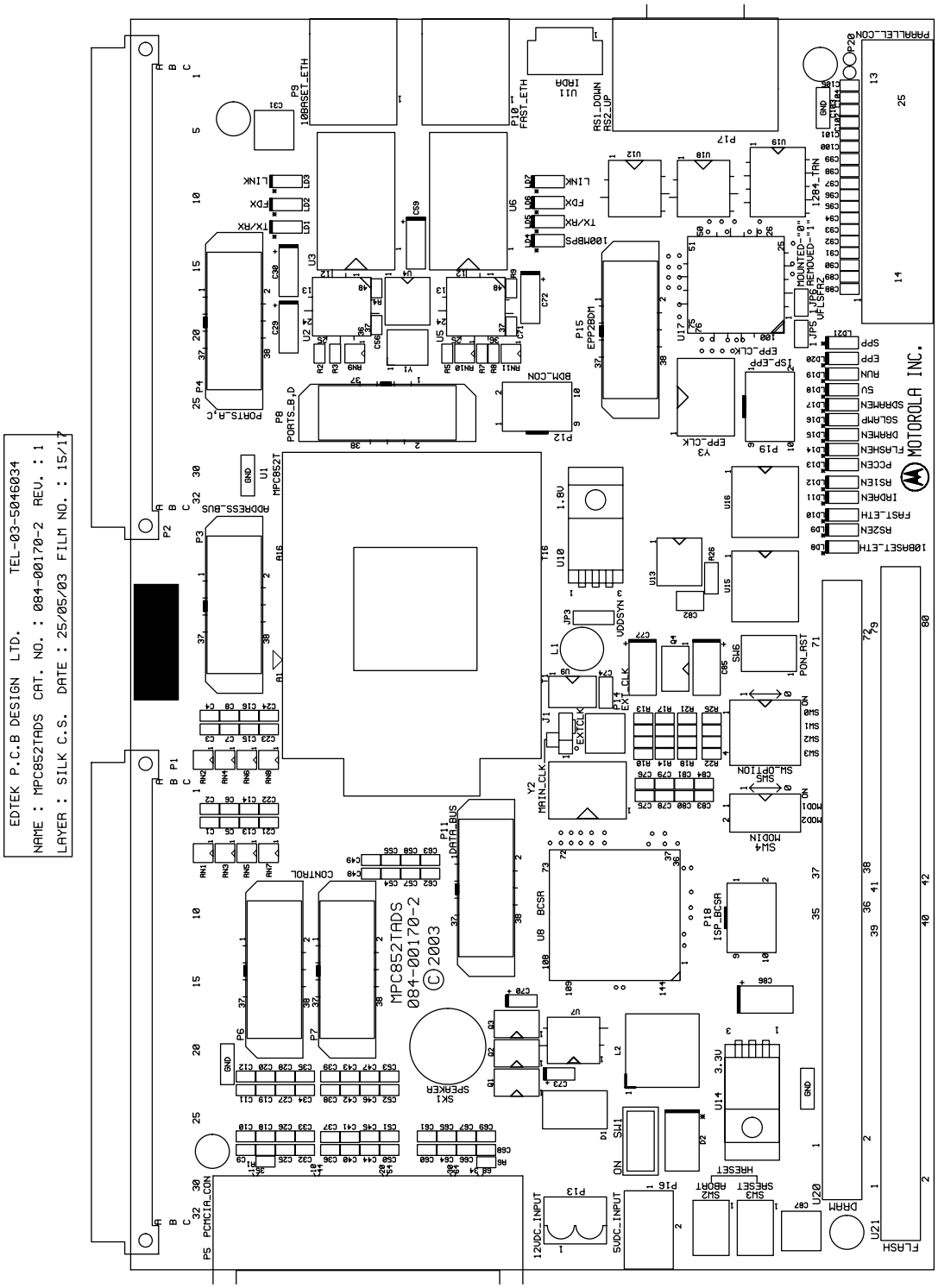
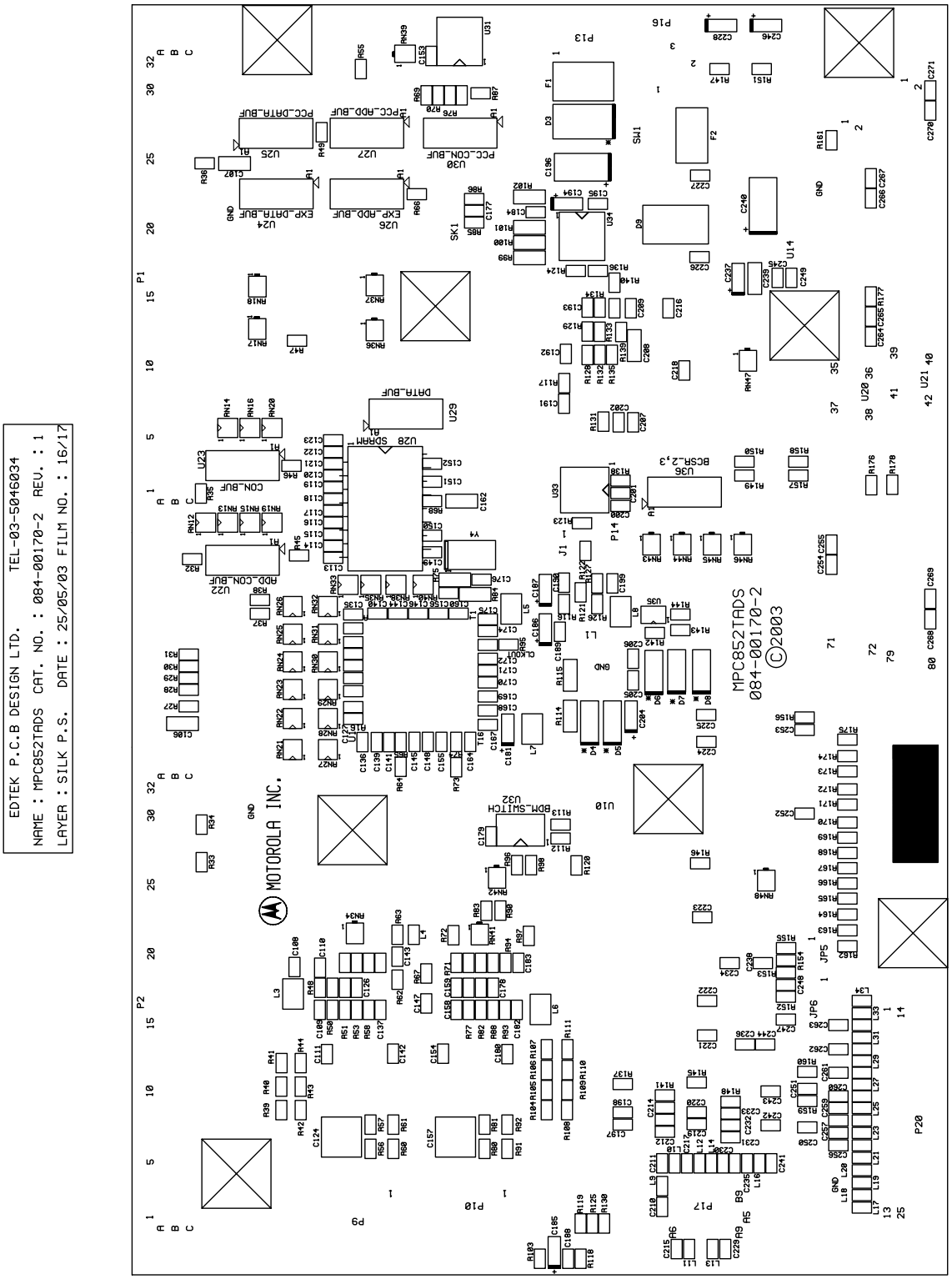


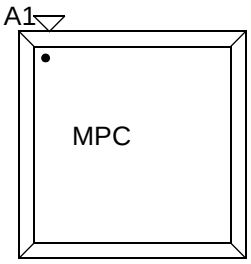
FIGURE 2-2 MPC852TADS Bottom-Side Part Location Diagram



2•3•1 MPC Replacement of U1

Turn off the power prior to replacing the MPC. Note the location of the original MPC A1 pin when replacing a U1 with another MPC. Set the new MPC in the same direction as the previous one.

FIGURE 2-3 MPC TOP-VIEW

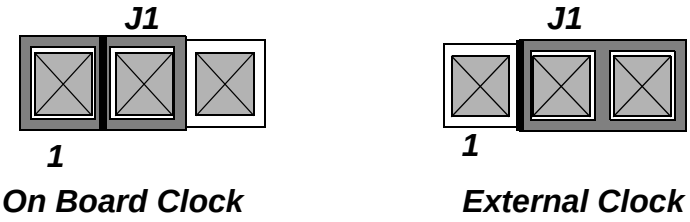


2•3•2 Clock Source Selection - J1

The clock source for the MPC is selected by J1. When a jumper is placed between position 1-2, On board Clock is selected either 10MHz Clock generator or 10MHz Crystal resonator depending on SW4 position.

When a jumper is placed between position 2-3, External Clock is selected.

FIGURE 2-4 Clock Source Selection - J1



2•3•3 Modin Selection - SW4

The on board clock source for the MPC is selected by SW4. The on-board 10MHz crystal resonator connected between EXTAL and XTAL MPC pins, becomes the clock source when SW4[1-2] = ['ON','ON'] or ['ON','OFF'] and the ADS is powered-up. However, when SW4[1-2] = ['OFF','ON'] or ['OFF','OFF'] but the ADS is powered-up, then the on-board 10MHz clock generator connected to EXTCLK MPC pin, becomes the clock source. Clkout is calculated by CLK_IN, 10MHz, multiplied by the PLL multiplication factor. See TABLE 2-1. "Power ON Reset DPLL Configuration" on page 9.

NOTE

Crystal resonator circuit is not assembled on board.

FIGURE 2-5 Modin Selection - SW4

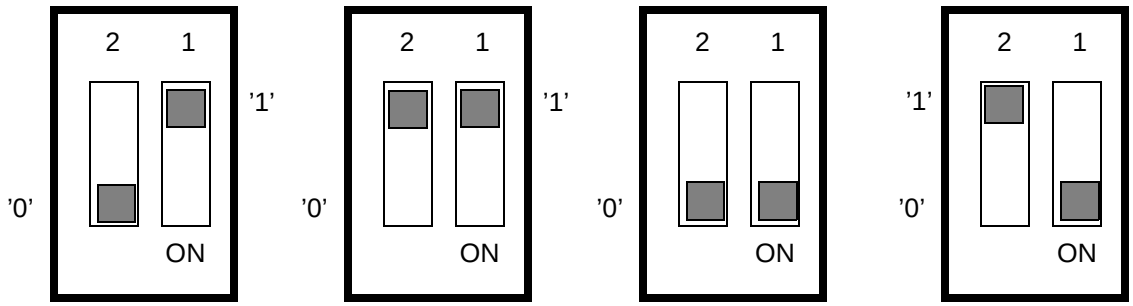


TABLE 2-1. Power ON Reset DPLL Configuration

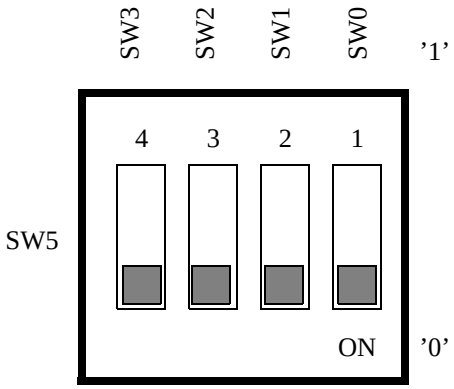
MODCK[1-2]	*Default at Power On Reset*		*DPLL and Interface Input*	*System Frequency*
	MFI[12-15]	*PDF[27-30]*		
00	8	0000	OSCM Freq[a]	40MHz for 10MHz input Crystal
01	15	0000	OSCM Freq	75MHz for 10MHz input Crystal
10	8	0011	EXTCLK Freq	1:1 Mode[b]
11	15	0000	EXTCLK Freq	75MHz for 10MHz input Clock Oscillator

a. OSCM Freq means the Frequency between EXTAL and XTAL MPC pins.
b. If Clock in is 10MHz Clock Oscillator, the System Frequency is 10MHz.

2•3•4 Software Option - SW5

SW5 is a 4-Dip Switch. This switch is connected over SWOPT[0-3] lines which are available at BCSR2. S/W Options may be manually selected, according to SW5 state. SW5 is factory set to all'ON'.

FIGURE 2-6 S/W Option - SW5



2•4 INSTALLATION INSTRUCTIONS

Boards are shipped without DRAM EDO. Since all the SW is based on the DRAM it is necessary that the user change BR2, BR3, BR4 and OR4. In BR2, BR3 the valid bit should be 0 (bit 31), BR4 = 0x000000C1 and OR4 should be 0xFC800A00. This configuration will map the SDRAM to ADD 0 & 0x3000000 for 8MB. Once configured, the MPC852TADS may be installed as per the required working environment:

- Host Controlled Operation
- Standalone

2•4•1 Host Controlled Operation

For host-controlled operation, a host computer controls the board via the BDM Debug Port, which is a subset of the JTAG port. This configuration serves for extensive debugging using an on-host debugger. Host computer connects with the board as follows:

- or through External Command Converter provided by a third party -

Macraigor System.

- or through On-Board Serial Command Converter[A] -

No needs an external part.

- or through On-Board Enhanced Parallel Port (EPP) Converter[A] -

No needs an external part.

A. For FUTURE USE

FIGURE 2-7 Host-Controlled Operation Scheme with External Command Converter

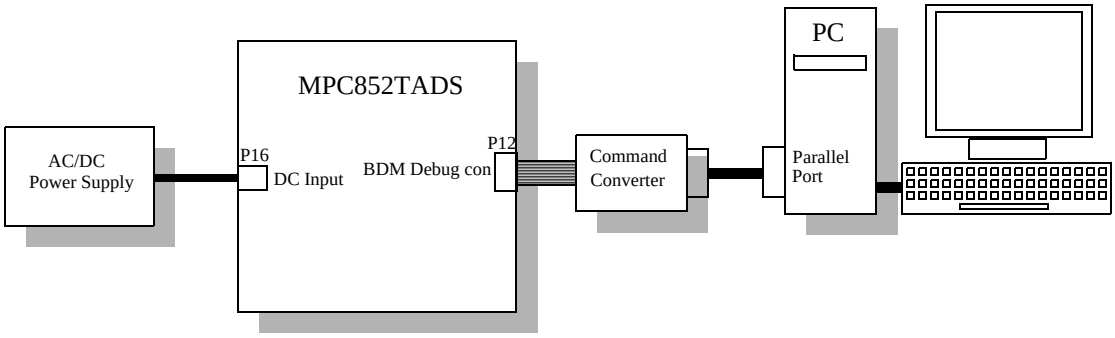
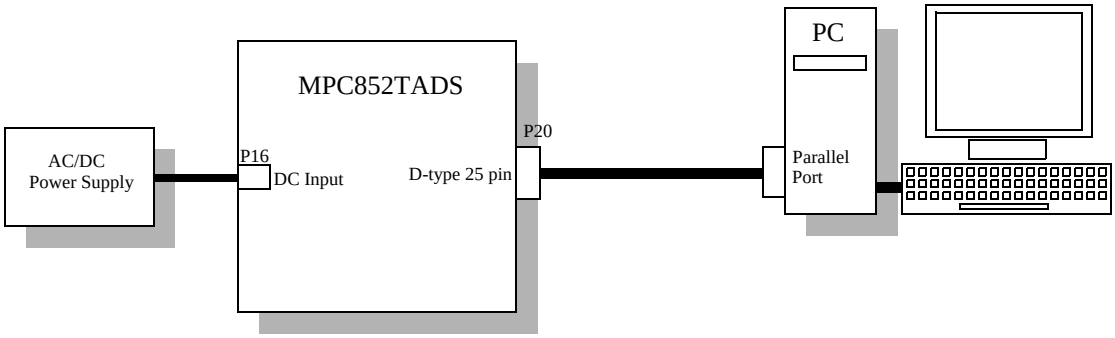


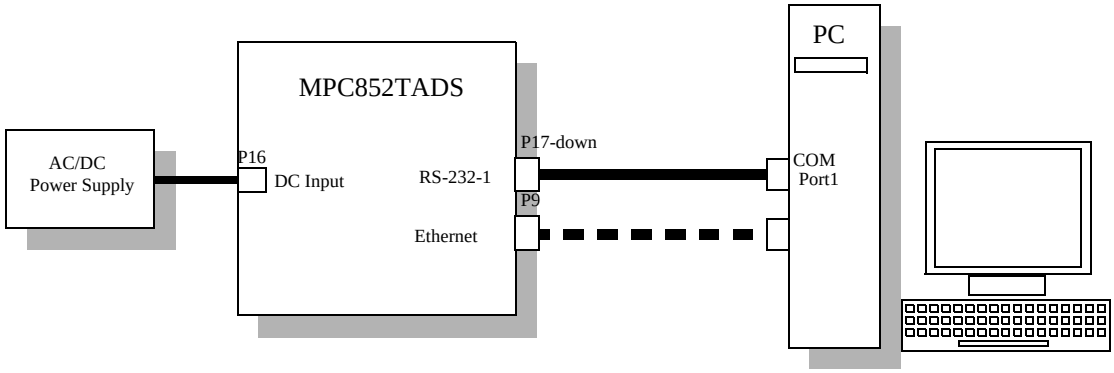
FIGURE 2-8 Host-Controlled Operation on board Command Converter schem



2•4•2 Standalone Operation

In this mode the ADS is not controlled by the host via the debug port. Rather, connection to the host may be made via another port, e.g., RS232 port, Ethernet port, etc. Operations in this mode require that an application be programmed into the board's Flash memory. No memory is required with host-controlled operations.

FIGURE 2-9 Standalone operation schem



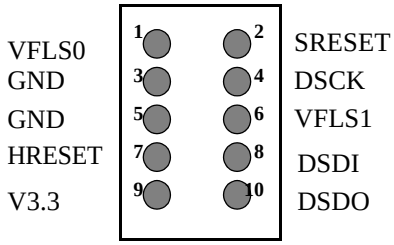
2•4•3 10/100-Base-T Ethernet Ports Connection - P9, P10

The 10/100-Base-T port connectors - P9 and P10, are an 8-pin, 90°, receptacle RJ45 connectors. The connection between the 10/100-Base-T ports to the network is done by a standard cable. The pinout of P9 and P10 is described in TABLE 5-11. "P9, P10: 100/10Base-T Ethernet Port Interconnect Signals" on page 83.

2•4•4 BDM Debug Port Connector - P12

Users may also control the board via the Bdm debug port connector. Currently, the majority of control SW use this connector via a command converter box connected to the PC parallel port.

FIGURE 2-10 BDM Debug Connector - P12

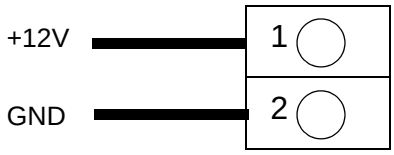


2•4•5 +12V Power Supply Connection - P13

The MPC852TADS requires a +12 Vdc @ 1 A max power supply for either the PCMCIA channel Flash programming capability or the 12V programmable Flash SIMM. As long as there is no need to program either a 12V programmable PCMCIA flash card or a 12V programmable Flash SIMM then the MPC852TADS works properly without a +12V power supply.

Connect the +12V power supply to connector P13 as shown below:

FIGURE 2-11 +12V Power Connector - P13

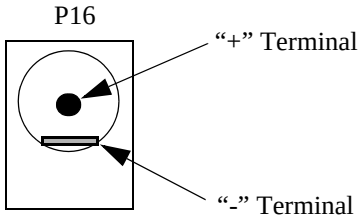


P13 is a 2-terminal block power connector with power plug. The plug is designed to accept 14 to 22 AWG wires though the use of between 14 to 18 AWG wires is recommended.

2•4•6 +5V Power Supply Connection - P16

The MPC852TADS requires a +5 VDC @ 3A max power supply for operation. Connect the +5V power supply to connector P16 as shown below:

FIGURE 2-12 P16: +5V Power Connector



P16 is a power jack connector.

NOTE

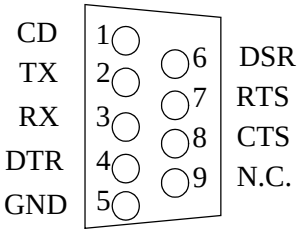
Hardware applications may be connected to the MPC852TADS via expansion connectors P1 & P2. Power consumption should be considered when a power supply is connected to the MPC852TADS. Thus when adding HW to the expansion connectors note that the new addition will not consume more power than 1A.

2•4•7 Terminal to MPC852TADS RS-232 Connection - P17

RS232 equipment and serial RS232 terminals may be connected to P17A and P17B RS-232 connectors. The RS-232, shown in FIGURE 2-13 "RS-232 Serial Port Connectors: P17A & P17B", is a female, 9-pin, stacked D-type connector.

The connectors are arranged in a manner that allows for a 1:1 connection via a flat cable to the serial port of an a personal computer.

FIGURE 2-13 RS-232 Serial Port Connectors: P17A & P17B



Note: On the MPC852TADS, the RTS line (pin #7) is not connected.

2•4•8 Parallel Host Connector in EPP I/F - P20

The MPC852TADS' P20-EPP interface connector is a male, 25-pin, D-type connector. The connection between the MPC852TADS and the host computer is by 25-line flat cable. This connector enables connection to host computer when using On board serial command converter or EPP converter. When connection to host is made via P20, the capability of working with an external BDM Debug connector is disabled. FIGURE 2-14 "Parallel host connector with EPP I/F - P20" below shows the pin configuration of the connector when choosing EPP Mode transfer.

FIGURE 2-15 "Parallel host connector in serial mode - P20" below shows the pin configuration of the same connector when choosing Serial Mode transfer.

FIGURE 2-14 Parallel host connector with EPP I/F - P20

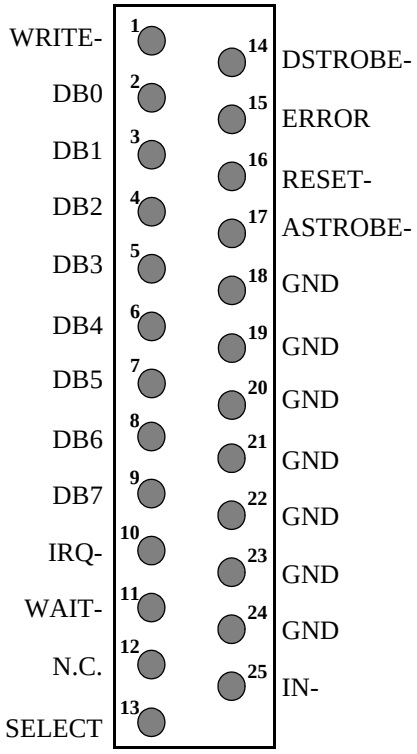
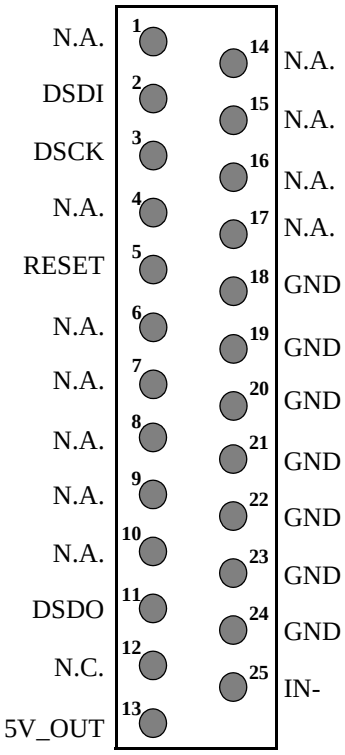


FIGURE 2-15 Parallel host connector in serial mode - P20



2•4•9 Memory Installation

The MPC852TADS has two types of memory SIMM:

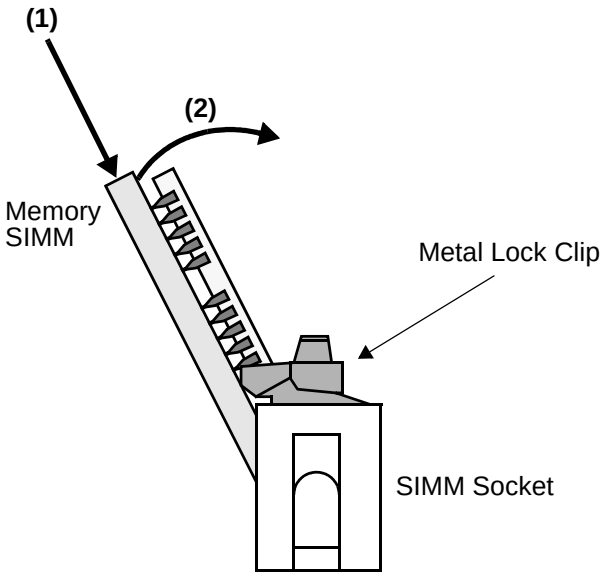
- Dynamic Memory SIMM: will not be populated, only the socket will be soldered.
- Flash Memory SIMM.

Installation of a memory SIMM: remove from packaging; place diagonally in its socket - difficult to err as the Flash socket has 80 contacts, while the DRAM socket only has 72; twist to a vertical position until the metal lock clips are locked. See FIGURE 2-16 "Memory SIMM Installation".

CAUTION

Near the #1 pin the memory SIMMs have an alignment nibble. It is essential to correctly align the memory before twisting as damage may result to both the memory SIMM and its socket.

FIGURE 2-16 Memory SIMM Installation



3 - OPERATING INSTRUCTIONS

3•1 INTRODUCTION

Information necessary for using the MPC852TADS in both host-controlled and standalone configurations is detailed in this chapter. The information includes controls and indicators, memory map details and board software initialization.

3•2 CONTROLS AND INDICATORS

The MPC852TADS features the switches and indicators noted in the following sub-sections.

3•2•1 ABORT Switch, SW2

The SW2 ABORT switch is used for aborting program execution. This is done by issuing a level 0 interrupt to the MPC. There is no resident debugger with the MPC852TADS. As such, if the ADS is in standalone mode, it is the users responsibility to provide a means of handling the interrupt. The Abort switch signal is debouncing and cannot be disabled by software.

3•2•2 SOFT RESET Switch, SW3

The SW3 SOFT RESET switch performs Soft Reset on the MPC internal modules while maintaining MPC configuration (clock & chip-select) Dram and SDram contents. The switch signal is debouncing and cannot be disabled by software. Upon completion of the Soft Reset sequence, the Soft Reset configuration is sampled prior to becoming valid.

3•2•3 HARD RESET Switches, SW2 & SW3

When both the SW2 and SW3 switches are depressed simultaneously then HARD RESET is generated on the MPC. When the MPC undergoes Hard Reset it must be re initialized as its configuration is lost - including data stored in the DRAM or SDRAM. Upon completion of the Hard Reset sequence, the Hard Reset configuration stored in BCSR0 becomes valid.

3•2•4 Modin Selection, SW4

The on board clock source for the MPC is selected by SW4. The on-board 10MHz crystal resonator[A] connected between EXTAL and XTAL MPC pins, becomes the clock source when SW4[1-2] = ['ON','ON'] or ['ON','OFF'] and the ADS is powered-up. However, when SW4[1-2] = ['OFF','ON'] or ['OFF','OFF'] but the ADS is powered-up, then the on-board 10MHz clock generator connected to EXTCLK MPC pin, becomes the clock source. Clkout is calculated by CLK_IN, 10MHz, multiplied by the PLL multiplication factor. See TABLE 2-1. "Power ON Reset DPLL Configuration" on page 9.

3•2•5 Software Options Switch, SW5

The SW5 SOFTWARE OPTIONS switch is a 4-switch DIP switch. The SW5 is connected over SWOPT(0:3) lines available at BCSR. Software options may be manually selected according to the state of the SW5.

3•2•6 Power-On RESET Switch, SW6

The Power-On RESET switch SW6 performs Power-On reset to the MPC852T, as if the power was re-applied to the

A. Crystal resonator is not assembled on board.

ADS. When the MPC is reset that way, all configuration and all data residing in volatile memories are lost. After PORST signal is negated, the MPC re-acquires the power-on reset and hard-reset configuration data from the hard-reset configuration source. (Flash / BCSR).

3•2•7 GND Bridges

The 4 GND bridges on the MPC852TADS are intended to assist in general measurements and logic-analyzer connections.

WARNING

Use only INSULATED GND clips when connecting to a GND bridge. Failure to do so may result in permanent damage to the MPC852TADS.

3•2•8 Ethernet 10Base-T. ETH TX/RX, LD1

The green ETH TX/RX LED indicates that the Ethernet port, Davicom DM9161E on SCC4, is transmitting or receiving data via the 10 Base-T port.

3•2•9 Ethernet Full Duplex Indicator, LD2

The red ETH FDX LED indicates that the Ethernet port, Davicom DM9161E on SCC4, is in Full Duplex operation mode.

3•2•10 Ethernet LINK Indicator, LD3

The yellow ETH Twisted Pair LINK LED indicates, that there is a good link integrity on the 10-Base-T port. LD3 is off when the link integrity fails.

3•2•11 Fast Ethernet 100Mbps Indicator, LD4

The green FAST ETH 100Mpbs LED indicates that the Fast Ethernet port, Davicom DM9161E on Port D is in 100 Mbps operation mode.

3•2•12 Fast Ethernet 10/100Base-T. TX/RX, LD5

The green FAST ETH TX/RX LED indicates that the Fast Ethernet port, Davicom DM9161E on Port D, is transmitting or receiving data via the 10/100 Base-T port.

3•2•13 Fast Ethernet Full Duplex Indicator, LD6

The red FAST ETH FDX LED indicates that the Fast Ethernet port, Davicom DM9161E on Port D, is in Full Duplex operation mode.

3•2•14 Fast Ethernet LINK Indicator, LD7

The yellow FAST ETH Twisted Pair LINK LED indicates, that there is a good link integrity on the 10/100-Base-T port. LD7 is off when the link integrity fails.

3•2•15 Ethernet 10Base-T. ETH ON, LD8

The yellow ETH ON LED indicates that the Ethernet port transceiver, Davicom DM9161E, is active.

3•2•16 RS232 Port 2 ON, LD9

The yellow RS232 Port 1 ON LED signifies that the RS232 transceiver, connected to SCC3, is active and that communication via that medium is allowed. The RS232 transceiver is in shutdown mode when unlit - an indication that the associated MPC pins may be used off-board via the expansion connectors.

3•2•17 Fast Ethernet 10/100Base-T. ON, LD10

The yellow FAST ETH ON LED indicates that the Fast Ethernet port transceiver, Davicom DM9161E, is active. The Davicom outputs pins are in tri-states when unlit - an indication that the associated Port D pins may be used off-board via the expansion connectors.

3•2•18 RS232 Port 1 ON, LD12

The yellow RS232 Port 1 ON LED signifies that the RS232 transceiver, connected to SMC1, is active and that communication via that medium is allowed. The RS232 transceiver is in shutdown mode when unlit - an indication that the associated MPC pins may be used off-board via the expansion connectors.

3•2•19 PCMCIA ON, LD13

The yellow PCMCIA ON LED indicates the following:

1) Address & strobe buffers are driven towards the PCMCIA card.
2) Data buffers are driven to / from the PCMCIA card whenever CE1A~ or CE2A~ signals are asserted.
3) Card status lines are driven towards the MPC from the PCMCIA card.

When unlit it indicates that the above noted buffers are tri-stated and that the pins associated with the PCMCIA channel A may be used off-board via the expansion connectors.

3•2•20 FLASH ON, LD14

The yellow FLASH ON LED indicates that the FLASH SIMM has been enabled in the BCSR1 register. For example, accessing the CS0~ address space will hit the Flash memory. When unlit the Flash has been disabled.

3•2•21 DRAM ON, LD15

The yellow DRAM ON LED indicates that the DRAM SIMM has been enabled in BCSR1 and that accessing CS2~ (or CS3~) will hit on the DRAM. When unlit the DRAM has been disabled in BCSR1.

3•2•22 SGLAMP ON, LD16

The green SGLAMP LED indicates that this signal is active (low). When inactive there is no LED light. The LED is used for software signalling. Controlling the led is done via BCSR4[3].

3•2•23 SDRAM ON, LD17

The yellow SDRAM ON LED indicates that the SDRAM has been enabled in BCSR1 and that accessing CS4~ will hit on the SDRAM. When unlit the SDRAM has been disabled in BCSR1.

3•2•24 5V Indicator, LD18

The green 5V LED indicates the presence of a +5V supply at P16.

3•2•25 RUN Indicator, LD19

The green RUN LED indicates that the MPC isn't in debug mode.

3•2•26 EPP Indicator, LD20[A]

The yellow Enhanced Parallel Port connection LED indicates that the board is connected directly to the Pc's parallel port using EPP transfer mode and the BDM Debug connector (P12) is irrelevant.

3•2•27 SPP Indicator, LD21[A]

The yellow SPP connection LED indicates that the board is connected directly to the Pc's parallel port using SPP transfer mode and the BDM Debug connector (P12) is irrelevant.

3•3 MEMORY MAP

All access to MPC852TADS memory slaves is controlled by the MPC's memory controller. As a consequence, the user may reprogram the memory map. The debug station performs Hard Reset. Then the debugger checks for the existence, size, delay and type of EDO DRAM and FLASH memory SIMMs that are mounted on board. Accordingly the debugger initializes chip-selects. The SDRAM, DRAM and FLASH memory respond to all types of memory access. For example: user / supervisory; program / data; and DMA.

Following is a memory map description for 2 options: Compatible Mode and MPC852TADS New Mode.

The Compatible Mode uses an EDO DRAM and 8MB SDRAM. Further, all the programmable registers remain the same - the memory map is the same as that of the MPC8xxFADS board with the ***exception*** of OR4 Mask Register bits. The latter are changed according to SDRAM size to 0xFF80.

In the MPC852TADS New Mode the EDO DRAM is not used and consequently the SDRAM is mapped differently. See TABLE 3-1. "Memory Map in MP852TADS New Mode," and TABLE 3-2. "Memory Map in MPC852TADS Compatible Mode". The following programmable changes are necessary in order to work on the board in the MPC852TADS New Mode:

- Programming BR2, BR3 Base Address bits for EDO DRAM aren't valid. The L-bit should be cleared.
- Programming OR4 Mask Register bits for SDRAM should be changed according to SDRAM size. This where the 2 MS bits are not masked. 8MB SDRAM, OR4 Mask bits = 0xFC80. In this case users may view address 0 and also add 30000000 - they are the same word in the memory. Users must also change the BIH to 0.

A. For FUTURE Use

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TABLE 3-1. Memory Map in MP852TADS New Mode,

ADDESS RANGE	*Memory Type*	*Device Type*				*Port Size*
00000000 - 007FFFFF[a]	SDRAM	8MByte				32
02000000 - 020FFFFF	Empty Space					
02000300 - 020003FF	Control Register					
02100000 - 02107FFF	BCSR(0:4)[b]					32[c]
02100000 - 02107FE3	BCSR0					
2100004 - 02107FE7	BCSR1					
2100008 - 02107FEB	BCSR2					
210000C - 02107FEF	BCSR3					
2100010 - 02107FF3	BCSR4					
02108000 - 021FFFFF	Empty Space					
02200000 - 02207FFF	MPC Internal MAP[d]					32
02208000 - 027FFFFF	Empty Space					
02800000 - 029FFFFF	Flash SIMM	MCM29F020	MCM29F040 SM732A1000A	MCM29F080 SM732A2000		32
02A00000 - 02BFFFFF						32
02C00000 - 02FFFFFF						32
03000000 - 037FFFFF	SDRAM[a]	(for 8MB)				32
03400000 - FFFFFFFF	Empty Space					

a. 0 - 0x007F_FFFF, 0x0300_0000 - 0x037F_FFFF are both mapped to SDRAM (8MB).
b. The device appears repeatedly in multiples of its size, e.g., BCSR0 appears at memory locations 2100000, 2100020, 2100040..., while BCSR1 appears at 2100004, 2100024, 2100044... and so on.
c. Only upper 16-bit (D0-D15) are used.
d. Refer to the relevant MPC User Manual for a complete description of the MPC internal memory map.

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TABLE 3-2. Memory Map in MPC852TADS Compatible Mode

ADDESS RANGE	*Memory Type*	*Device Type*				*Port Size*
00000000 - 003FFFFF	DRAM SIMM	MB321Bx[a]08	MB322Bx[a]08	MC324Cx[a]00	MB328Cx[a]00	32
00400000 - 007FFFFF						32
00800000 - 00FFFFFF						32
01000000 - 01FFFFFF						32

TABLE 3-2. Memory Map in MPC852TADS Compatible Mode

ADDESS RANGE	*Memory Type*	*Device Type*				*Port Size*
02000000 - 020FFFFF	Empty Space					
02000300 - 020003FF	Control Register					
02100000 - 02107FFF	BCSR(0:4)[b]					32[c]
02100000 - 02107FE3	BCSR0					
2100004 - 02107FE7	BCSR1					
2100008 - 02107FEB	BCSR2					
210000C - 02107FEF	BCSR3					
2100010 - 02107FF3	BCSR4					
02108000 - 021FFFFF	Empty Space					
02200000 - 02207FFF	MPC Internal MAP[d]					32
02208000 - 027FFFFF	Empty Space					
02800000 - 029FFFFF	Flash SIMM	MCM29F020	MCM29F040 SM732A1000A	MCM29F080 SM732A2000		32
02A00000 - 02BFFFFF						32
02C00000 - 02FFFFFF						32
03000000 - 037FFFFF	SDRAM (for 8MB)					32
03400000 - FFFFFFFF	Empty Space					

a. x Œ [B,T]
b. The device appears repeatedly in multiples of its size, e.g., BCSR0 appears at memory locations 2100000, 2100020, 2100040..., while BCSR1 appears at 2100004, 2100024, 2100044... and so on.
c. Only upper 16-bit (D0-D15) are used.
d. Refer to the relevant MPC User Manual for a complete description of the MPC internal memory map.

3•4 MPC Register Programming

The MPC offers the following functions on the MPC852TADS:

1) DRAM Controller
2) SDRAM Controller
3) Chip Select Generator
4) UART for terminal or host computer connection
5) Ethernet Controller
6) Fast Ethernet Controller
7) General Purpose I/O signals

OPERATING INSTRUCTIONS

The MPC internal registers must be programmed after Hard Reset. See the following paragraphs for descriptions. The addresses and programming values are in hexadecimal base. For more information and a better understanding of the below noted initialization, refer to the MPC866 User Manual.

TABLE 3-3. SIU REGISTER PROGRAMMING

Register	*Init Value[hex]*	*Description*
SIUMCR	01012440	Internal arbitration. External master arbitration priority - 0. External arbitration priority - 0. PCMCIA channel II pins - PCMCIA. Debug Port on JTAG port pins. FRZ/IRQ6~ - FRZ. Debug register - locked. No parity for non-CS regions. DP(0:3)/ IRQ(3:6)~ pins - DP(0:3). Reservation disabled. SPKROUT - Tri-stated. BS_A(0:3)~ and WE(0:3)~ are only driven on their dedicated pins. GPL_B5~ enabled. GPL_A/B(2:3)~ function as GPLs.
SYPCR	FFFFFF88	Software watchdog timer count - FFFF. Bus-monitor timing FF. Bus-monitor - Enabled. S/W watch-dog - Freeze. S/W watch-dog - disabled. S/W watch-dog (if enabled) causes NMI. S/W (if enabled) not prescaled.
TBSCR	00C2	No interrupt level. Reference match indications cleared. Interrupts disabled. No freeze. Time-base disabled.
PISCR	0082	No level for interrupt request. Periodic interrupt disabled. Clear status. Interrupt disabled. FREEZE. Periodic timer disabled.

3•4•1 Memory Controller Registers Programming

The MPC852TADS memory controller is initialized for 66 MHz operation. For example, register programming is based on a 66 MHZ timing calculation; an exception being the refresh timer that is initialized for 16.67Mhz. The latter is the lowest frequency at which the ADS may begin to operate. The ADS may be made to *wake-up* at 25MHz[A] but with inefficient initialization for there are too many wait-states inserted. As a consequence, an additional set of initialization is provided in order to support an effective 25MHz operation.

The ADS is initialized at 66Mhz in order to allow for a proper, though not efficient, ADS operation via all available ADS clock frequencies.

A. The refresh rate parameter is the only one initialized to the start-up frequency. Initialization to 66Mhz would have been inadequate for a board is running at a lower frequency. Thus, for the best bus bandwidth availability, the refresh rate should be adapted to the current system clock frequency.

OPERATING INSTRUCTIONS

Warning

Due to availability problems with several of the supported memory components, the initialization noted below were not tested with all the parts. Consequently, these initialization may CHANGE during the course of the testing period.

TABLE 3-4. Memory Controller Initialization For 66Mhz with DRAM-EDO

Register	*Device Type*	*Init Value [hex]*	*Description*
BR0	All Flash SIMMs supported.	02800001	Base at 2800000, 32-bit port size, no parity, GPCM
OR0	MCM29F020-90	FFE00D34	2MB block size, all types access, CS early negate, 6 w.s., timing relax
	MCM29F040-90 SM732A1000A-9	FFC00D34	4MB block size, all types access, CS early negate, 6 w.s., timing relax
	MCM29F080-90 SM732A2000-9	FF800D34	8MB block size, all types access, CS early negate, 6 w.s., timing relax
	MCM29F020-12	FFE00D44	2MB block size, all types access, CS early negate, 8 w.s., timing relax
	MCM29F040-12 SM732A1000A-12	FFC00D44	4MB block size, all types access, CS early negate, 8 w.s., timing relax
	MCM29F080-12 SM732A2000-12	FF800D44	8MB block size, all types access, CS early negate, 8 w.s., timing relax
BR1	BCSR	02100001	Base at 2100000, 32-bit port size, no parity, GPCM
OR1		FFFF8110	32 KB block size, all types access, CS early negate, 1 w.s.
BR2	All DRAM SIMMs supported	00000081	Base at 0, 32-bit port size, no parity, UPMA
OR2	MCM36100/200-60/70	FFC00800	4MB block size, all types access, initial address multiplexing according to AMA.
	MCM36400/800-60/70 MT8/16D432/832X-6/7	FF000800	16MB block size, all types access, initial address multiplexing according to AMA.
BR3	MCM36200-60/70	00400081	Base at 400000, 32-bit port size, no parity, UPMA
	MCM36800-60/70 MT16D832X-6/7	01000081	Base at 1000000, 32-bit port size, no parity, UPMA
OR3	MCM36200-60/70	FFC00800	4MB block size, all types access, initial address multiplexing according to AMA
	MCM36800-60/70 MT16D832X-6/7	FF000800	16MB block size, all types access, initial address multiplexing according to AMA.

TABLE 3-4. Memory Controller Initialization For 66Mhz with DRAM-EDO

Register	*Device Type*	*Init Value [hex]*	*Description*
BR4 Compatible Mode	K4S643232-TC60	030000C1	Base at 3000000, on UPMB
OR4 Compatible Mode		FFC00800	4 MB block size, all types access, initial address multiplexing according to AMB.
MPTPR	All Dram SIMMs supported	0400	Divide by 16 (decimal)
MAMR	MB321BT08TASN60	40A21114[a] 60A21114[b] C0A21114[c]	Refresh clock divided by 40[a] or 60[b] or C0[c]. Periodic timer enabled. Type 2 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB322BT08TASN60	20A21114[a] 30A21114[b] 60A21114[c]	Refresh clock divided by 20[a] or 30[b] or 60[c]. Periodic timer enabled. Type 2 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB324CT00TBSN60	40B21114[a] 60B21114[b] C0B21114[c]	Refresh clock divided by 40[a] or 60[b] or C0[c]. Periodic timer enabled. Type 3 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB328CT00TBSN60	20B21114[a] 30B21114[b] 60B21114[c]	Refresh clock divided by 20[a] or 30[b] or 60[c]. Periodic timer enabled. Type 3 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
MBMR	KS643232C-TC60	D0802114[c] 80802114[d]	Refresh clock divided by D0 or 80. Periodic timer enabled. Type 0 address multiplexing scheme. 2 cycle disable timer. GPL4enabled. 1 loop read. 1 loop write. 4 beats refresh burst.

a. Assuming 16.67 MHz BRGCLK.
b. Assuming 25MHz BRGCLK
c. For 66MHz BRGCLK
d. Assuming 32MHz BRGCLK.

TABLE 3-5. Memory Controller Initialization For 66Mhz with No DRAM-EDO

Register	*Device Type*	*Init Value [hex]*	*Description*
BR0	All Flash SIMMs supported.	02800001	Base at 2800000, 32-bit port size, no parity, GPCM
OR0	MCM29F020-90	FFE00D34	2MB block size, all types access, CS early negate, 6 w.s., timing relax
	MCM29F040-90 SM732A1000A-9	FFC00D34	4MB block size, all types access, CS early negate, 6 w.s., timing relax
	MCM29F080-90 SM732A2000-9	FF800D34	8MB block size, all types access, CS early negate, 6 w.s., timing relax
	MCM29F020-12	FFE00D44	2MB block size, all types access, CS early negate, 8 w.s., timing relax
	MCM29F040-12 SM732A1000A-12	FFC00D44	4MB block size, all types access, CS early negate, 8 w.s., timing relax
	MCM29F080-12 SM732A2000-12	FF800D44	8MB block size, all types access, CS early negate, 8 w.s., timing relax
BR1	BCSR	02100001	Base at 2100000, 32-bit port size, no parity, GPCM
OR1		FFFF8110	32 KB block size, all types access, CS early negate, 1 w.s.
BR2	All Dram SIMMs supported	00000080	Invalid bank
OR2	MCM36100/200-60/70	FFC00800	Invalid bank
	MCM36400/800-60/70 MT8/16D432/832X-6/7	FF000800	
BR3	MCM36200-60/70	00400080	Invalid bank
	MCM36800-60/70 MT16D832X-6/7	01000080	Invalid bank
OR3	MCM36200-60/70	FFC00800	Invalid bank
	MCM36800-60/70 MT16D832X-6/7	FF000800	Invalid bank
BR4 MPC86x New Mode	K4S643232-TC60	0x000000C1	Base at 0x0, on UPMB
OR4 MPC86x New Mode		0xFC800A00	4 MB block size, all types access, initial address multiplexing according to AMB.
MPTPR	All Dram SIMMs supported	0400	Divide by 16 (decimal)

TABLE 3-5. Memory Controller Initialization For 66Mhz with No DRAM-EDO

Register	*Device Type*	*Init Value [hex]*	*Description*
MAMR	MB321BT08TASN60	40A21114[a] 60A21114[b] C0A21114[c]	Refresh clock divided by 40[a] or 60[b] or C0[c]. Periodic timer enabled. Type 2 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB322BT08TASN60	20A21114[a] 30A21114[b] 60A21114[c]	Refresh clock divided by 20[a] or 30[b] or 60[c]. Periodic timer enabled. Type 2 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB324CT00TBSN60	40B21114[a] 60B21114[b] C0B21114[c]	Refresh clock divided by 40[a] or 60[b] or C0[c]. Periodic timer enabled. Type 3 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB328CT00TBSN60	20B21114[a] 30B21114[b] 60B21114[c]	Refresh clock divided by 20[a] or 30[b] or 60[c]. Periodic timer enabled. Type 3 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
MBMR	KS643232C-TC60	D0802114[c] 80802114[d]	Refresh clock divided by D0 or 80. Periodic timer enabled. Type 0 address multiplexing scheme. 2 cycle disable timer. GPL4 enabled. 1 loop read. 1 loop write. 4 beats refresh burst.

a. Assuming 16.67 MHz BRGCLK.
b. Assuming 25MHz BRGCLK
c. For 66MHz BRGCLK
d. Assuming 32MHz BRGCLK.

TABLE 3-6. UPMA Initialization for 60nsec DRAMs @ 66MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exceptions
Offset in UPM		0	8	18	20	30	3C
Contents @ Offset +	0	FFFFCC24	FFFFCC24	FFFFCC24	FFFFCC24	E0FFCC84	33FFCC07
	1	0FFFCC24	0FFFCC24	0FAFCC24	0FAFCC24	00FFCC04	FFFFFFFF
	2	0FFFCC04	0FFFCC04	0FAFCC04	0FAFCC04	00FFCC04	FFFFFFFF
	3	0CFFCC04	08FFCC04	08AFCC04	08AFCC00	0FFFCC04	FFFFFFFF
	4	00FFCC04	00FFCC04	00AFCC00	07AFCC4C	7FFFCC04	
	5	00FFCC00	00FFCC08	37FFCC47	08AFCC00	FFFFCC86	
	6	37FFCC47	0CFFCC44	FFFFFFFF	07AFCC4C	FFFFCC05	
	7	FFFFFFFF	00FFEC0C	FFFFFFFF	08AFCC00	FFFFFFFF	
	8		03FFEC00		07AFCC4C	FFFFFFFF	
	9		00FFEC44		08AFCC00	FFFFFFFF	
	A		00FFCC08		37AFCC47	FFFFFFFF	
	B		0CFFCC44		FFFFFFFF	FFFFFFFF	
	C		00FFEC04		FFFFFFFF		
	D		00FFEC00		FFFFFFFF		
	E		3FFFEC47		FFFFFFFF		
	F		FFFFFFFF		FFFFFFFF		

TABLE 3-7. Memory Controller Initialization For 20Mhz

Register	*Device Type*	*Init Value [hex]*	*Description*
BR0	All Flash SIMMs supported.	02800001	Base at 2800000, 32-bit port size, no parity, GPCM
OR0	MCM29F020-90	FFE00D20	2MB block size, all types access, CS early negate, 2 w.s.
	MCM29F040-90 SM732A1000A-9	FFC00D20	4MB block size, all types access, CS early negate, 2 w.s.
	MCM29F080-90 SM732A2000-9	FF800920	8MB block size, all types access, CS early negate, 2 w.s., timing relax
	MCM29F020-12	FFE00D30	2MB block size, all types access, CS early negate, 3 w.s.
	MCM29F040-12 SM732A1000A-12	FFC00D30	4MB block size, all types access, CS early negate, 3 w.s.
	MCM29F080-12 SM732A2000-12	FF800930	8MB block size, all types access, CS early negate, 3 w.s.
BR1	BCSR	02100001	Base at 2100000, 32-bit port size, no parity, GPCM
OR1		FFFF8110	32 KB block size, all types access, CS early negate, 1 w.s.
BR2	All Dram SIMMs supported	00000081	Base at 0, 32-bit port size, no parity, UPMA
OR2	MB321/2BT08TASN60	FFC00800	4MB block size, all types access, initial address multiplexing according to AMA.
	MB324/8CT00TBSN60	FF000800	16MB block size, all types access, initial address multiplexing according to AMA.
BR3[a]	MB322BT08TASN60	00400081	Base at 400000, 32-bit port size, no parity, UPMA
	MB328CT00TBSN60	01000081	Base at 1000000, 32-bit port size, no parity, UPMA
OR3	MB322BT08TASN60	FFC00800	4MB block size, all types access, initial address multiplexing according to AMA
	MB328CT00TBSN60	FF000800	16MB block size, all types access, initial address multiplexing according to AMA.
BR4 Compatible Mode	K4S643232-TC60	030000C1	Base at 3000000, on UPM B
OR4 Compatible Mode		FFC00A00	4 MB block size, all types access, initial address multiplexing according to AMB.

OPERATING INSTRUCTIONS

TABLE 3-7. Memory Controller Initialization For 20Mhz

Register	*Device Type*	*Init Value [hex]*	*Description*
BR4 MPC86x New Mode	K4S643232-TC60	0x000000C1	Base at 0x0, on UPM B
OR4 MPC86x New Mode		0xFC800A00	4 MB block size, all types access, initial address multiplexing according to AMB.
MPTPR	All Dram SIMMs supported	0400	Divide by 16 (decimal)
MAMR	MB321BT08TASN60	60A21114	Refresh clock divided by 60. Periodic timer enabled. Type 2 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB322BT08TASN60	30A21114	Refresh clock divided by 30. Periodic timer enabled. Type 2 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB324CT00TBSN60	60B21114	Refresh clock divided by 60. Periodic timer enabled. Type 3 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
	MB328CT00TBSN60	30B21114	Refresh clock divided by 30. Periodic timer enabled. Type 3 address multiplexing scheme. 2 cycle disable timer. GPL4 disabled for data sampling edge flexibility. 1 loop read. 1 loop write. 4 beats refresh burst.
MBMR	KS643232C-TC60	42802114[b]	Refresh clock divided by 42. Periodic timer enabled. Type 0 address multiplexing scheme. 2 cycle disable timer. GPL4 enabled. 1 loop read. 1 loop write. 4 beats refresh burst.

a. BR3 is not initialized for MB321xx or MB324xx EDO DRAM SIMMs.
b. Assuming 16.67MHz BRGCLK

TABLE 3-8. UPMA Initialization for 60nsec EDO DRAMs @ 20MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exceptions
Offset in UPM		0	8	18	20	30	3C
Contents @ Offset +	0	8FFFCC04	8FFFCC04	8FEFCC00	8FEFCC00	80FFCC84	33FFCC07
	1	08FFCC00	08FFCC08	39BFCC47	09AFCC48	17FFCC04	X
	2	33FFCC47	08FFCC08	X	09AFCC48	FFFFCC86	X
	3	X	08FFCC08	X	09AFCC48	FFFFCC05	X
	4	X	08FFCC00	X	39BFCC47	X	
	5	X	3FFFCC47	X	X	X	
	6	X	X	X	X	X	
	7	X	X	X	X	X	
	8		X		X	X	
	9		X		X	X	
	A		X		X	X	
	B		X		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

TABLE 3-9. UPMB Initialization for KS643232C-TC60 upto 32MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exceptions
Offset In UPM		0	8	18	20	30	3C
Contents @ Offset +	0	0126CC04	0026FC04	0E26BC04	0E26BC00	1FF5FC84	7FFFFC07
	1	0FB98C00	10ADFC00	01B93C00	10AD7C00	FFFFFC04	X
	2	1FF74C45	F0AFFC00	1FF77C45	F0AFFC00	FFFFFC84	X
	3	X	F1AFFC00	X	F0AFFC00	FFFFFC05	X
	4	X	EFBBBC00	X	E1BBBC04	X	
	5	1FE77C34[a]	1FF77C45	X	1FF77C45	X	
	6	EFAABC34	X	X	X	X	
	7	1FA57C35	X	X	X	X	
	8		X		X	X	
	9		X		X	X	
	A		X		X	X	
	B		X		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

a. MRS initialization uses free space.

TABLE 3-10. UPMB Initialization for KS643232C-TC60, 32+MHz - 50MHz

Cycle Type		Single Read	Burst Read	Single Write	Burst Write	Refresh	Exceptions
Offset In UPM		0	8	18	20	30	3C
Contents @ Offset +	0	1F07FC04	1F07FC04	1F27FC04	1F07FC04	1FF5FC84	7FFFFC07
	1	EEAEFC04	EEAEFC04	EEAEBC00	EEAEBC00	FFFFFC04	X
	2	11ADFC04	10ADFC04	01B93C04	10AD7C00	FFFFFC04	X
	3	EFBBBC00	F0AFFC00	1FF77C47	F0AFFC00	FFFFFC04	X
	4	1FF77C47	F0AFFC00	X	F0AFFC00	FFFFFC84	
	5	1FF77C34[a]	F1AFFC00	X	E1BBBC04	FFFFFC07	
	6	EFEABC34	EFBBBC00	X	1FF77C47	X	
	7	1FB57C35	1FF77C47	X	X	X	
	8		X		X	X	
	9		X		X	X	
	A		X		X	X	
	B		X		X	X	
	C		X		X		
	D		X		X		
	E		X		X		
	F		X		X		

a. MRS initialization uses free space.

4 - Functional Description

The design details of the various modules comprising the MPC852TADS are described in this chapter.

4•1 Reset & Reset - Configuration

The ADS has several reset sources:

1) Regular Power-On Reset
2) Manual Soft Reset
3) Manual Hard Reset
4) Host Hard Reset through on board command converter
5) MPC Internal Sources - see the appropriate Spec or U/M

4•1•1 Regular Power - On Reset

The power on reset to the MPC852T initializes the processor state after power up. A dedicated logic, using Seiko S-80828ANMP-EDR-T2, which is a voltage detector of 2.8V +/- 2%, asserts PORESET~ inputs to the MPC852T and for a period of ~500msec. This time period is long enough to cover also for the stabilization, of the VDDL power buses of the MPC852T, powered by different voltage regulators. It is assumed that the stabilization time for all linear regulators (see also 4•14 "Power" on page 63) is about the same.

Power On Reset may be generated manually as well by a dedicated push-button SW6.

4•1•2 Manual Soft Reset

A Soft Reset button has been provided in order to support application development in areas other than around the debug port and resident debuggers. Pressing the SW3 button asserts the SRESET* pin of the MPC and generates a Soft Reset sequence.

When SRESET~ is asserted to the MPC then the debug-port controller makes a Soft Reset configuration available to the MPC. See 4•1•6•3 "Soft Reset Configuration".

4•1•3 Manual Hard Reset

A Hard Reset button has been provided[A] in order to support application development in areas other than around the debug port. Pressing the SW3 Soft Reset button in conjunction with the SW2 ABORT button asserts the HRESET* line thus generating a HARD RESET sequence. In order to economize on board space the button sharing was developed. However, this does not in any way effect functionality.

When HRESET~ is asserted to the MPC then a Hard Reset configuration, via BCSR0, is made available. See 4•1•6•2 "Hard Reset Configuration" and TABLE 4-10. "BCSR0 Description".

4•1•4 Host Hard Reset through on board command converter[B]

Hardware Reset through on board Command Converter is implemented in Altera Logic.
When using Serial Transfer mode Reset should be send via DB3.
When using EPP transfer mode Reset should be send via nInit signal and then the Host computer should enter into

A. The Hard Reset button is not dedicated.
B. For FUTURE Use

EPP negotiation mode.

4•1•5 MPC Internal Sources

On-board reset logic drives, with open-drain gates, the MPC's HRESET* and SRESET* open-drain lines. Correct operation of the internal reset sources of the MPC facilitates. As a rule, an internal reset source asserts HRESET* and / or SRESET* for a 512 system clock time minimum. With the exception of the Debug-Port Soft / Hard Resets[A], it is beyond the scope of this document to describe all the internal reset sources.

4•1•6 Reset Configuration

During reset the MPC device samples the state of some external pins in order to determine operational modes and pin configurations. The MPC has 3 reset levels - each levels configurations are sampled:

1) Power-On Reset Configuration
2) Hard Reset Configuration
3) Soft Reset Configuration.

4•1•6•1 Power-On Reset Configuration

The power-on reset configuration is sampled prior to the external logic's negation of the PORESET. Included in this configuration are pins, MODCK(1:2), that determine the MPC clock operation mode. The MPC852TADS supports one clock modes:

1:6.5 PLL operation via an on-board clock generator.

In this mode MODCK(1:2) are driven with'10' during[B] power-on reset.

4•1•6•2 Hard Reset Configuration

When the RSTCONF* pin is asserted during a Hard Reset sequence, the MPC data bus is sampled in order to achieve the MPC's Hard Reset configuration. The reset configuration word is driven by the BCSR0 register whose defaults are set during power-on reset. The BCSR0 drives half of the configuration word, i.e. data bits D(0:15) wherein the reserved bits are designated as RSRVxx. It is possible to change[C] the Hard Reset configuration by rewriting the BCSR0 with new values. The configuration change becomes valid after Hard Reset has been applied to the MPC.

The RSTCONF* line on the ADS is always driven during Hard Reset. As consequent example being the MPC's internal Hard Reset configuration defaults become unusable.

The following system parameters act as the BCSR0 default address during power-on reset and, further, are characterized as being driven at Hard Reset.

1) Arbitration: internal arbitration is selected.
2) Interrupt Prefix: the internal default is the interrupt prefix at 0xFFF00000. It is overridden in order to provide an interrupt prefix, address 0, located within the DRAM.
3) Boot Disable: Boot is enabled.
4) Boot Port Size: a boot port size of 32-bit is selected.
5) Initial Internal Space Base: directly following Hard Reset the internal space is located at 0xFF000000.
6) Debug Pin Configuration: PCMCIA port B[D] pins become PCMCIA port B pins.

A. Debug-Port Soft / Hard Resets are part of the development system and therefore bear mentioning.
B. In the 1:6.5 PLL operation the HRESET~ line drives the MODCK lines longer.
C. With respect to the ADS's power-on defaults.

7) Debug Port Pin Configuration: Debug port pins are located on the JTAG port.

8) External Bus Division Factor: internal to external clock frequencies are selected at a ratio of 1:1.

4•1•6•3 Soft Reset Configuration

The SRESET* rising edge is used to configure the development port. Prior to the negation of SRESET*, the DSCK[A] is sampled in order to determine the debug mode enable / disable. After SRESET* negation, in the instance that the debug mode was enabled, DSCK is again sampled for debug mode entry / non-entry.

DSDI is used to determine the debug port clock mode. DSDI is sampled after the negation of SRESET*.

The debug port controller, via on board command converter, provides the Soft Reset configuration. Option exists for entering the debug mode directly.

4•2 Local Interrupter

Generated by a button, the ABORT (NMI) is the only external interrupt applied to the MPC via its interrupt controller. When pressed, NMI input to the MPC is asserted. This interrupt type is meant to support the use of resident debuggers made available to the ADS. MPC peripherals and the debug port generate all other MPC interrupts internally.

The IRQ0* line, routed as an NMI input, is driven by an open-drain gate in order to support external (off-board) NMI generation. In order that external hardware may also drive this line, it is mandatory that the IRQ0* be driven by an open-drain (or open-collector) gate.

4•3 Clock Generator

Clocking the MPC on the MPC852TADS is done by using 10MHz Clock Generator Y2 connected to an EXTCLK input. With 1:6.5 PLL mode (SW4[1-2] ='OFF,ON'), 66MHz of Clkout is achieved.

All MPC852TADS bus timings are referenced to the Clkout. Clkout signal drives all other clocks in the system, via necessary buffering.

Use is done with Crystal 3.3V zero delay buffer, which is connected to 4 outputs, very low output to output skew (< 250 ps) clock splitter - the CY2309ZC-1H, to split the load between all various clock consumers on board.

4•4 Buffering

The ADS is also meant to serve as a hardware development platform. As such, it is necessary to buffer the MPC from the local bus in order to avoid wasting its capacitive drive capability and, further, in order that the MPC remain available for off-board applications via the expansion connectors.

Buffers provide address and strobe lines while transceivers provide data. Since the capacitive load over DRAM address lines may[B] exceed 200 pF, the DRAM address lines are buffered separately. This is achieved with 74LVC buffers operated by 3.3V though 5V tolerant. The 74LVC buffer reduces board noise by reducing transition amplitudes. Additional reductions in noise and reflection are made when a series of resistors is placed over a DRAM address and strobe lines.

Data transceivers will open under two conditions: available access to a valid[C D] board address or during Hard Reset configuration[E]. Consequently data conflicts are avoided when the off-board memory is read - provided no mapping to a valid board address exists. Avoiding such errors is the responsibility of the user.

D. In cases where PCMCIA port B pins exist.

A. At Hard Reset DSCK is configured to reside on the BDM Debug port - P12 or in Altera logic, when using on board command converter.

B. Capacitive load is dependant on the DRAM SIMM's internal structure.

C. A valid address *being* one covered within a Chip-Select region.

D. Excepting SDRAM which is unbuffered.

E. Allows a configuration word, stored in Flash memory, to become active.

4•5 Chip - Select Generator

The MPC memory controller is used as a chip-select generator in order to access on-board[A] memories and reduce board area. The latter cuts costs, lessens power consumption and increases flexibility. Off-board application development may be enhanced by disabling memory modules (including the BCSRx) via BCSR1[B] in favour of an external memory connected via the expansion connectors. In this way, with the associated local memory disabled, a CS line may be used off-board via the expansion connectors.

Local data transceivers do not open when a particular CS region has been disabled via BCSR1. This avoids possible[C] contention over data lines.

TABLE 4-1. "MPC852TADS Chip-Select Assignment" outlines an MPC chip-select assignment for various ADS memories / registers:

TABLE 4-1. MPC852TADS Chip-Select Assignment

Chip Select:	*Assignment*
CS0*	Flash Memory
CS1*	BCSR
CS2*	DRAM Bank 1
CS3*	DRAM Bank 2[a]
CS4*	SDRAM
CS5*	Unused, user available
CS(6-7)*	Unused, user available

a. If existent.

4•6 DRAM

DRAM EDO is not supplied with the board. Users may place their own DRAM EDO on the U20 DRAM SIMM. The MPC852TADS can operate with 4 MB of 60nsec delay EDO DRAM SIMM. Support is provided for the following: 5V powered FPM / EDO DRAM SIMM configured as 1M X32 up to 2 X 4M X 32 with 60 nsec or 70nsec delay.

All DRAM configurations are supported via the Board Control & Status Register (BCSR). For example, DRAM size (4M to 32M) and delay (60 / 70 nsec) are read from BCSR2 and the associated registers (including the UPM) are programmed accordingly.

DRAM timing control is performed by the MPC's UPMA via the CS2 region or, in the instance of a dual-bank SIMM, via region CS3. For example, RAS and CAS signal generation is performed using UPMA under the following conditions: normal[D] access; refresh cycles; and, during necessary address multiplexing[E]. CS2* and CS3* signals are split to two in order to overcome the capacitive load on the DRAM SIMM RAS lines. Further, each is buffered from the DRAM.

The DRAM module may be enabled / disabled at any time by writing DRAMEN~ bit in the BCSR1. See TABLE 4-

A. Peripherals and off-board.
B. After removal, the BCSR cannot be accessed unless power is reapplied to the ADS.
C. Data line contention is avoided during read cycles.
D. *Normal* being, for example, Single Read, Single Write, Burst Read & Burst Write.
E. Address multiplexing must take into account support for narrower bus widths.

11. "BCSR1 Description".

Note: The DRAM is not populated on the board. As such users may populate their own DRAM in order to either expand memory or to run old SW that ran on the old MPC8xxFADS.

4•6•1 DRAM 16-Bit Operation

In order to enhance evaluation capabilities and achieve the *best fit* for application requirements, support is given to DRAM's with 16-bit and 32-bit data bus widths. A DRAM in 16-bit mode is only 50% in use. For example, only the memory portion connected to data lines D(16:31) is in use.

To configure the DRAM for a 16-bit data bus width operation, the following steps should be taken:

1) Set the Dram_Half_Word bit in BCSR1 to Half-Word. See TABLE 4-11. "BCSR1 Description".
2) The Port size bits of BR2~ (and of BR3~ for a 2-bank DRAM SIMM) should be set to 16-bits.
3) The AM bits in the OR2 register should be set to **half** of the nominal **single-bank** DRAM SIMM volume or to a **quarter** of the nominal **dual-bank** DRAM SIMM volume.

If a dual-bank DRAM SIMM is being used then perform the following:

4) If a contiguous DRAM block is required then set the base-address bits in the BR3 register to DRAM_BASE plus a **quarter** Nominal_Volume.
5) The AM bits of the OR3 register should be set to a **quarter** of the Nominal_Volume.

If the above noted steps (1-5) are executed from a running code then, during execution, this code shouldn't reside on the DRAM for potentially erratic behavior may result in a system crash.

4•6•2 DRAM Performance Figures

Projected DRAM performance figures are shown in TABLE 4-2. "Regular DRAM Performance Figures" and in

TABLE 4-3. "EDO DRAM Performance Figures".

TABLE 4-2. Regular DRAM Performance Figures

	Number of System Clock Cycles			
System Clock Frequency [MHz]	*50*		*25*	
DRAM Delay [nsec]	*60*	*70*	*60*	*70*
Single Read	6	6	3	4
Single Write	4	4	3	3
Burst Read	6,2,3,2	6,3,2,3	3,2,2,2	4,2,2,2
Burst Write	4,2,2,2	4,2,2,2	3,1,2,2	3,2,2,2
Refresh	21[a b]	25[a b]	13[a b]	13[a b]

a. Four-beat refresh burst.
b. Doesn't include arbitration overhead.

TABLE 4-3. EDO DRAM Performance Figures

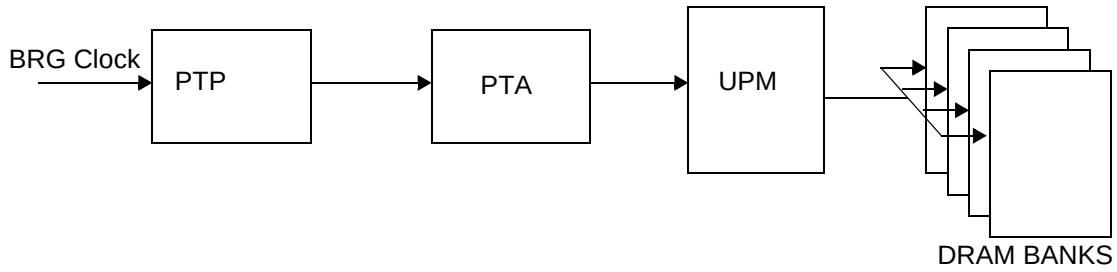
	Number of System Clock Cycles			
System Clock Frequency [MHz]	*50*		*25*	
DRAM Delay [nsec]	*60*	*70*	*60*	*70*
Single Read	6	6	3	4
Single Write	4	4	2	3
Burst Read	6,2,2,2	6,3,2,2	3,1,1,1	4,1,2,2
Burst Write	4,2,2,2	4,2,2,2	2,1,1,1	3,2,2,2
Refresh	21[a b]	25[a b]	13[a b]	13[a b]

a. Four-beat refresh burst.
b. Doesn't include arbitration overhead.

4•6•3 Refresh Control

Prior to a RAS refresh, the DRAM refresh is CAS. The refresh is controlled by UPMA. Refresh logic is clocked by the MPC's BRG clock. The latter is not influenced by the MPC's low-power divider.

FIGURE 4-1 Refresh Scheme



As seen in FIGURE 4-1 above, the BRG clock is divided twice. Once by the PTP (Periodic Timer Prescaler) and thereafter by another prescaler, the PTA (Periodic Timer A), with its dedicated UPM. When there is more than one DRAM bank then refresh cycles are performed for consecutive banks resulting in faster refreshes. Below is the PTA formula calculation:

$$PTA = \frac{Refresh\_Period \times Number\_Of\_Beats\_Per\_Refresh\_Cycle}{Number\_Of\_Rows\_To\_Refresh \times T\_BRG \times MPTPR \times Number\_Of\_Banks}$$

Where:

- PTA: Periodic Timer A filed in MAMR. The value of the second divider.
- Refresh_Period: time (usually in msec) required to refresh a DRAM bank.
- Number_Of_Beats_Per_Refresh_Cycle: using the UPM looping capability, more than one refresh cycle per refresh burst (up to 16) may be performed.
- Number_Of_Rows_To_Refresh: number of rows in a DRAM bank.
- T_BRG: cycle time of the BRG clock.
- MPTPR: value of the PTP or Periodic Timer Prescaler (2 to 64).
- Number_Of_Banks: number of DRAM banks to refresh.

As an example, a MCM36200 SIMM has the following data:

- Refresh_Period == 16 msec.
- Number_Of_Beats_Per_Refresh_Cycle: 4 on the ADS.
- Number_Of_Rows_To_Refresh == 1024.
- T_BRG == 20 nsec (system clock @ 50 Mhz).
- MPTPR: arbitrarily chosen to be 16.
- Number_Of_Banks == 2 for that SIMM

If these figures are assigned to the PTA formula then the PTA value should be 97 decimal or 61 hex.

4•6•4 Variable Bus-Width Control

Port width determines address line connection schemes. The number of address lines required for byte-selection varies according to port width (1 for 16-bit port and 2 for 32-bit port) thus address connections to a memory port must be changed if the width is changed. For example, a memory initially configured as a 32-bit port will have a list significant (LS) address line connected to both the memory's A0 line and the MPC's A29 line. If the port is reconfigure as a 16-bit port then the MPC's LS address line becomes A30.

To maintain a linear[A] address scheme, all address lines connected to a memory must shift one bit. This shift involves

extensive multiplexing (passive or active). If a linear addressing scheme is not mandatory then only minimal multiplexing is required in order to support variable port widths.

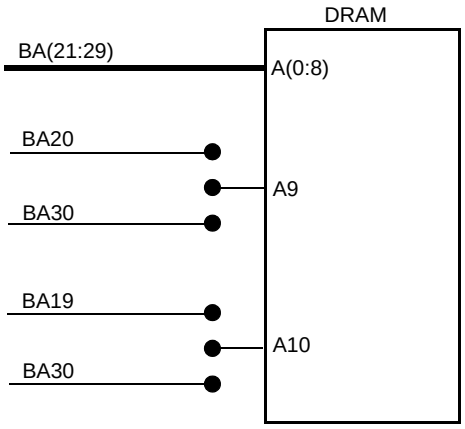
In TABLE 4-4. below, the ADS DRAM address connection scheme is presented:

TABLE 4-4. DRAM ADDRESS CONNECTIONS

Width	*32 - Bit*		*16 - Bit*	
	Depth		*Depth*	
DRAMADD	*4 M*	*1 M*	*4 M*	*1 M*
A0	BA29	BA29	BA29	BA29
A1	BA28	BA28	BA28	BA28
A2	BA27	BA27	BA27	BA27
A3	BA26	BA26	BA26	BA26
A4	BA25	BA25	BA25	BA25
A5	BA24	BA24	BA24	BA24
A6	BA23	BA23	BA23	BA23
A7	BA22	BA22	BA22	BA22
A8	BA21	BA21	BA21	BA21
A9	BA20	BA20	BA20	BA30
A10	BA19		BA30	

The above table shows that the majority of address lines remain fixed. Only two lines (shaded cells) required switching. In FIGURE 4-2 "DRAM Address Line Switching Scheme" the noted switches are implemented by active multiplexers controlled by the BCSR1/Dram_Half_Word* bit.

FIGURE 4-2 DRAM Address Line Switching Scheme



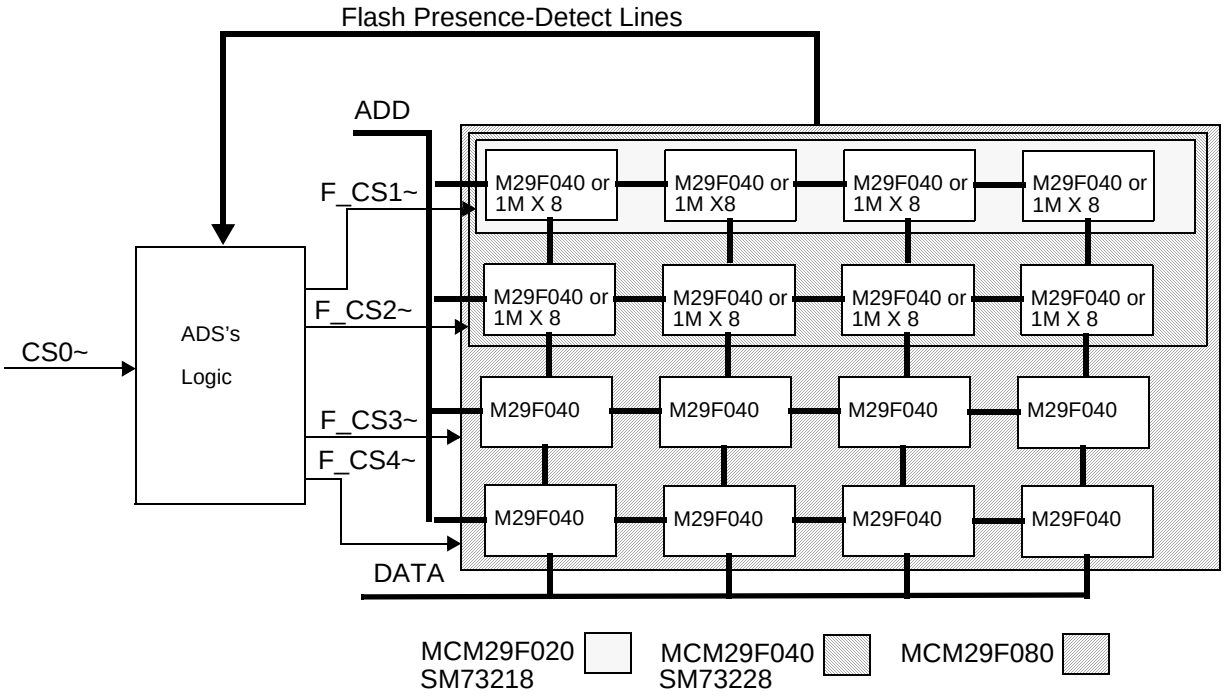
A. Resultant addresses lead to adjacent memory cells.

4•7 Flash Memory SIMM

The MPC852TADS has 2MB of 90 nsec Flash Memory SIMM or, more specifically, Motorola's MCM29020. In addition to Motorola's MCM29020, support is also provided for the following Smart Technology products: 4MB MCM29F040, 8 MB MCM29F080, 4 MB SM73218 and 8 MB SM73228. A Motorola SIMM is composed of one, two or four banks of four Am29F040 compatible devices. A Smart Technology SIMM is comprised of one or two banks of four 28F008 Intel devices. The Flash SIMM resides on an 80 pin SIMM socket.

To minimize MPC chip-select line usage only one chip-select line (CS0~) is used in order to select the Flash Memory as a whole. The distribution of chip-select lines, amongst the internal banks, is done via on-board programmable logic. The latter is achieved according to the Presence-Detect lines of the ADS's Flash SIMM.

FIGURE 4-3 Flash Memory SIMM Architecture



The ADS Flash Memory access time is 90 nsec although 120 nsec devices are also suitable. Via OR0, the debugger establishes the correct number of wait-states for a 66MHz system clock frequency by reading the delay section of the Flash SIMM Presence-Detect lines.

A Motorola SIMM is built from 5V programmable AMD Am29F0X0 devices. As such, there is no need for external programming voltage and the Flash may be written[A] as a regular memory.

Smart Technology parts, however, require that 12V ± 0.5% programming voltage be applied during programming. If on-board programming of these devices is required then a 12V supply must be connected to the ADS (P13). However, during normal[B] Flash operations a 12V supply is not required.

Flash control is achieved using both the GPCM and a dedicated CS0~ region with complete bank control. During Hard Reset initialization the debugger reads the Flash Presence-Detect lines via BCSR2 and, thereafter, concludes how to program the BR0 & OR0 registers. It is within these registers that a regions size and delay are determined.

Flash memory performance is outlined below in TABLE 4-5.

A. A manufacturer specific dedicated programming algorithm should be implemented during Flash programming.
B. For example, *read only* is an example of a *normal* operation.

:

TABLE 4-5. Flash Memory Performance Figures

	Number of System Clock Cycles			
System Clock Frequency [MHz]	*50*		*25*	
Flash Delay [nsec]	*90*	*120*	*90*	*120*
Read / Write[a] Access [Clocks]	8	10	4	5

a. Table figures refer to actual write access. Write operations continue internally and the device has to be polled for operation completion.

The Flash module may be disabled / enabled at any time by writing of'1' /'0' in the FlashEn~ bit in BCSR1.

4•8 Synchronous DRAM

Performance is enhanced, particularly at higher operation frequencies, by the board's 8 MB of SDRAM. The SDRAM is unbuffered from the MPC bus and then configured as 4 X 512K X 32 with Micron (or compatible) MT48LC2M32B2 chips. Removing buffers eliminates the delay associated with address and data buffers. Due to the fact that only one memory chip is involved, overall system performance is not affected.

The SDRAM doesn't reside on a SIMM, rather it is soldered directly to the ADS pcb. The SDRAM may be enabled / disabled at any time by writing'1' /'0' to the SDRAM bit in BCSR1. See TABLE 4-11. "BCSR1 Description" on page 54.

SDRAM timing is controlled by the UPMB via its assigned CS line. See TABLE 4-1. "MPC852TADS Chip-Select Assignment" on page 37. Unlike a regular DRAM, the synchronous DRAM has CS input in addition to RAS and CAS signals.

The SDRAM connection scheme is shown in FIGURE 4-4 on page 46 and the performance figures are available in TABLE 4-8. on page 45.

The selected SDRAM has 2048 rows and 256 columns thus necessitating eleven row and eight column address lines. TABLE 4-6. on page 44 below suggests a *glueless* interface between an MPC852T and the SDRAM. In the case of a 32-bit bus, one 32-bit SDRAM device is connected. Control is driven by the UPMB on the MPC852T thus the SDRAM's CS is interfaced to CS4 on the MPC852T. Any chip-select line that excludes CS0 is suitable. A utilized SDRAM device's DQM signals select byte lanes and connect to the appropriate MPC852T Byte Strobe (BS0:3) signals. A10 SD connects to GPL0 as it has the functionality to either drive an address on the line or define a level. This is required for A10 SD acts as both an address line and a control line. RAS and CAS are generated by GPL1 and GPL2 respectively. The WE is generated by GPL3. CLK is driven by the MPC852T's CLKOUT signal, a reference point with respect to the MPC852T's Memory Controller. The BS lines are connected to MPC lines A10 and A9 and are used as high order address bits. Note in the table below that the numbering scheme of the MPC852T address lines

differs from those of the SDRAM when address line mapping for 32-bits is being read.

TABLE 4-6. SDRAM ADD and MPC852T Pin Correlations

MPC8xx	*SDRAM*
A9, A10	BS1, BS0
A11:A21	11 ROW
A22:A29	8 Column

MPC address bits A11:21 are mapped to MPC lines A19:29 as row addresses via the UPM Register AMx =0b000. Starting with the MPC line A21 connection to A8 SD and MPC A20 to A9 SD, it is necessary to provide for the leftover row address A10 SD. This is not done through use of MPC line A19 as that would show MPC A10 as a multiplexed row address but, rather, as described above by using GPL0. In the UPM Register MxMR the GPL0 is programmed to show MPC A10 with complete row addressing.

In this case the SDRAM device has four banks. On occasion, a single 32-bit SDRAM bank does not provide enough application memory. Connecting multiple 32-bit SDRAM-based banks to the MPC852T is fairly straightforward as is extending the above noted interface.

The most significant row address bit, MPC BS SD.A10, is connected due to the 19-bit address size (8/11 address multiplex!) covered by the selected SDRAM device. SDRAM devices with two BS lines, BS0 SD and BS1 SD, must use the next address bit, e.g. MPC A10, A9 in order to keep the memory mapping linear. All in all, address lines are used for binary encoding of the bank selection.

TABLE 4-7. SDRAM - MPC Connections

MPC Output ADD	*SDRAM ADD*	*MPC Internal Column ADD*	*MPC Internal Row ADD*	
A29	A0	A29	A21	
A28	A1	A28	A20	
A27	A2	A27	A19	
A26	A3	A26	A18	
A25	A4	A25	A17	
A24	A5	A24	A16	
A23	A6	A23	A15	
A22	A7	A22	A14	
A21	A8		A13	
A20	A9		A12	
GPL0	A10 (AP)		A11	
A10 Note1	NC(A11)			
A10 / A9 Note1	BS0		A10	
A9 / A8 Note 1	BS1		A9	

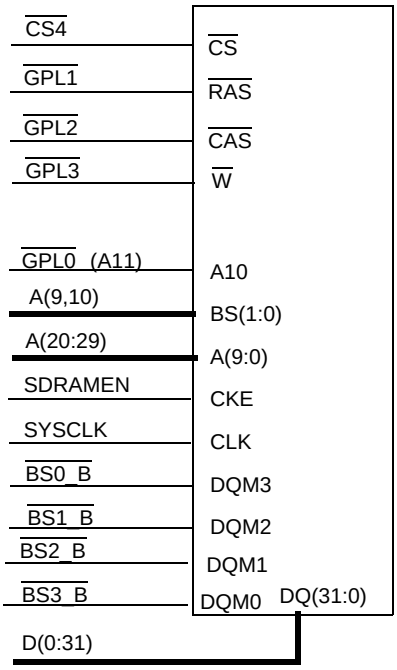
Note: If users want a larger SDRAM via a 16M A11 connection to A10 then note that this connection is existent in the board layout. Users must connect BS0, BS1 to MPC ADD A9 & A8. This is achieved by removing R31, R28 resistors and assemble R30, R29.

TABLE 4-8. Estimated SDRAM Performance Figures

	Number of System Clock Cycles	
System Clock Frequency [MHz]	*50*	*25*[a]
Single Read	5	3
Single Write	3+1[b]	2 + 1[b]
Burst Read	5,1,1,1	3,1,1,1
Burst Write	3,1,1,1 + 1[b]	2,1,1,1 + 1[b]
Refresh	21 [c]	13 [b]

a. Up to 32MHz.
b. One additional cycle for RAS precharge.
c. Four-beat refresh burst doesn't include arbitration overhead.

FIGURE 4-4 SDRAM Connection Scheme



4•8•1 SDRAM Programming

To establish the SDRAM's mode of operation it must, after power-up, be initialized by means of programming. The programming is undertaken by issuing a Mode Register Set command that passes data along the SDRAM address lines to the Mode Register. The UPM fully supports the noted command by means of a dedicated Memory Address Register as well as the UPM command run option. Mode Register programming values are shown in TABLE 4-9. "SDRAM Mode Register Programming".

In order to operate the SDRAM at speeds higher than 66Mhz read the application note at **http://e-www.motorola.com/brdata/PDFDB/docs/AN2066.pdf** and, further, refer to both the MPC860COD09 MPC860 UPM Programming Tool - UPM860 and the MPC860COD10 UPM860 Manual for MPC860 UPM Programming Tool found on the following web page, **http://e-www.motorola.com/webapp/sps/site/prod_summary.jsp?code=MPC860&nodeId=01M98657**.

TABLE 4-9. SDRAM Mode Register Programming

	Value @ Frequency	
SDRAM Option	*50MHz*	*25MHz*
Burst Length	4	4
Burst Type	Sequential	Sequential
CAS Latency	2	1
Write Burst Length	Burst	Burst

4•8•1•1 SDRAM Initializing Procedure

Following power-up, the SDRAM needs to be initialized in the manner outlined below:

1) Program the UPMB with the values noted in TABLE 3-9. "UPMB Initialization for KS643232C-TC60 upto 32MHz" on page 32 or in TABLE 3-10. "UPMB Initialization for KS643232C-TC60, 32+MHz - 50MHz" on page 33.
2) Program the Memory Controller (MPTPR, MBMR, OR4 and BR4) registers as per TABLE 3-7. "Memory Controller Initializations For 20Mhz" on page 29 or TABLE 3-4. "Memory Controller Initialization For 66Mhz with DRAM-EDO" on page 24.
3) Set the MAR to the correct value (0x48 for up to 32MHz or 0x88 for 32-50 MHz).
4) Run the MRS command, programmed in locations five to eight of the UPMB, by writing the MCR with 0x80808105.
5) Change the MBMR TLFB field to eight in order to maintain 8-beat refresh bursts.
6) Run the refresh sequence (8 refresh cycles being performed) by writing the MCR with 0x80808130.
7) Restore the MBMR TLFB field to four in order to provide the 4-beat refresh bursts of normal operation.
8) The SDRAM is now initialized and ready for operation.

4•8•2 SDRAM Refresh

Refresh the SDRAM by using its auto-refresh mode. For example, the UPMB periodic timer issues a burst of four auto-refresh commands to the SDRAM every 62.4 msec. As a result, all 2048 SDRAM rows are refreshed within a specific 32.8 msec slot.

4•9 Communication Ports

The ADS board contains all the modules that could possibly be configured on the MPC852T. The various communication ports are noted below:

- SMC1,SCC3 - RS232
- SCC4 Ethernet
- FETHC - Fast Ethernet Controller on Port - D
- PCMCIA Controller

4•9•1 RS232 Ports

The ADS has two identical RS232 ports for both assisting with user applications and as a means of providing convenient communication channels between terminal and host computers. The MPC type determines the MPC communication ports to which the RS232 ports are routed. The MAX3241ECAI transceivers, equipped with OE and shutdown mode, are used to generate RS232 levels internally through use of a single 3.3V power supply. When the $\overline{\text{RS232EN1}}$ or $\overline{\text{RS232EN2}}$ bits in BCSR1 are asserted (low) then the associated transceiver is enabled. When negated, the associated transceiver enters a standby mode characterized by tri-stated receiver outputs, that enables off-board use of the associated port's pins via the expansion connectors.

A female Dual port, 9-pin each, D-Type stacked connector is configured for direct connection (via a flat cable) to a standard IBM-PC compatible RS232 connector.

4•9•1•1 RS232 Port Signal Descriptions

The direction','I/O', is relative to the ADS board. For example,'I' signifies ADS input.

- CD (O): Data Carrier Detect - the ADS always asserts this line.
- TX (O): Transmit Data
- RX (I): Receive Data
- DTR (I): Data Terminal Ready - ADS software may use this signal to detect whether a terminal is connected to the ADS board.
- DSR (O): Data Set Ready - the ADS always asserts this line.
- RTS (I): Request To Send - in the ADS this line is not connected.
- CTS (O): Clear To Send - the ADS always asserts this line.

4•9•2 Ethernet Port

The MPC852TADS has an Ethernet port with T.P. 10-Base-T I/F connected to SCC4.

Use is done by Davicom DM9161E. The initial configuration of the DM9161E on the MPC852TADS is set by external resistors to 10Base-T GPSI 7-Wired mode.

The DM9161E is able to interrupt the MPC via IRQ3 line.

Ethernet SCC4 pins are located at the expansion connectors in order to allow for alternative usage of the board's port expansion connector P2.

4•9•3 FETHC - Fast Ethernet Controller on Port - D

Fast Ethernet port with T.P. 100-Base-T I/F is provided on the MPC852TADS. These port also support 10 Mbps

ethernet (10-Base-T) via the same transceiver - the DM9161E by Davicom.

The DM9161E are connected to Port D via MII interface. The initial configuration of the DM9161E on the MPC852TADS is set by external resistors to 100Base-T Full Duplex in MII mode.

The DM9161E reset input is driven by either asserting the RSTMII bit in BCSR4 (see TABLE 4-20.) or by asserting a specific bit in an internal register via MII I/F.

To allow external use of Port D, their pins appear at the expansion connectors and the ethernet transceiver may be Disabled / Enabled at any time via the MIIs' MDIO port or via MIIRXEN bit in BCSR4.

The DM9161E is able to interrupt the MPC via IRQ6 line.

4•9•3•1 DM9161E Control

The DM9161E is controlled via 2 wire interface: a clock (MDC) and a bidirectional data line (MDIO). This is in fact a bus, i.e., up to 32 devices may reside over it, while the protocol defines a 5-bit slave address field, which is compared against the slave address set to each device by hardware during device reset, according to the levels on some pins. On the board, the slave address is hard-set to b00000 for Fast Ethernet and b00011 for Ethernet. The MPC interfaces this port using two PI/O pins: MII_MDIO for MDIO and PD12/MIIMDC for MDC. There is no special support within the MPC for the MDIO port and the protocol is implemented in S/W.

The MDIO port may interrupt a host in 2 ways: (a[A]) driving low the MDIO line during IDLE time or (b) using a dedicated interrupt line $\overline{\text{MDINT}}$. This line is connected to the MPC's IRQ6 line in Fast Ethernet I/F and IRQ3 line in Ethernet I/F, appearing also at the expansion connectors.

4•10 PCMCIA Port

To enhance PCMCIA I/F development, the ADS has a dedicated PCMCIA port. Support is only provided to 5V PC-Cards that are PCMCIA standard 2.1+ compliant. The MPC generates all necessary control signals. To both protect MPC signals from external hazards and to provide sufficient drive capability, a set of buffers and latches is provided over the PC-Card address, data and strobe lines.

To conform with the ADS design spirit, such as maximizing the number of available MPC resources available for external application development, input buffers are provided for input control signals. The buffers are controlled by the PCC_EN~ bit in BCSR1 and by writing'1' /'0' to PCMCIA port that may be Disabled / Enabled at any time. If the PCMCIA channel has been disabled then its associated pins become available for off-board use via the expansion connectors.

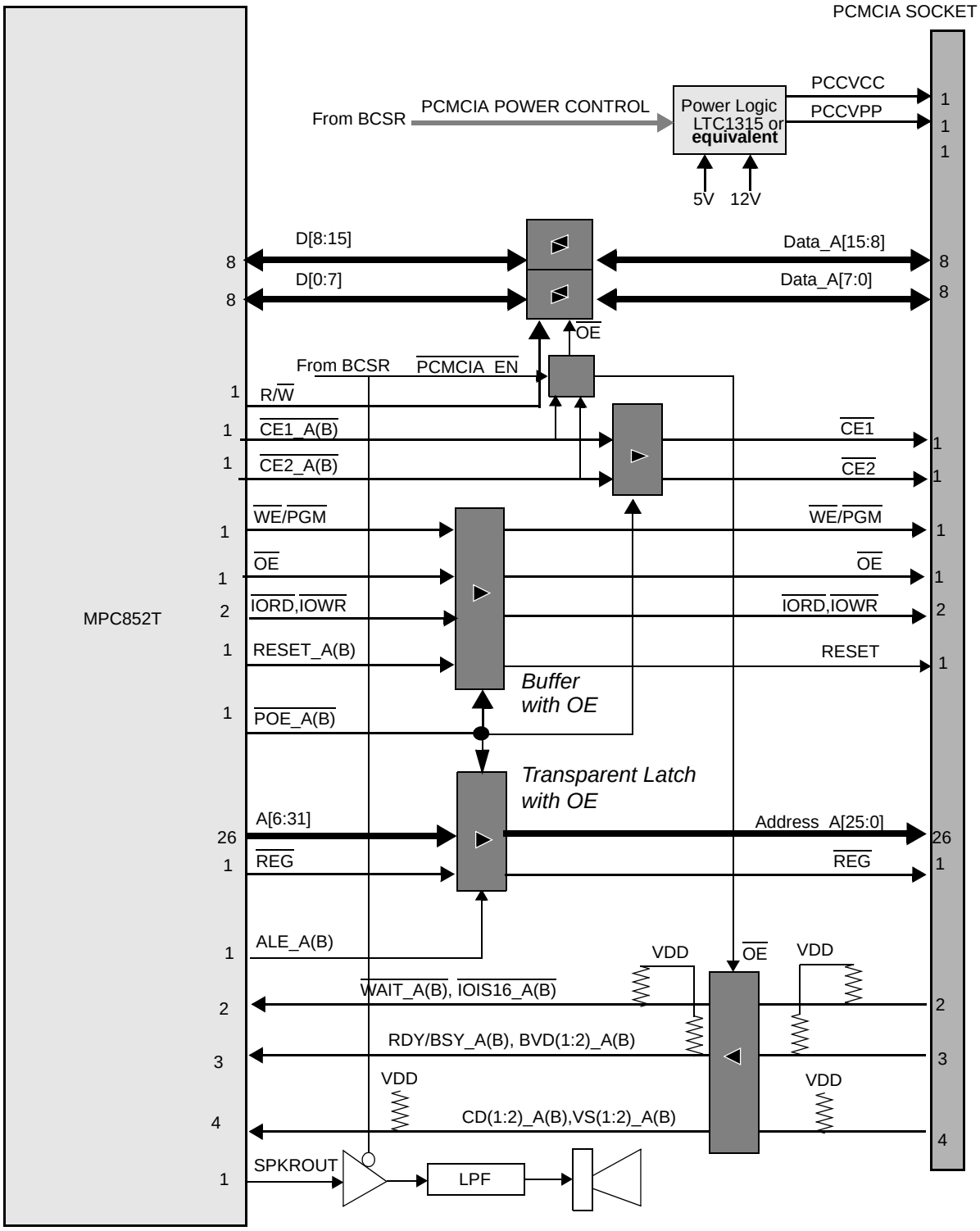
The board has a loudspeaker that is connected to the MPC's SPKROUT line. The loudspeaker is buffered from the MPC and low-pass filtered. When the PCC_EN~ bit in BCSR1 is negated (high) then the loudspeaker buffer is tri-stated so the SPKROUT signal of the MPC may be used for an alternate function.

It is not recommended [B] to apply control signals to an unpowered PC-Card as the strobe / data signal buffers / transceivers are tri-stated and may only be driven when a PC-Card is powered.

FIGURE 4-5 "PCMCIA Port Configuration" on page 50 illustrates a block diagram of the PCMCIA port.

A. Not supported on the board.
B. If the PC-Card has protection diodes on its inputs then they will force down any input signals regardless of their driven level.

FIGURE 4-5 PCMCIA Port Configuration



4•10•1 PCMCIA Power Control

In order to support hot-insertion[A], socket power is controlled via LINEAR TECHNOLOGY's LTC1315 dedicated PCMCIA power controller. The LTC1315, through which the PC Card VCC is switched, switches 12V VPP's for the purpose of card programming as well as gate control of external MOSFET transistors. The LTC1315 is controlled by BCSR1.

If, for example, a PC Card is inserted while the PCMCIA channel is enabled via BCSR1 then both of the CD(1:2)* (Card Detect) lines are asserted (low). Thereafter, read the voltage select lines VS(1:2)* status to determine the PC Card's operation voltage level accordingly to which PCCVCC(0:1) bits in BCSR1 should be set in order to drive the correct VCC (5V) to the PC-Card.

If a PC Card is removed from the socket, while the channel is enabled via BCSR1, the negation of CD1~ and CD2~ may be sensed by the MPC and, consequently, the Card's power supply may be cut.

Warning

5V power applied to a 3.3V-only PC Card will inflict permanent damage. Prior to applying power to a PC Card, all application software handling the PCMCIA channel must check the Voltage-Sense lines.

4•11 Board Control & Status Register: BCSR

The majority of MPC852TADS hardware options are controlled or monitored by the BCSR. The BCSR is a 32[B]-bit wide read / write register file accessed via the MPC's CS1 region that includes five registers: BCSR0 to BCSR4. A CS region has a minimum block size of 32 KB thus registers BCSR0 - BCSR4 are duplicated within that region. See TABLE 3-2. "Memory Map in MPC852TADS Compatible Mode" on page 21 or TABLE 3-1. "Memory Map in MP852TADS New Mode," on page 21.

The BCSR controls / monitors the following functions:

1) MPC Hard Reset Configuration
2) Flash Module Enable / Disable
3) Flash Size / Delay Identification
4) DRAM Module Enable / Disable
5) DRAM Port Width: 32-bit / 16-bit.
6) DRAM Type / Size and Delay Identification
7) SDRAM Module Enable / Disable
8) Fast Ethernet Port Enable / Disable
9) Fast Ethernet Port Control
10) Reset Fast Ethernet PHY
11) RS232 Port 1 Enable / Disable
12) RS232 Port 2 Enable / Disable
13) Hard Reset Configuration Source - BCSR0 / Flash Memory
14) PCMCIA controls:

A. Hot insertion refers to card insertions made when the ADS is powered.
B. Despite the BCSR being mapped as a 32-bit wide register, that should be accessed as such, only the upper 16 bits - D(0:15) are used.

- Channel Enable / Disable
- PC Card VCC appliance
- PC Card VPP appliance

15) External (off-board) tool identification or software-option selection switch, SW5 status

16) Board Revision Code

4•11•1 BCSR0: Hard Reset Configuration Register

The BCSR0 is located at offset 0 on BCSR space, may be read or written at any time and has defaults set at the time of MAIN[A] power-on reset. If the Flash_Configuration_Enable~ bit in BCSR1 is inactive then, during Hard Reset, data contained in BCSR0 is driven on the data bus to provide the MPC's Hard Reset configuration. The BCSR0 may be written at any time in order to change the MPC's Hard Reset configuration. The new values, regardless of the Hard Reset source, become valid the next time a Hard Reset is issued to the MPC. TABLE 4-10. provides a description of BCSR0 bits.

TABLE 4-10. BCSR0 Description

BIT	*MNEMONIC*	*FUNCTION*	*PON DEF.*	*ATT*
0	ERB	***External Arbitration.*** Arbitration is performed internally if'0' during Hard Reset. If'1' during Hard Reset, Arbitration is performed externally.	0	R,W
1	IP	***Interrupt Prefix.*** Interrupt Prefix set to 0xFFF00000 if'0' during Hard Reset. If'1' during Hard Reset, Interrupt Prefix set to 0.	1	R,W
2	Reserved	Implemented[a]	0	R,W
3	BDIS	***Boot Disable.*** CS0~ region is enabled for boot if'0' during Hard-Reset. If'1', CS0~ region is disabled for boot.	0	R,W
4 - 5	BPS(0:1)	***Boot Port Size***,'00' - 32-bit,'01' - 8-bit,'10' - 16-bit,'11' - reserved, determines the CS0~ port size at boot.	'00'	R,W
6	Reserved	Implemented[a]	0	R,W
7 - 8	ISB(0:1)	***Initial Space Base.*** Initial base address of the internal MPC's memory map determined by the value at Hard Reset. If'00', initial space at 0. If'01', initial space at 0x00F00000. If'10', initial space at 0xFF000000. If'11', initial space at 0xFFF00000.	'10'	R,W
9 - 10	DBGC(0:1)	***Debug Pin Configurations.*** PCMCIA channel II pin function's determined by the value during Hard Reset. If'00' the pins function as PCMCIA channel II pins. If'01' the pins serve as Watch Points. If'10' the pins are reserved. If'11' the pins become show-cycle attributes, e.g., VFLS, VF...	'00'	R,W
11-12	DBPC(0:1)	***Debug Port Pin Configurations.*** Location of the debug port pins determined by the value during Hard Reset. If'00', debug port pins found on the JTAG port. If'01', the debug port is non-existent. If'10', reserved. If'11', the debug port is on PCMCIA channel II pins.	'00'	R,W

A. MAIN power-on reset, i.e. when VDDH is powered to the MPC.

TABLE 4-10. BCSR0 Description

BIT	MNEMONIC	FUNCTION	PON DEF.	ATT
13 - 14	EBDF(0:1)	***External Bus Division Factor.*** The factor for dividing the CLKOUT of the MPC's external bus, with respect to its internal MPC clock, is determined by the value at Hard Reset. If'00' then CLKOUT is GCLK2 divided by 1. If'01' then CLKOUT is GCLK2 divided by 2.	'00'	R,W
15	Reserved	Implemented[a]	'0'	R,W
16 - 31	Reserved	Not Implemented	-	-

a. Reserved mnemonics may be read and written as any other field. They are presented at their associated data pins during Hard Reset.

4•11•2 BCSR1: Board Control Register 1

BCSR1 serves as an ADS control register, may be read or written at any time, is accessible at offset 4 from the BCSR

base address and has defaults set at the time of power-on reset. TABLE 4-11.describes BCSR1 fields.

TABLE 4-11. BCSR1 Description

BIT	*MNEMONIC*	*Function*	*PON DEF*	*ATT.*
0	FLASH_EN	***Flash Enable***. When active (**low**), the Flash Memory module is enabled on the local memory map. When inactive, the Flash memory is removed from the local memory map.	0	R,W
1	DRAM_EN	***DRAM Enable***. When active (**low**), the DRAM module is enabled on the local memory map. When inactive, the DRAM is removed from the local memory map.	0	R,W
2-3	Reserved	Not implemented	-	-
4	FLASH_CFG_EN	***Flash Configuration Enable***. When asserted (**low**), the Hard Reset configuration held in BCSR0 is NOT driven on the data bus during Hard Reset. Also, configuration data held at the 1'st word of the Flash Memory is driven to the data bus during Hard Reset. [a]	1	R,W
5-6	Reserved	Not implemented	-	-
7	RS232EN_1	***RS232 Port 1 Enable***. When asserted (**low**), the RS232 Port 1 transceiver is enabled. When negated, the transceiver is in standby mode and the relevant MPC Communication Port pins become available for off-board use via the expansion connectors.	1	R,W
8	PCCEN	***PC Card Enable***. When asserted (**low**), the on-board PCMCIA channel is enabled, i.e. address and strobe buffers are enabled to / from the card. When negated, all buffers to / from the PCMCIA channel are disabled allowing off-board use of its associated lines.	1	R,W
9	PCCVCC0	***PC Card VCC Select 0***. These signals, in conjunction with PCCVCC1, determine the voltage applied to the PCMCIA card's VCC. Possible values are 0 / 3.3 / 5 V. For line encoding and associated voltages see TABLE 4-12. "PCCVCC(0:1) Encoding" on page 55.	0	R,W
10 - 11	PCCVPP(0:1)	***PC Card VPP***. These signals determine the voltage applied to the PCMCIA card's VPP. Possible values are 0 / 5 / 12 V. For line encoding and associated voltages see TABLE 4-13. "PCCVPP(0:1) Encoding" on page 55.	'11'	R,W
12	Dram_Half_Word	***DRAM Half Word***. When active (**low**), and the steps listed in 4•6•1 "DRAM 16-Bit Operation" on page 38 are taken, the DRAM is 16-bit wide. When inactive, the DRAM is 32-bit wide.	1	R,W
13	RS232EN_2	***RS232 Port 2 Enable***. When asserted (**low**), the RS232 Port 2 transceiver is enabled. When negated, the transceiver enters standby mode and the relevant MPC Communication Port pins become available for off-board use via the expansion connectors.	1	R,W
14	SDRAMEN	***SDRAM Enable***. When active (**high**), the SDRAM module is enabled on the local memory map. When inactive, the SDRAM is placed in low-power mode.	1	R,W

TABLE 4-11. BCSR1 Description

BIT	*MNEMONIC*	*Function*	*PON DEF*	*ATT.*
15	PCCVCC1	***Pc Card VCC Select 1***. These signals, in conjunction with PCCVCC0, determine the voltage applied to the PCMCIA card's VCC. Possible values are 0 / 3.3 / 5 V. For line encoding and associated voltages see TABLE 4-12. "PCCVCC(0:1) Encoding" on page 55.	1	R,W
16 - 31	Reserved	Not implemented	-	-

a. Configuration data is handled in this manner provided that the MPC supports the option by driving address lines low and asserting CS0~ during Hard Reset.

TABLE 4-12. PCCVCC(0:1) Encoding

PCCVCC(0:1)	*PC-Card VCC [V]*
00	0
01	5
10	3.3
11	0

TABLE 4-13. PCCVPP(0:1) Encoding

PCCVPP(0:1)	*PC Card VPP [V]*
00	0
01	5
10	12[a]
11	Hi-Z

a. Provided a 12V power supply is applied.

4•11•3 BCSR2: Board Control / Status Register 2

BCSR2 is a status register accessed at offset 8 from the BCSR base address. It is a read-only register that may be read at any time. TABLE 4-14. "BCSR2 Description" on page 56 describes the various BCSR2 fields.

TABLE 4-14. BCSR2 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
0 - 3	FLASH_PD(4:1)	***Flash Presence Detect(4:1)***. These lines are connected to the Flash SIMM Presence Detect lines that encode the Flash SIMM Type mounted on the Flash SIMM socket. Three additional Presence Detect lines, that encode the SIMM Delays, appear in BCSR3. For FLASH_PD(4:1) encoding see TABLE 4-15. "Flash Presence Detect (4:1) Encoding" on page 56.	-	R
4	Reserved	Not Implemented	-	-
5 - 8	DRAM_PD(4:1)	***DRAM Presence Detect***. These lines are connected to the DRAM SIMM Presence Detect lines that encode the size and delay of the DRAM SIMM mounted on the DRAM SIMM socket. For DRAM_PD(4:1) encoding see TABLE 4-16. "DRAM Presence Detect (2:1) Encoding" on page 56 and TABLE 4-17. "DRAM Presence Detect (4:3) Encoding" on page 57.	-	R
9-31	Reserved	Not Implemented	-	-

TABLE 4-15. Flash Presence Detect (4:1) Encoding

FLASH_PD(4:1)	FLASH TYPE / SIZE
0 - 3	Reserved
4	SM732A2000 / SM73228: 8 MB SIMM by SMART Modular Technologies.
5	SM732A1000A / SM73218: 4 MB SIMM by SMART Modular Technologies.
6	MCM29080: 8 MB SIMM by Motorola
7	MCM29040: 4 MB SIMM by Motorola
8	MCM29020: 2 MB SIMM by Motorola
9 - F	Reserved

TABLE 4-16. DRAM Presence Detect (2:1) Encoding

DRAM_PD(2:1)	DRAM TYPE / SIZE
00	MCM36100 by Motorola or MT8D132X by Micron: 4 MB SIMM
01	MCM36800 by Motorola or MT16D832X by Micron: 32 MB SIMM
10	MCM36400 by Motorola or MT8D432X by Micron: 16 MB SIMM

TABLE 4-16. DRAM Presence Detect (2:1) Encoding

DRAM_PD(2:1)	*DRAM TYPE / SIZE*
11	MCM36200 by Motorola or MT16D832X by Micron: 8 MB SIMM

TABLE 4-17. DRAM Presence Detect (4:3) Encoding

DRAM_PD(4:3)	*DRAM DELAY*
00	Reserved
01	Reserved
10	70 nsec
11	60 nsec

WARNING

SWOPT(0:3) lines may be driven low ('0') by the DIP switch. Off-board tools should never drive lines high as this may result in permanent damage to the ADS and/or to the off-board logic.

4•11•4 BCSR3: Board Control / Status Register 3

BCSR3 is an additional BCSR that may be accessed at offset 0xC from the BCSR base address. BCSR3 sets defaults during Power-On reset and may be read or written at any time. TABLE 4-18. on page 58 describes the BCSR3.

TABLE 4-18. BCSR3 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
0 - 1	Reserved	Implemented	'00'	R
2 - 8	Reserved	Not Implemented	-	-
9 - 11	FLASH_PD(7:5)	***Flash Presence Detect(7:5)***. These lines are connected to the Flash SIMM Presence Detect lines that encode the Flash SIMM Delay mounted on the Flash SIMM socket - U21. Four additional Presence Detect lines, that encode the SIMM Types, appear in BCSR2. For FLASH_PD(7:5) encoding see TABLE 4-19. "FLASH Presence Detect (7:5) Encoding" on page 58.	-	
12-15	Reserved	Not Implemented	-	R

TABLE 4-19. FLASH Presence Detect (7:5) Encoding

FLASH_PD(7:5)	Flash Delay [nsec]
000	Unsupported
001	150
010	120
011	90
100 - 111	Unsupported

4•11•5 BCSR4 - Board Control / Status Register 4

The BCSR4 serves as an ADS control register, is accessed at offset 10H from the BCSR base address, may be read or written at any time and has defaults set at Power-On reset. BCSR4 fields are described in TABLE 4-20. "BCSR4 Description" on page 58.

.

TABLE 4-20. BCSR4 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
0-2	Reserved	Not Implemented	-	-
3	SIGNAL_LAMP	***Signal Lamp***. When the signal is active (low) a dedicated LED illuminates. When inactive there is no LED light. The LED is used for software signalling.	1	R,W
4	RSTMII	***RSTMII.*** When active (**low**), the MII Fast Ethernet Device Davicom DM9161E gets reset and being initialized to its Reset value. When inactive, the MII Fast Ethernet Device is out of Reset.	1	R,W

TABLE 4-20. BCSR4 Description

BIT	MNEMONIC	Function	PON DEF	ATT.
5	MIIRXEN	***MIIRXEN.*** When active (**high**), the MII Fast Ethernet Device Davicom DM9161E connected to Port D is enabled. When negated (low) all device output signals are tri- stated.	0	R,W
6	PORESET	***PORESET***[a]***.*** When active (**high**), PORESET is implemented on the MPC852TADS. When negated (low), the board is out of Power on Reset.	0	R,W
7	ETHRST	***ETHRST.*** When active (**low**), the Ethernet Device Davicom DM9161E gets reset and being initialized to its Reset value. When inactive, the Ethernet Device is out of Reset.	1	R,W
8-31	Reserved	Not Implemented	-	R,W

a. Not implemented.

4•12 On board EPP/SPP Command Converter[A]

For host-controlled operation, a host computer controls the board via the BDM Debug Port. This configuration serves for extensive debugging using an on-host debugger. Host computer can be connected with the board directly via On board Serial command converter or via On board EPP converter. No needs external parts.

EPP is an asynchronous, byte wide, bidirectional channel controlled by the host device. This interface provides the capability to send data from the host computer to the MPC852T at a high speed.

The bus is a multiplexed address/data bus connected to a D-Type 25 pins Parallel connector called P20. Typically, EPP operates on a two-phase-bus cycle. First, an address is generated on the bus and is latched by Altera logic when the host generates an address strobe. The Altera logic uses this cycle for control. A separate Data strobe is generated to perform the actual data transfer. Cycles are terminated when the Busy signal is transferred from the Altera to the host computer.

In the Altera logic there is a parallel to serial converter for write data and a serial to parallel converter for read data from the MPC.

The signals used for EPP Mode transfer are described in detail in TABLE 4-21. "Parallel Host Port Connector's Signal Description with EPP I/F" below . The signals used for Serial Command Converter Mode transfer are described in detail in TABLE 4-22. "Parallel Host Port Connector's Signal Description with Serial Command

A. For FUTURE Use

Converter I/F" below.

TABLE 4-21. Parallel Host Port Connector's Signal Description with EPP I/F

Pin #	*Signal Mnemonic*	*ATT.*[a]	*Description*
1	Write-	I	Write signal. Used to denote an address or data read or write operation between the host and the MPC852TADS.
2-9,15	AD1-AD8	I/O	8 bit Bidirectional Address Data Muxed Bus.
10	IRQ-	O	Interrupt signal. Used by the MPC852TADS to Interrupt the Host.
11	Wait-(BUSY)	O	Wait signal. Used by the MPC852TADS to acknowledge that the Data or Address transfer requested by the Host has completed.
12	FREEZE0	O	Connected to VFLS0 via the Altera logic. See 4•13•1•1 "VFLS(0:1)" on page 62.
13	Select	O	5V_OUT. This is the MPC852TADS 5V power supply, which indicate to the debug station, that the target processor is powered.
14	Dstrobe-	I	Data Strobe signal. Used by the Host to denote a Data cycle
15	FREEZE1	O	Connected to VFLS1 via the Altera logic. See 4•13•1•1 "VFLS(0:1)" on page 62.
16	Reset-	I	PP_RST signal. Used by the Host to initiate a termination cycle to return the interface to the Compatible mode.
17	Astrobe-	I	Address Strobe signal. Used by the Host to denote an Address cycle.
18-24	GND	-	MPC852TADS Ground Plane.
25	IN-	I	This is a mechanical signal. On the Host side it is connected to GND. When on the MPC852TADS side it will identify GND on this pin, it is indicated that the Parallel connector was pluged.

a. Signal attributes are with reference to the MPC852TADS.

TABLE 4-22. Parallel Host Port Connector's Signal Description with Serial Command Converter I/F

Pin #	*Signal Mnemonic*	*ATT.*[a]	*Description*
1	-	N.C.	Not Connected.
2	DSDI	I	Serial Data Input to the MPC852TADS.
3	DSCK	I	Serial Clock Input to the MPC852TADS.
4	-	N.C.	Not Connected.
5	Reset	I	Reset signal is active high. Used by the Host to cause Hard reset to MPC852TADS.

TABLE 4-22. Parallel Host Port Connector's Signal Description with Serial Command Converter I/F

Pin #	*Signal Mnemonic*	*ATT.*[a]	*Description*
3-10	-	N.C.	Not Connected.
11	DSDO	O	Serial Data Out from the MPC852TADS.
12	-	N.C.	Not Connected.
13	5V_OUT	O	5V_OUT. This is the MPC852TADS 5V power supply, which indicates to the debug station, that the target processor is powered.
14-17	-	N.C.	Not Connected.
18-24	GND	-	MPC852TADS Ground Plane.
25	IN-	I	This is a mechanical signal. On the Host side it is connected to GND. When on the MPC852TADS side it will identify GND on this pin, it is indicated that the Parallel connector was pluged.

a. Signal attributes are with reference to the MPC852TADS.

4•12•1 EPP Register Definitions

EPP is an Enhanced Parallel Port which is one of IEEE 1284 data transfer mode. EPP is an extension to the register definitions for the standard parallel port called SPP. See TABLE 4-23. "EPP Register Interface" below.

TABLE 4-23. EPP Register Interface

Port name	*I/O MAP Address*[a]	*Mode*	*Read/Write*	*Description*
SPP Data Port	Base + 0	SPP/EPP	W	Standard SPP Data Port.
SPP Status Port	Base + 1	SPP/EPP	R	Reads the input status lines on the interface.
SPP Control Port	Base + 2	SPP/EPP	W	Sets the state of the Output Control lines.
EPP Address Port	Base + 3	EPP	R/W	Generates Address Read or Write Cycle.
EPP Data Port	Base + 4	EPP	R/W	Generates Data Read or Write Cycle.
Not Defined	Base + 5 to Base + 7	EPP	N.A.	Not Available.

a. IBM PC defines two standard port base addresses: 0x378 or 0x278.

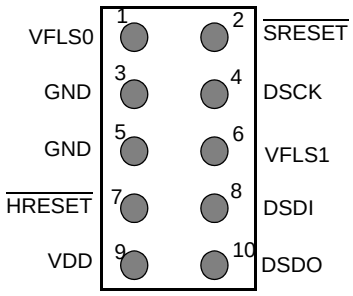
When both Parallel connector P20 and BDM Debug Connector P12 are connected,
priority will be to on board serial command converter or EPP transfer mode via P20.

Default host selection is SPP Transfer Mode.
When the Host computer will begin an EPP negotiation access, MPC852TADS will switch to EPP Transfer Mode.
For EPP negotiation please refer to IEEE 1284 EPP Protocol.

4•13 BDM Debug Port

The MPC852TADS has a BDM Debug interface (10 pin generic header connector) to enable debugging through external host. The signals are described in detail in FIGURE 4-6 "Standard BDM Debug Port Connector" below.

FIGURE 4-6 Standard BDM Debug Port Connector



4•13•1 Standard MPC852T Debug Port Connector Pin Description

The standard debug port connector pins are needed to support debug port controllers for MPC852TADS.

4•13•1•1 VFLS(0:1)

These pins indicate to the debug port controller whether or not the MPC is in debug mode. When both VFLS(0:1) are at'1', the MPC is in debug mode. As these lines may serve varying functions for the MPC the FRZ must be selected on either the ADS or target system[A].

4•13•1•2 HRESET*

This is the MPC's Hard Reset bidirectional signal. When asserted (low) the MPC enters a Hard Reset sequence that includes Hard Reset configuration. The signal is made redundant with the MPC852T debug port controller as there is a Hard Reset command integrated into the debug port protocol. However, for compatibility with existing MPC5XX boards and software, the local debug port controller uses this signal.

4•13•1•3 SRESET*

This is the MPC852T's Soft Reset bidirectional signal whereas on the MPC5XX it is an output. The debug port configuration is sampled and determined on the rising-edge[B] of SRESET* (for both processor families). On the MPC852T this bidirectional signal may be driven externally to generate a Soft Reset sequence. Regarding the MPC852T debug port controller, the signal is redundant as there is a Soft Reset command integrated into the debug port protocol. However, for compatibility with existing MPC5XX boards and software, the local debug port controller uses this signal.

4•13•1•4 DSDI: Debug Port Serial Data In

The debug port controller sends its data to the MPC via the DSDI signal. The DSDI also serves a role during Soft

A. The FRZ line should be connected to both VFLS(0:1) pins on the debug port connector when a target system needs to use either of the alternative VFLS(0:1) functions.
B. The configuration is divided into two parts, the first is sampled three system-clock cycles prior to the rising edge of SRESET* while the second is sampled eight clocks after the rising edge.

Reset configuration. See 4•1•6•3 "Soft Reset Configuration" on page 36.

4•13•1•5 DSCK: Debug Port Serial Clock

Serial data is clocked into the MPC according[A] to the DSCK clock during the asynchronous clock mode. The DSCK also serves a role during Soft Reset configuration. See 4•1•6•3 "Soft Reset Configuration" on page 36.

4•13•1•6 DSDO: Debug Port Serial Data Out

The MPC clocks out the DSDO according to the debug port clock and in parallel[B] with the DSDI being clocked in. The DSDO also serves as a *READY* signal for the debug port controller by indicating that the debug port is ready to receive the controller's command or data.

4•14 Power

The MPC852T features three power buses:

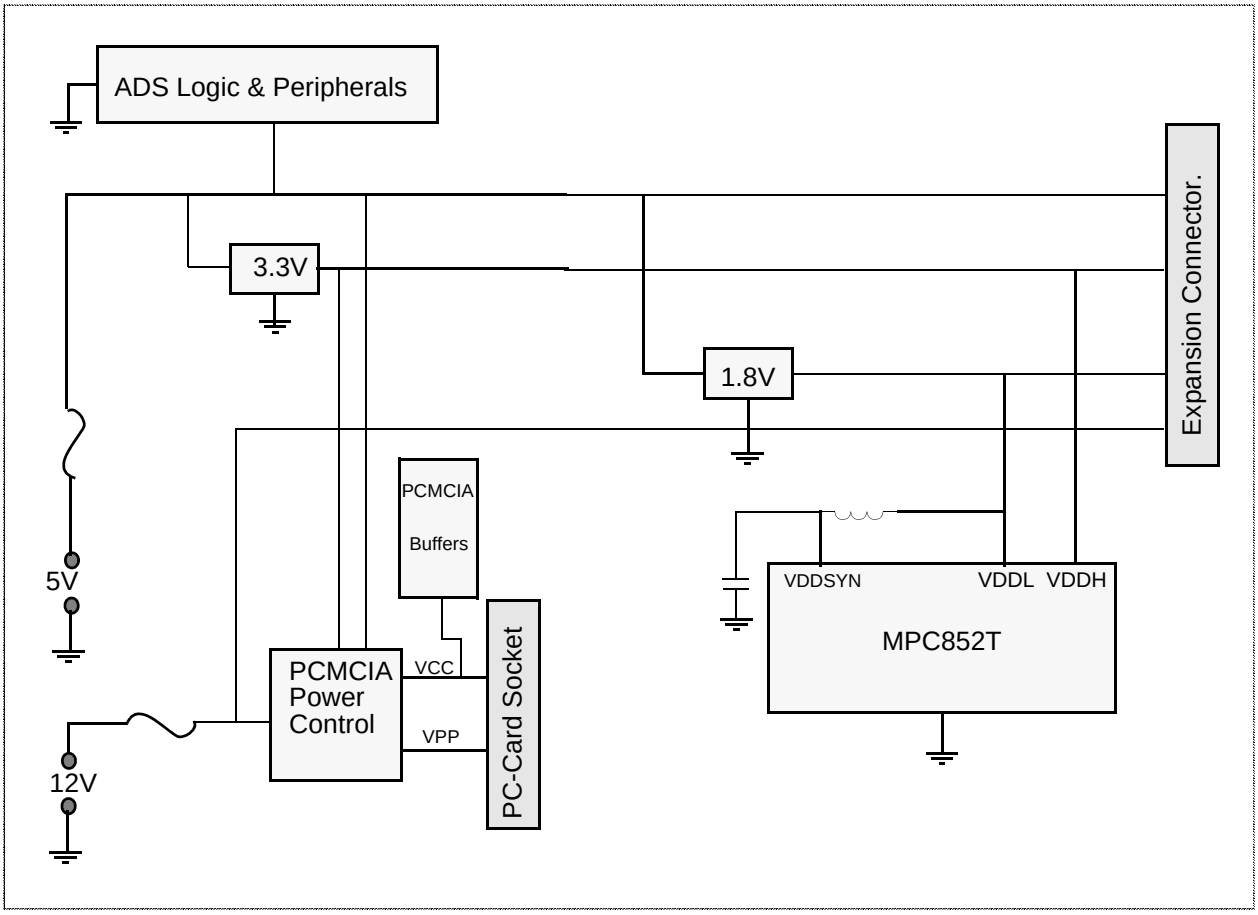
1) I/O
2) Internal Logic
3) PLL

The MPC852TADS has four different power:

1) 5V
2) 3.3V
3) 12V
4) 1.8V

A. For example, the DSDI must meet the DSCK's setup / hold time to / from rising edge criteria.
B. In parallel, i.e. full-duplex communication.

FIGURE 4-7 MPC852TADS Power Scheme



To support off-board application development, the power buses are connected to the expansion connectors in order that external logic may be powered directly from the board. The maximum current allowed drawn from each board bus is shown in TABLE 4-24. "Off-board Application Maximum Current Consumption" below.

TABLE 4-24. Off-board Application Maximum Current Consumption

Power BUS	*Current*
5V	1.5A
3.3V	1.5A
12V	100 mA.

In order to protect on board devices from supply spikes, uncoupling capacitors (typically 0.1µF) are located in the closest possible proximity to the device's power leads and the GND.

4•14•1 5V Bus

Some ADS peripherals reside on the 5V bus. The MPC, however, is not 5V compatible. Consequently 3.3V to 5V buffers were added between the MPC and the 5V devices in order that the MPC may operate 5V levels on its lines without damage. The 5V bus is connected via a fuse (5A) to an external power connector.

To forestall reverse-voltage or over-voltage being applied to the 5V inputs, a set of high-current diodes and a zener diode were connected between the 5V bus and the GND.

4•14•2 3.3V Bus

The MPC and SDRAM as well as the address and data buffers are powered by a 3.3V[A] bus produced from a 5V bus using Micrel's special low-voltage drop / linear voltage regulator, the MIC29500-3.3BT. This device is capable of driving a fuse of up to 5A as well as facilitating operation of external logic.

4•14•3 12V Bus

The sole purpose of the 12V bus is to supply VPP (programming voltage) to the PCMCIA card and the Flash SIMM[B]. The 12V bus is connected to a dedicated input connector via a fuse (1A) and is protected from over / reverse voltage application. If the 12V supply is not required for either the PC Card or the Flash SIMM then 12V input to the ADS may be omitted.

A. 3.3 V required for full speed. Internal logic may be powered by a 2V bus for reduced performance levels.
B. 12V necessary only for the PCMCIA card and the Flash SIMM.

5 - Support Information

This chapter provides MPC852TADS support, maintenance and connectivity information.

5•1 Interconnect Signals

The MPC852TADS interconnects with external devices via the following connectors:

1) P1, P2: Expansion Connectors
2) P3, P4, P6, P7, P8, P11, P15: Logic Analyzer Mictor Connectors
3) P5: PCMCIA Port
4) P9, P10: 100/10Base-T Ethernet Port Connectors (RJ45)
5) P12: External Debug Port Controller
6) P13: 12V Power-In
7) P14: External Clock Connector
8) P16: 2.1 mm Power-Jack 5V Connector
9) P17: RS232 Dual Port Connector
10) P18, P19: Altera programming ISP Connectors
11) P20: Parallel Host Port connector[A]

5•1•1 P1, P2: Expansion Connectors

P1, P2 are a 96-pin, 90^{o}, DIN 41612 connectors that enable convenient expansion of the MPC's signals. P1 contains

A. For FUTURE Use

buffered data [0-7], buffered address [16-31] and PCMCIA signals. P2 contains the I/O ports signals.

TABLE 5-1 P1: ADD, Data and PCMCIA Expansion Connector Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
A1	BWAITAb	I	Wait Slot A PCMCIA signal for extending bus cycle
A2	BVS1	I	Input Port A 0, Voltage Sense 1 - buffered
A3	BVS2	I	Input Port A 1, Voltage Sense 2 - buffered
A4	BWP	I	Input Port A 2, Write Protect - buffered
A5	BCD2b	I	Input Port A 3, Card Detect 2 - buffered
A6	BCD1b	I	Input Port A 4, Card Detect 1 - buffered
A7	BBVD2	I	Input Port A 5, Battery Voltage Detect 2 - buffered
A8	BBVD1	I	Input Port A 6, Battery Voltage Detect 1 - buffered
A9	BRDY	I	Input Port A 7, Ready/Busy - buffered
A10	GND		GND
A11	RESETA	O	Output Port 0, Card Reset
A12	GND		GND
A13	N.C	-	
A14	BWE0b	O	MPC852T WE0 Pin - used for external peripheral
A15	BDRMWb	O	MPC852T GPL0 Signal - used for DRAM write signal
A16	BEDOOEb	O	MPC852T GPL1 Pin - used for DRAM oe~ signal
A17	BGPL2b	O	MPC852T GPL2 Pin - buffered
A18	BGPL3b	O	MPC852T GPL3 Pin - buffered
A19	BGPL4Ab	O	MPC852T GPL4A Pin - buffered
A20	N.C.	-	
A21	BGPL5Ab	O	MPC852T GPL5A Pin - buffered
A22	BGPL5Bb	O	MPC852T GPL5B Pin - buffered
A23	GND		
A24	BSYSCLK3	O	MPC852T CLKOUT Pin - driven by zero delay buffer
A25	GND		GND
A26	BBSA0b	O	MPC852T BS0b Pin - buffered
A27	GND		GND
A28	BRW2b	O	MPC852T RWb Pin - buffered
A29	BTSb	O	MPC852T TSb Pin - buffered

Support Information

TABLE 5-1 P1: ADD, Data and PCMCIA Expansion Connector Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
A30	TAb	I/O	MPC852T TA Pin
A31	BCS7b	O	MPC852T CS7 Pin - buffered
A32	BCS6b	O	MPC852T CS6 Pin - buffered
B1	3.3V	I/O	Power 3.3V
B2	3.3V	I/O	Power 3.3V
B3	3.3V	I/O	Power 3.3V
B4	3.3V	I/O	Power 3.3V
B5	3.3V	I/O	Power 3.3V
B6	3.3V	I/O	Power 3.3V
B7	N.C.	-	
B8	GND		GND
B9	BCE2Ab	O	Card Enable 2 for odd bytes in PCMCIA I/F - buffered
B10	BCE1Ab	O	Card Enable 1 for even bytes in PCMCIA I/F - buffered
B11	BALEA	O	Address Latch Enable - buffered
B12	MIICOL	I	MPC852T MII Collision Detect
B13	MIITXEN	O	MPC852T MII Transmit Enable
B14	MPCMDIO	I/O	MPC852T MII Management Data
B15	MIICRS	I	MPC852T MII Carrier Sense Detect
B16	GND		GND
B17	N.C	-	
B18	GND	I/O	GND
B19	N.C	-	
B20	GND		GND
B21	N.C	-	
B22	GND		GND
B23	N.C	-	
B24	GND		GND
B25	N.C	-	
B26	GND		GND
B27	N.C	-	
B28	GND		GND

Support Information

TABLE 5-1 P1: ADD, Data and PCMCIA Expansion Connector Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
B29	N.C	-	
B30	GND		GND
B31	N.C	-	
B32	GND		GND
C1	EXP_BD0	I/O	MPC852T Buffered D0 - D7
C2	EXP_BD1	I/O	
C3	EXP_BD2	I/O	
C4	EXP_BD3	I/O	
C5	EXP_BD4	I/O	
C6	EXP_BD5	I/O	
C7	EXP_BD6	I/O	
C8	EXP_BD7	I/O	
C9	EXP_A16	O	MPC852T buffered A16 - A31
C10	EXP_A17	O	
C11	EXP_A18	O	
C12	EXP_A19	O	
C13	EXP_A20	O	
C14	EXP_A21	O	
C15	EXP_A22	O	
C16	EXP_A23	O	
C17	EXP_A24	O	
C18	EXP_A25	O	
C19	EXP_A26	O	
C20	EXP_A27	O	
C21	EXP_A28	O	
C22	EXP_A29	O	
C23	EXP_A30	O	
C24	EXP_A31	O	
C25	N.C.	-	
C26	N.C	-	
C27	N.C	-	

Support Information

TABLE 5-1 P1: ADD, Data and PCMCIA Expansion Connector Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
C28	N.C	-	
C29	N.C	-	
C30	N.C	-	
C31	N.C	-	
C32	N.C	-	

TABLE 5-2. P2: I/O Port Expansion Interconnect Signals

Pin No.	Signal Name	Attribute	Description
A1	N.C.	-	
A2	N.C.	-	
A3	N.C.	-	
A4	N.C.	-	
A5	MIITXERR	I/O	MPC852T PD11 Pin used on the board as MII Transmit Error
A6	MIIRXD0	I/O	MPC852T PD10 Pin used on the board as MII Receive data bit 0.
A7	MIITXD0	I/O	MPC852T PD9 Pin used on the board as MII Transmit data bit 0.
A8	MIIRXCLK	I/O	MPC852T PD8 Pin used on the board as MII Receive Clock.
A9	N.C.	-	
A10	N.C.	-	
A11	N.C.	-	
A12	N.C.	-	
A13	ETHRXCK	I/O	MPC852T PA3 Pin used on the board as 10Base-T Ethernet port **receive** clock
A14	ETHTXCK	I/O	MPC852T PA2 Pin used on the board as 10Base-T Ethernet port **transmit** clock
A15	PA1	I/O	MPC852T PA1 Pin
A16	PA0	I/O	MPC852T PA0 Pin
A17	VCC	-	VCC
A18	RSRXD2	I/O	MPC852T PA11 Pin used on the board as RS232_2 RXD signal
A19	RSTXD2	I/O	MPC852T PA10 Pin used on the board as RS232_2 TXD signal.
A20	ETHRXD	I/O	MPC852T PA9 Pin used on the board as 10Base-T Ethernet port **receive** data
A21	ETHTXD	I/O	MPC852T PA8 Pin used on the board as 10Base-T Ethernet port **transmit** data
A22	GND		GND
A23	GND		GND
A24	N.C.	-	
A25	FRZ	I/O	MPC852T FRZ pin
A26	N.C.	-	
A27	IRQ3b	I, L	MPC852T IRQ3~ Pin

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TABLE 5-2. P2: I/O Port Expansion Interconnect Signals

Pin No.	Signal Name	Attribute	Description
A28	IRQ2b	I, L	MPC852T IRQ2~ Pin
A29	IRQ1b	I, L	MPC852T IRQ1~ Pin
A30	NMIb	I, L	MPC852T NMI~ Pin
A31	nRSEN1	O,L	BCSR RS232 _1 Enable
A32	GND		GND
B1	PB31	I/O	MPC852T PB31 Pin
B2	PB30	I/O	MPC852T PB30 Pin
B3	PB29	I/O	MPC852T PB29 Pin
B4	PB28	I/O	MPC852T PB28 Pin
B5	N.C.	-	
B6	N.C.	-	
B7	RSTXD1	I/O	MPC852T PB25 Pin used on the board as RS232_1 TXD signal.
B8	RSRXD1	I/O	MPC852T PB24 Pin used on the board as RS232_1 RXD signal.
B9	N.C.	-	
B10	N.C.	-	
B11	N.C.	-	
B12	N.C.	-	
B13	N.C.	-	
B14	N.C.	-	
B15	N.C.	-	
B16	N.C.	-	
B17	PB15	I/O	MPC852T PB15 Pin
B18	N.C.	-	
B19	GND		GND
B20	BINPACKb	I/O	MPC852T PC15 pin used as INPACK for PCMCIA
B21	N.C.	-	
B22	nRSRTS2	I/O	MPC852T PC13 Pin used as RS232_2 RTS signal
B23	ETHTXEN	I/O	MPC852T PC12 Pin used as 10Base-T Ethernet port TENA signal
B24	N.C.	-	
B25	N.C.	-	
B26	N.C.	-	

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TABLE 5-2. P2: I/O Port Expansion Interconnect Signals

Pin No.	Signal Name	Attribute	Description
B27	N.C.	-	
B28	nRSCTS2	I/O	MPC852T PC7 Pin used as RS232_2 CTS signal
B29	nRSCD2	I/O	MPC852T PC6 Pin used as RS232_2 CD signal
B30	ETHCOL	I/O	MPC852T PC5 Pin used as 10Base-T Ethernet port Collision signal
B31	ETHCRS	I/O	MPC852T PC4 Pin used as 10Base-T Ethernet port CRS signal
B32	GND		GND
C1	VCC		VCC
C2			
C3			
C4			
C5			
C6	nRSEN2	O, L	BCSR RS232 _2 Enable
C7	GND		GND
C8			
C9			
C10			
C11			
C12			
C13			
C14			
C15	MIIRXD3	I/O	MPC852T PD15 Pin used on the board as MII Receive data bit 3
C16	MIIRXD2	I/O	MPC852T PD14 Pin used on the board as MII Receive data bit 2
C17	MIIRXD1	I/O	MPC852T PD13 Pin used on the board as MII Receive data bit 1
C18	MPCMDC	I/O	MPC852T PD12 Pin used on the board as MPC Management Data Clock
C19	MIIRXERR	I/O	MPC852T PD7 Pin used on the board as MII Receive Error signal
C20	MIIRXDV	I/O	MPC852T PD6 Pin used on the board as MII Receive Data Valid
C21	VCC		VCC
C22	HRESET~	I/O, L	MPC852T HRESET Pin
C23	SRESET~	I/O, L	MPC852T SRESET Pin
C24	N.C.	-	

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TABLE 5-2. P2: I/O Port Expansion Interconnect Signals

Pin No.	Signal Name	Attribute	Description
C25	VCC		VCC
C26	MIITXD1	I/O	MPC852T PD3 Pin used on the board as MII Transmit data bit 1
C27	VPPIN	I/O	+12V input for PCMCIA Flash programming. Parallel to MPC852TADS's P13.
C28			
C29	GND		GND
C30	MIITXD2	I/O	MPC852T PD4 Pin used on the board as MII Transmit data bit 2
C31	GND		GND
C32	MIITXD3	I/O	MPC852T PD5 Pin used on the board as MII Transmit data bit 3

5•1•2 P3, P4, P6, P7, P8, P11 and P15 MICTOR: Logic Analyzer connectors

The noted connectors are AMP 38-pin, receptacle MICTOR connectors. They connect to a dedicated adaptor from the HP 16500 Series of logic analyzers. The adaptor joins between two 16-bit pods.

TABLE 5-3. P3: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
1	N.C.	2	N.C.
3	GND	4	N.C.
5	BSYSCLK4	6	MODCK1
7	A0	8	A16
9	A1	10	A17
11	A2	12	A18
13	A3	14	A19
15	A4	16	A20
17	A5	18	A21
19	A6	20	A22
21	A7	22	A23
23	A8	24	A24
25	A9	26	A25
27	A10	28	A26
29	A11	30	A27

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TABLE 5-3. P3: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
31	A12	32	A28
33	A13	34	A29
35	A14	36	A30
37	A15	38	A31

TABLE 5-4. P4: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Names	Pin #	MPC852T Signal Names
1	N.C.	2	N.C.
3	GND	4	N.C.
5	DRMWb	6	CE2Ab
7	GPL5Ab	8	PA0
9	GPL3b	10	PA1
11	GPL2b	12	ETHTXCK
13	EDOOEb	14	ETHRXCK
15	ETHCRS	16	N.C.
17	ETHCOL	18	N.C.
19	nRSCD2	20	N.C.
21	nRSCTS2	22	N.C.
23	N.C.	24	ETHTXD
25	N.C.	26	ETHRXD
27	N.C.	28	RSTXD2
29	N.C.	30	RSRXD2
31	ETHTXEN	32	N.C.
33	nRSRTS2	34	N.C.
35	N.C.	36	N.C.
37	BINPACKb	38	N.C.

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TABLE 5-5. P6: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
1	N.C.	2	N.C.
3	GND	4	N.C.
5	TAb	6	TEAb
7	VFLS0	8	FCSb
9	VFLS1	10	BCSRCSb
11	BADDR28	12	DRMCS1b
13	BADDR29	14	DRMCS2b
15	BADDR30	16	SDRMCSb
17	ASb	18	CS5b
19	N.C.	20	CS6b
21	N.C.	22	CS7b
23	BGb	24	BS0Ab
25	BBb	26	BS1Ab
27	BRb	28	BS2Ab
29	BIb	30	BS3Ab
31	GPL5Bb	32	WE0b
33	BURSTb	34	WE1b
35	RWb	36	WE2b
37	TSb	38	WE3b

TABLE 5-6. P7: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
1	N.C.	2	N.C.
3	GND	4	N.C.
5	EXTCLK	6	ALEA
7	N.C.	8	IRQ2b
9	AT1	10	IRQ3b
11	N.C.	12	DP0

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TABLE 5-6. P7: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
13	RESETA	14	DP1
15	POEAb	16	DP2
17	MODCK1	18	DP3
19	MODCK2	20	FRZ
21	RPORIb	22	SPKROUT
23	RSTCNFb	24	BVS1
25	HRESETb	24	BVS2
27	SRESETb	28	BWP
29	N.C.	30	BCD2b
31	BWAITAb	32	BCD1b
33	GPL4Ab	34	BBVD2
35	N.C.	36	BBVD1
37	CE1Ab	38	BRDY

TABLE 5-7. P8: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
1	N.C.	2	N.C.
3	GND	4	N.C.
5	IRQ1b	6	MIITXCLK
7	NMIb	8	MPCMDIO
9	MIITXD1	10	MIICRS
11	MIITXD2	12	MIITXEN
13	MIITXD3	14	MIICOL
15	MIIRXDV	16	N.C.
17	MIIRXERR	18	N.C.
19	MIIRXCLK	20	N.C.
21	MIITXD0	22	N.C.

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TABLE 5-7. P8: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
23	MIIRXD0	24	RSRXD1
25	MIITXERR	26	RSTXD1
27	MPCMDC	28	N.C.
29	MIIRXD1	30	N.C.
31	MIIRXD2	32	PB28
33	MIIRXD3	34	PB29
35	N.C.	36	PB30
37	PB15	38	PB31

TABLE 5-8. P11: Logic Analyzer Interconnect Signals

Pin#	MPC852T Signal Name	Pin#	MPC852T Signal Name
1	N.C.	2	N.C.
3	GND	4	N.C.
5	REGAb	6	TSIZ1
7	D0	8	D16
9	D1	10	D17
11	D2	12	D18
13	D3	14	D19
15	D4	16	D20
17	D5	18	D21
19	D6	20	D22
21	D7	22	D23
23	D8	24	D24
25	D9	26	D25
27	D10	28	D26
29	D11	30	D27
31	D12	32	D28
33	D13	34	D29
35	D14	36	D30

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TABLE 5-8. P11: Logic Analyzer Interconnect Signals

Pin#	*MPC852T Signal Name*	*Pin#*	*MPC852T Signal Name*
37	D15	38	D31

TABLE 5-9. P15: Logic Analyzer Interconnect Signals

Pin#	*MPC852T Signal Name*	*Pin#*	*MPC852T Signal Name*
1	N.C.	2	N.C.
3	GND	4	N.C.
5	EPP_CLK	6	N.C.
7	PP_INTb	8	HRESETb
9	BDM_DSCK	10	PP_AD7
11	BDM_DSDI	12	PP_AD6
13	PP_WEb	14	PP_AD5
15	VFLSP0	16	PP_AD4
17	FRZ	18	PP_AD3
19	VFLSP1	20	PP_AD2
21	VFLS0	22	PP_AD1
23	VFLS1	24	PP_AD0
25	SRESETb	24	PP_BUSY_OUT
27	RPORIb	28	PP_RSTb
29	N.C.	30	PP_ASTRb
31	N.C.	32	PP_DSTRb
33	N.C.	34	BDM_DSDO
35	N.C.	36	N.C.
37	N.C.	38	N.C.

5•1•3 P5: PCMCIA Port Connector

P5 is a male, 68-pin, 90º, PC Card port connector type. The connector signals are presented in TABLE 5-10. "P5: PCMCIA Connector Interconnect Signals" below

TABLE 5-10. P5: PCMCIA Connector Interconnect Signals

Pin No.	Signal Name	Attribute	Description
1	GND		*Ground*
2	PCCD3	I/O	PCMCIA Data line 3
3	PCCD4	I/O	PCMCIA Data line 4
4	PCCD5	I/O	PCMCIA Data line 5
5	PCCD6	I/O	PCMCIA Data line 6
6	PCCD7	I/O	PCMCIA Data line 7
7	BCE1Ab	O	PCMCIA *Chip Enable* 1: active/low and enables EVEN-numbered address bytes.
8	PCCA10	O	PCMCIA Address line 10
9	OE~	O	PCMCIA *Output Enable* Signal: active/low and enables data outputs from PC Card during memory read cycles.
10	PCCA11	O	PCMCIA Address line 11
11	PCCA9	O	PCMCIA Address line 9
12	PCCA8	O	PCMCIA Address line 8
13	PCCA13	O	PCMCIA Address line 13
14	PCCA14	O	PCMCIA Address line 14
15	WE~/PCM~	O	PCMCIA *Memory Write Strobe*: active/low and strobes data to PC Card during memory write cycles.
16	CRDY	I	PC Card *+Ready/-Busy Signal*: allows PC Card to stall host access when a previous access' processing is incomplete.
17	PCCVCC	O	*PC Card 5V VCC* is switched by the MPC852TADS via BCSR1.
18	PCCVPP	O	12V/5V *VPP for PC Card* programming: 12V available only if applied to P13 in MPC852TADS, controlled via BCSR1.
19	PCCA16	O	PCMCIA Address line 16
20	PCCA15	O	PCMCIA Address line 15
21	PCCA12	O	PCMCIA Address line 12
22	PCCA7	O	PCMCIA Address line 7
23	PCCA6	O	PCMCIA Address line 6
24	PCCA5	O	PCMCIA Address line 5
25	PCCA4	O	PCMCIA Address line 4
26	PCCA3	O	PCMCIA Address line 3

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TABLE 5-10. P5: PCMCIA Connector Interconnect Signals

Pin No.	Signal Name	Attribute	Description
27	PCCA2	O	PCMCIA Address line 2
28	PCCA1	O	PCMCIA Address line 1
29	PCCA0	O	PCMCIA Address line 0
30	PCCD0	I/O	PCMCIA Data line 0
31	PCCD1	I/O	PCMCIA Data line 1
32	PCCD2	I/O	PCMCIA Data line 2
33	CWP	I	PC Card *Write Protect* indication
34	GND		*Ground*
35	GND		*Ground*
36	CCD1b	I	*Card Detect 1*~: active/low. Indicates, with CCD2b, that a PC Card is correctly placed in a socket.
37	PCCD11	I/O	PCMCIA Data line 11
38	PCCD12	I/O	PCMCIA Data line 12
39	PCCD13	I/O	PCMCIA Data line 13
40	PCCD14	I/O	PCMCIA Data line 14
41	PCCD15	I/O	PCMCIA Data line 15
42	BCE2Ab	O	PCMCIA *Chip Enable 2*: active/low and enables ODD-numbered address bytes.
43	CVS1	I	PC Card *Voltage Sense 1*: indicates, with CVS2, the PC Card's operational voltage.
44	IORD~	O	*I/O Read*: active/low and drives data bus during I/O-Card read cycles.
45	IOWR~	O	*I/O Write*: active/low and strobes data to the PC-Card during I/O-Card write cycles.
46	PCCA17	O	PCMCIA Address line 17
47	PCCA18	O	PCMCIA Address line 18
48	PCCA19	O	PCMCIA Address line 19
49	PCCA20	O	PCMCIA Address line 20
50	PCCA21	O	PCMCIA Address line 21
51	PCCVCC	O	*PC Card 5V VCC* is switched by the MPC852TADS via BCSR1.
52	PCCVPP	O	*12V/5V VPP for PC Card* programming: 12V only available if applied to P13, Controlled by the MPC852TADS via BCSR1.
53	PCCA22	O	PCMCIA Address line 22
54	PCCA23	O	PCMCIA Address line 23

TABLE 5-10. P5: PCMCIA Connector Interconnect Signals

Pin No.	Signal Name	Attribute	Description
55	PCCA24	O	PCMCIA Address line 24
56	PCCA25	O	PCMCIA Address line 25
57	CVS2	I	PC Card *Voltage Sense 2*: indicates, with CVS1, the PC Card operational voltage.
58	RESETA	O	PC Card *Reset* signal
59	CWAITAb	I	PC Card *Cycle Wait*: active/low
60	CINPACKb	I	*Input Port Acknowledge*: active/low. Indicates PC Card's ability to respond to I/O access of a certain address.
61	PCREGb	O	Attribute Memory or I/O Space - Select: active/low. For selecting either attribute (card-configuration) memory or I/O space.
62	CBVD2	I	*Battery Voltage Detect 2*: used, with CBVD1, to indicate the PC Card's battery condition.
63	CBVD1	I	*Battery Voltage Detect 1*: used, with CBVD2, to indicate the PC Card's battery condition.
64	PCCD8	I/O	PCMCIA Data line 8
65	PCCD9	I/O	PCMCIA Data line 9
66	PCCD10	I/O	PCMCIA Data line 10
67	CCD2b	I	*Card Detect 2*~: active/low. Indicates, with CCD1b, the correct placement of a PC Card in a socket.
68	GND		*Ground*

5•1•4 P9, P10: 100/10BaseT Ethernet Port Connector

The MPC852TADS's P9, P10 connectors are twisted-pair 100/10-Base-T compatible connector. P9, P10 connectors are used with an 8-pin 90^{o} RJ45 connectors. The connectors signals are described in TABLE 5-11. "P9, P10: 100/

10Base-T Ethernet Port Interconnect Signals" below.

Note: **output** indicates data leaving the MPC852TADS whereas **input** indicates data entering the MPC852TADS.

TABLE 5-11. P9, P10: 100/10Base-T Ethernet Port Interconnect Signals

Pin No.	*Signal Name*	*Description*
1	TPTX	MPC852TADS *Twisted-Pair Transmit Data* **positive output**
2	TPTX~	MPC852TADS *Twisted-Pair Transmit Data* **negative output**
3	TPRX	MPC852TADS *Twisted-Pair Receive Data* **positive input**
4	-	Not connected
5	-	Not connected
6	TPRX~	MPC852TADS *Twisted-Pair Receive Data* **negative input**
7	-	Not connected
8	-	Not connected

5•1•5 P12: External Debug Port Controller Input Interconnect

P12 is a male, 10-pin header connector. The connector signals are outlined in TABLE 5-12. "P12: External Debug

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Port Controller Input Interconnect Signals" below

TABLE 5-12. P12: External Debug Port Controller Input Interconnect Signals

Pin No.	*Signal Name*	*Attribute*	*Description*
1	VFLS0	O	*Visible History Flushes Status 0*. Indicates, with VFLS1, the number of instructions flushed from the core's history buffer and if the MPC is in debug mode. If debug port not used then may be configured for alternate function.
2	SRESET~	I/O	MPC's *Soft Reset* line: active/low and open-drain.
3	GND		*Ground*
4	CON_DSCK	I/O	*Debug Serial Clock*. Over its rising edge the MPC samples, from the DSDI signal, the serial date. Over its falling edge the DSDI is driven to the MPC and the MPC drives DSDO. Configured on the MPC's JTAG port. **Output** - when debug port controller is on the local MPC. **Input** - when disconnected from the ADS.
5	GND		*Ground*
6	VFLS1	O	*See VFLS0*.
7	HRESET~	I/O	MPC's *Hard Reset* line: active/low and open-drain.
8	CON_DSDI	I/O	Debug Port's *Debug Serial Data In*. Configured on the MPC's JTAG port. **Output** - when debug port controller is on the local MPC. **Input** - when disconnected from the ADS.
9	V3.3	O	*3.3V Power indication*. An indicatory line from which no significant power may be drawn.
10	CON_DSDO	I/O	MPC's *Debug Serial Data Output.* Configured on the MPC's JTAG port. **Output** - when debug port controller is on the local MPC.

5•1•6 P13: 12V Power-In Connector

The P13 is a 2-lead, 2-part, terminal block connector. The P13 supplies, when necessary, programming voltage to the Flash SIMM and / or to the PCMCIA.

TABLE 5-13. P13: 12V Power-In Interconnect Signals

Pin Number	*Signal Name*	*Description*
1	12V	12V input from an external power supply.
2	GND	GND line from an external power supply.

5•1•7 P14: BNC Connector

P14 is a BNC connector that drives the clock into the MPC EXTCLK pin. Users may use this connector but only after connecting J1 pins 2-3. J1 Pins 1-2 are connected by default in the factory.

5•1•8 P16: 2.1 mm Power Jack 5V Connector

P16 is a 2.1 mm Plug Jack connector connected to the board's power supply. To operate the board users must plug the 5V power supply's connector into the P16 connector.

5•1•9 P17: RS232 Dual Port Connector

P17A (1-down) and P17B (2-up) connectors are female, 9-pin, 90°, D-type stacked connectors. The connector signals are outlined TABLE 5-14. "P17B: RS232 Interconnect Signals" below.

Note: **output** indicates data leaving the MPC852TADS whereas **input** indicates data entering the MPC852TADS.

TABLE 5-14. P17B: RS232 Interconnect Signals

Pin No.	*Signal Name*	*Description*
1	CD	MPC852TADS *Carrier Detect* **output**
2	TX	MPC852TADS *Transmit Data* **output**
3	RX	MPC852TADS *Receive Data* **input**
4	DTR	MPC852TADS *Data Terminal Ready* **input**
5	GND	MPC852TADS *Ground Signal*
6	DSR	MPC852TADS *Data Set Ready* **output**
7	RTS (N.C.)	*Request To Send* - not connected in the MPC852TADS
8	CTS	MPC852TADS *Clear To Send* **output**
9	-	Not connected

In P17A only RX and TX signals are existed.

5•1•10 P18, P19: Altera programming ISP Connectors

P18, P19 are 10-pin generic 0.100" pitch header connector that provide In-System Programming capability for the board's Altera-made programmable logic U8 - BCSR and U17 - BDM to EPP I/F respectively. The pinout is shown

in TABLE 5-15. "P18, P19 - JTAG connector for Altera programing." below:

TABLE 5-15. *P18, P19 - JTAG connector for Altera programing.*

Pin No.	Pin Name	Attribute	Description
1	TCK	I	*Test Port Clock*. The clock shifts data in/out and to/from the programmable logic JTAG chain.
2	GND	O	*Digital GND*. Main GND plane.
3	TDO	O	*Transmit Data Output*. The programmable logic JTAG serial data output is driven by the TCK's falling edge.
4	V3U3	O	*3.3V Power Supply Bus*
5	TMS	I	*Test Mode Select*. The signal, qualified with TCK, changes the state of the programmable logic JTAG machine
6	N.C.	-	Not connected
7	N.C.	-	Not connected
8	N.C.	-	Not connected
9	TDI	I	*Transmit Data In*. The programmable logic JTAG serial data input.
10	GND	O	*Digital GND*. Main GND plane.

5•1•11 P20: Parallel Host Port Connector

The Parallel Host port connector - P20 is a D-Type 25 pins male connector. It should be connected to IEEE 1284 - 1994 cable. For Serial transfer mode the signals are presented in TABLE 4-22. "Parallel Host Port Connector's Signal Description with Serial Command Converter I/F" below. For EPP transfer mode the signals are presented in TABLE 4-21. "Parallel Host Port Connector's Signal Description with EPP I/F" below.

5•2 MPC852TADS Parts Listing

This section lists the MPC852TADS's Bill of Material according to reference designations.

TABLE 5-16. MPC852TADS Part List

Reference Designation	Part Description	Manufacturer	Part #
C1-C28,C32-C58,C60-C69,C71, C75,C76,C78-C81,C83,C84,C108-C112, C114,C115,C117,C118,C120, C121,C123,C125-C127,C129, C131, C133,C135-C138,C142, C143,C145-C147,C149-C154, C156,C158,C159,C163-C166, C168,C169,C171,C173,C174, C177-C180,C182-C184,C189, C191-C193,C195,C197-C200, C202,C203,C205-C207,C209, C212-C214,C216,C218-C224, C231-C234,C236,C238,C242-C244, C247,C248,C250-C253,C265, C267,C268,C270	100NF(0.1uF)16V 10% X7R 0603	EPCOS	0603X7R104K016P07
C29,C30,C59,C72	10UF 25V 10% SMD C TANT	SPRAGUE	293D106X9025C2T
C31,C87,C124,C157	0.01uF 2KV X7R 1825 10% SMD	JOHANSON DIELECTRIC	202S49W103KV4E
C70,C73,C204,C228,C246	1uF 25V 10% SMD A TANT	SPRAGUE	293D105X9025A2T
C74	120PF 50V 5% SMD COG 1206	AVX	1206 5A 121 JTR
C82	10NF 50V 10% NPO 1210	VITRAMON	VJ1210A103KXAT
C85,C240	47UF 16V 10% SIZE D	AVX	TAJD476K016
C86	100UF/10V TNT D SMT 10%	SIEMENS	B45196-H2107K
C88-C105,C210,C211,C215,C217,C226, C227,C229,C230,C235,C241,C256-C263	1nF 50V 5% X7R 0603 SMD	AVX	06035C102JAT
C113,C116,C119,C122,C128,C130,C132, C134,C139-C141,C144,C148,C155,C160, C167,C170,C172,C175,C190,C201,C245, C249,C254,C255,C264,C266,C269,C271	0.01UF (10nF) 50V 10% SMD X7R 0603	AVX	06035C103KAT2A
C181,C186,C187,C194,C237	10uF 10V 10% SIZE A TANT SMD CAP	SPRAGUE	293D106X9010A2T
C196	68UF 20V 20% SIZE D or E CAP	SPRAGUE	293D686X9020E2T
C225	100pF 50V 10% 0603 SMD	AVX	06035A101KAT2A
C239	1UF 16V SMD 10% X7R 1206	AVX	1206YC105KAT1A
D1,D9	MBRD620CT	ON SEMICONDUCTOR	MBRD620CT
D2	DIODE 1SMC5.OAT3	ON SEMICONDUCTOR	1SMC5.OAT3
D3	DIODE 1SMC12AT3	ON SEMICONDUCTOR	1SMC12AT3
D4-D8	LL4004	TSC	LL4004G
F1	SMD150/33-2	RAYCHEM	FSMD150/33-2
F2	SMD260 POLYSWITCH 5.2A	RAYCHEM	FSMD260
JP1-JP4, JP7	GND Bridge	PRECIDIP	PD9991111210
JP5-JP6	BRIDGE	MOLEX	87156-4003
J1	3 PIN SINGLE ROW	MOLEX	87156-0303

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TABLE 5-16. MPC852TADS Part List

Reference Designation	Part Description	Manufacturer	Part #
LD1,LD4,LD5,LD16,LD18,LD19	LED_GREEN	KINGBRIGHT	KPT-3216SGD
LD2,LD6	LED_RED	KINGBRIGHT	KPT-3216ID
LD3,LD7-LD15,LD17,LD20,LD21	LED_YELLOW	KINGBRIGHT	KPT-3216YD
L1	PT12133 8,2MH INDUCTOR	BOURNS	PT12133
L2	ACM1110-102-2P COMMON MODE CHOCK COIL TO DC LIN	TDK	ACM1110-102-2P
L3, L5-L8	FERRITE NFM60R30T222T	MURATA	NFM60R30T222T1
L4,L9-L34	BLM18AG121SN1 CHIP FERRITE BID 120 OHM 0603	MURATA	BLM18AG121SN1
P1,P2	CONN-96 96P DIN C F 90'PC+TAIL	ELCO	268477096002025
P3,P4,P6-P8,P11,P15	MICTOR38 38P LOG ANL MICTOR CON	AMP	2-767004-2
P5	PCMCIA TOP 90'SMD CON	AMP	AMP 822021-5
P9,P10	8P RJ45 90'PC MODULAR JACK	MOLEX	43202-8110/8919
P12,P18,P19	10PIN TERM STRIP SHORT SMD 5X2	SAMTEC	TSM10501-SDV AP
P13	PWR2 2PIN PC STRGHT POW CON	WIELEND BAMBERG	8113S253303253
P14	SMB Straight Jack for PCB	SUHNER	82SMB-50-0-1/111
P16	POWER JACK 2.1mm	SWITCHCRAFT	RAPC722
P17	RS232 - 9P DUAL F/90'DCON+TAIL	EDA	8LE009009D306H
P20	CON D-Type. 25P D 90'+TAIL M 7.2/8.08mm	KCC	DNR 25P CB SG
Q1-Q3	MMDF3N03HD	ON SEMICONDUCTOR	MMDF3N03HD
Q4	MMDF4N01HD	ON SEMICONDUCTOR	MMDF4N01HD
RN1-RN16,RN19-RN33,RN35,RN38,RN40	22ohm 5% 4R 8P SMD CHIP RE NETW	AVX	CRA3A4E220JT
RN17,RN18,RN34,RN36,RN37,RN39, RN41,RN43-RN48	10K 5% 8R 10P SMD CHIP RE NETW	ROHM	RS8A1002J-OR-MNR15EORPJ103
RN42	1K 5% 8R 10P SMD CHIP RE NETW	ROHM	RS8A1001J-OR-MNR15EORPJ102
R1,R3,R6,R34,R41-R43,R48,R49, R52,R54,R55,R59,R64,R69-R71, R76,R79,R87,R89,R94,R97,R106-R109, R136,R137,R141,R143,R145, R147,R148,R151,R153,R155-R158	10K 1% 0.1W 0603 SMD T/R	ROEDERSTEIN	D11 010KFCS
R2,R8,R62,R67,R72,R74,R117,R128, R132,R134,R135,R140	22.1ohm 1% 0.1W 0603 SMD T/R	ROEDERSTEIN	D11 22R1FCS
R4,R9	6.8K 1% 0603 SMD RES T/R	DALE	CRCW0603-6801F
R7,R39,R104	330ohm 1% 0603 SMD RES T/R	DALE	CRCW0603-3300F
R11-R13,R17-R19,R21-R23,R25,R28,R31, R37,R38,R95,R96,R112,R116,R121,R123, R126,R127,R129,R133	0 ohm 1% 0.1W 0603 SMD T/R	AVX	CJ10-000-T
R26	5.1K 5% 1/4W 1206 SMD	ROEDERSTEIN	D25 05K1JCS
R27,R36,R68,R120	100ohm 1% 0603 SMD RES T/R	DALE	CRCW0603-1000F

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TABLE 5-16. MPC852TADS Part List

Reference Designation	Part Description	Manufacturer	Part #
R32,R35,R45,R46,R63,R65,R66, R73,R85,R90,R98,R113, R131,R142,R149,R150,R152, R154,R160	1K 1% 0603 SMD T/R	DRALORIK	D11 001KFCS
R33,R83	2.21K 1% 0603 SMD RES T/R	DALE	CRCW0603-2211FRT1
R40,R44,R105,R110,R111,R162-R165, R167-R175	150ohm 1% 0603 SMD RES T/R	DALE	CRCW0603-1500F
R47	510ohm 1% 0603 SMD RES T/R	DALE	CRCW0603-5100F
R50,R51,R77,R82	78.7ohm 1% 0603 SMD RES T/R	DALE	CRCW0603-78R7F
R53,R58,R88,R93,R122	49.9 OHM 1% SMD 0603 RES T/R	DALE	CRCW0603-49R9F
R56,R57,R60,R61,R80,R81,R86,R91,R92	75 ohm 1% 0603 SMD T/R	DRALORIK	D11 075RFCS
R78	1.5K 1% 0603 SMD RES T/R	DALE	CRCW0603-1501F
R114	143 OHM 1% 1/8W 1206	ROEDERSTEIN	D25 143RFCS
R115	63.4ohm 1% 0603 SMD RES T/R	DRALORIK	D11 63R4FCS
R166	51.1ohm 1% 0.1W 0603 SMD T/	ROEDERSTEIN	D11 51R1FCS
SK1	SEP-1162 PIEZO SPEAKER	SOUNDTECH	SEP-1162
SW1	SINGLE TOGGLE SWITCH	C&K	1101M2S3CQE2
SW2	ABORT-BROWN PUSHBUTTON SMD	C&K	KT11P2SM-BROWN
SW3,SW6	SRESET and POWER ON RESET -RED PUSHBUTTON SMD	C&K	KT11P2SM-RED
SW4	SW DIP-2/SM 2POS 4PIN SEALD DIP SW. SMD	GRAYHIL	90HBW02PR
SW5	SW DIP-4/SM 4POS 8PIN SEALD DIP SW. SMD	GRAYHIL	90HBW04PR
U1_SOCKET	256 PIN BGA SOCKET FOR MPC852T	3M	2256A-1381-50-0001
U1	MPC852T	MOTOROLA	MPC852T
U2,U5	FAST ETHERNET/ETHERNET PHY	DAVICOM	DM9161E
U3,U6	TG22-3506ND TRANSFORMETR TG22-3506	HALO	TG22-3506ND
U4,U31	74LCX125D	ON SEMICONDUCTOR	74LCX125D
U7	LTC1315 DUAL PCMCIA VPP SWITCH	LINEAR TECH	LTC1315CG
U8	ALTERA CPLD FOR BCSR	ALTERA	EPM3256ATC144-7
U9	CY2309ZC-1H 3.3V ZD BUFFER 16P SOIC	CYPRESS SEMICONDUCTOR IDT	CY2309ZC-1H IDT 2309-1HDC
U10	LM317MT Regulator.	Motorola	LM317MT
U12,U18	MAX3241ECAI 28 SSOP	MAXIM	MAX3241ECAI/EEAI
U13,U34	74AC14D	ON SEMICONDUCTOR	74AC14D
U14	MIC29500-3.3BT TO220	MICREL	MIC29500-3.3BT
U15,U16	74LS244DW	ON-SEMICONDUCTOR	SN74LS244DW
U17	ALTERA CPLD FOR BDM to EPP I/F	ALTERA	EPM3128ATC100-10

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TABLE 5-16. MPC852TADS Part List

Reference Designation	*Part Description*	*Manufacturer*	*Part #*
U19	74LVX161284 LOW VOLTAGE EPP TRAN.	FAIRCHILD SEMICONDUCTOR	74LVX161284MTD
U20_SOCKET	SIMM72 4MB EDO DRAM_SOCKET	AMP	822021-4
U20 (*)	4MB EDO DRAM	TUSHIBA MICRON MICRON	THM3210CSG-60 MT2D132M-6X MT2D132M-60X
U21_SOCKET	SIMM80 FOR FLASH	AMP	822021-5
U21	2MB 55132T9DX SIMM FLASH	WHITE MICROELECTRONICS SOUTHLAND MICRO SYSTEM	WPF512K32-70PSC5T WPF512K32-70PSC5T WPF512K32-70PSC5T 55132T9DX
U22,U23,U26,U30,U36	SN74LVC32244GKER	TI	SN74LVC32244GKER
U24,U25,U29	SN74LVC32245GKER	TI	SN74LVC32245GKER
U27	SN74LVCH32373AGKER	TI	SN74LVCH32373AGKER
U28	MT48LC2M32B2TG-7 SDRAM 2MX32	MICRON	MT48LC2M32B2TG-8
U32	BUS SWITCH QUAD 2:1 MUX/DEMUX	IDT	IDT74CBTLV3257PG
U33	74LCX08	ON SEMICONDUCTOR	74LCX08D
U35	RESET CONTROLLER	SEIKO1	S-80828CNMC-B8N-T2
Y1	25Mhz 3V SMD 25PPM PROGRAMMING CLK OSC 7X5mm	CARDINAL COMPONENTS	CPPLC7LTBR-25.000MHZ-TS
Y2,Y3_SOCKET	8PIN SMD SOCKET FOR CLOCK OSCILLTOR	PRECIDIP	1109330841105
Y2	10MHz 3V TH 25PPM HS PROGRAMMING OSCILLTOR	CARDINAL COMPONENTS	CPPLC4LBP10.00MTS
Y3	40MHz 3V TH 25PPM HS PROGRAMMING OSCILLTOR	CARDINAL COMPONENTS	CPPLC4LBP40.00MTS

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APPENDIX A - Schematics

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FIGURE A-1 Bus Config Diagram

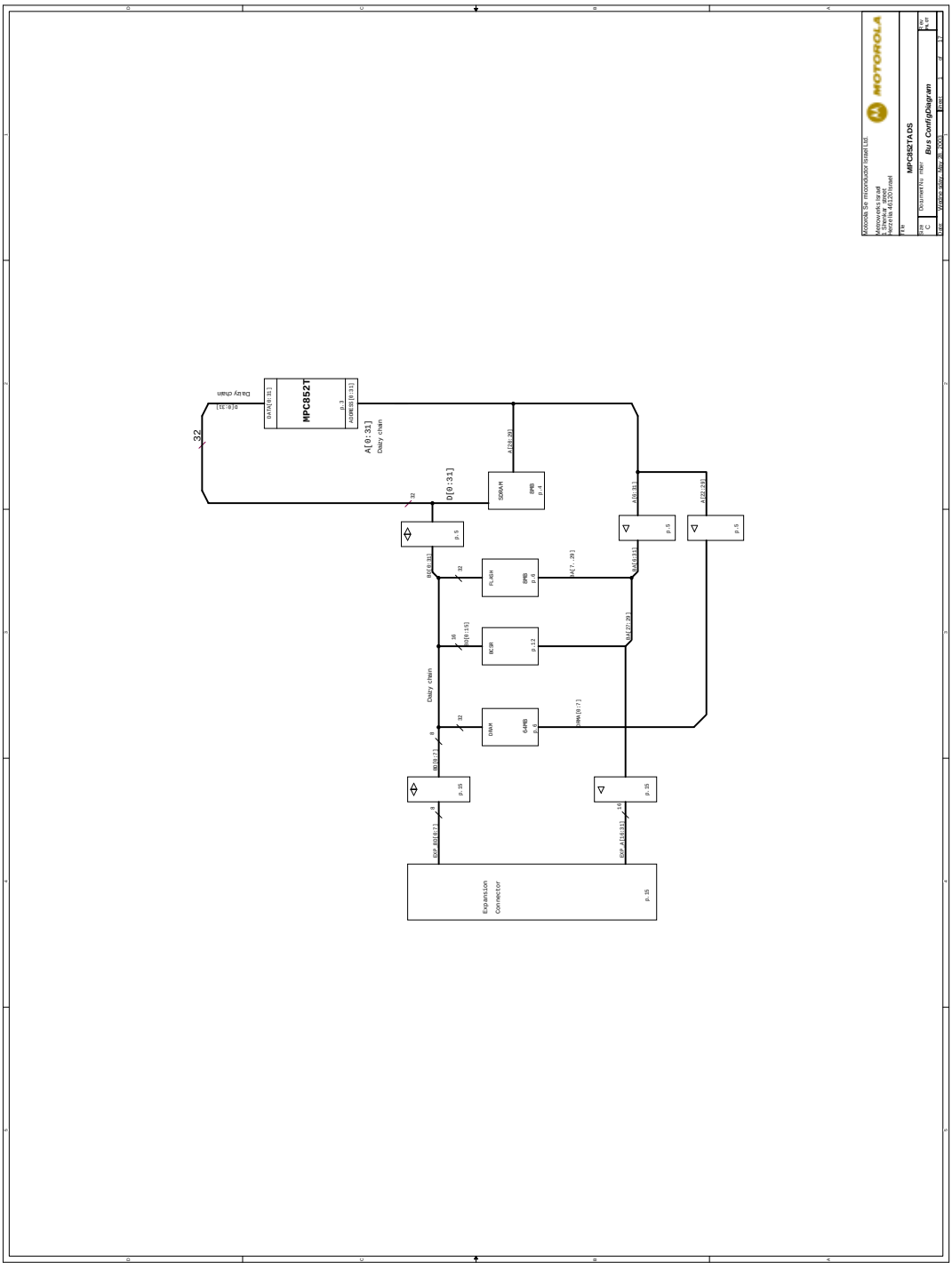

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FIGURE A-2 Table of Contents

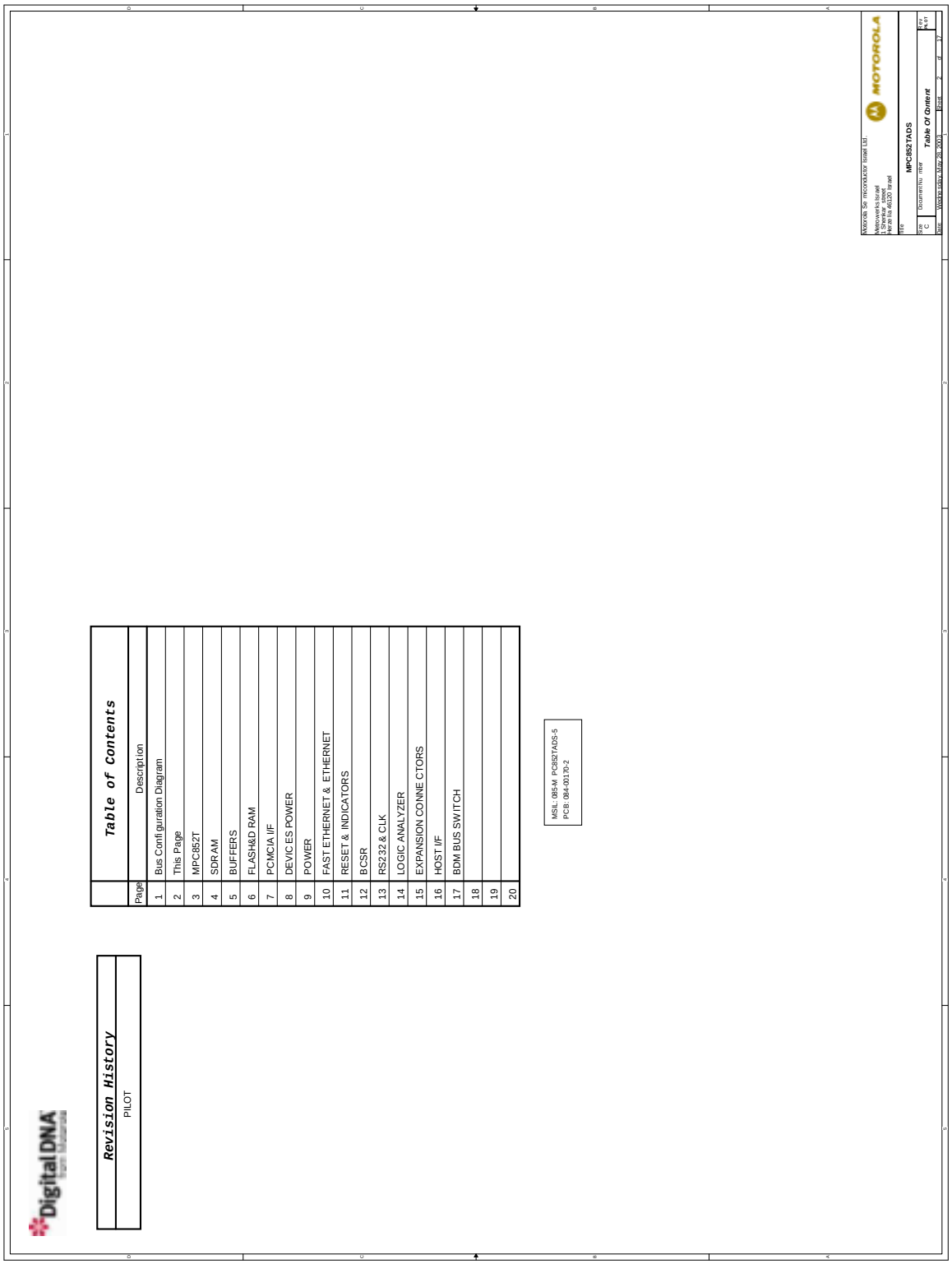

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FIGURE A-3 MPC852T

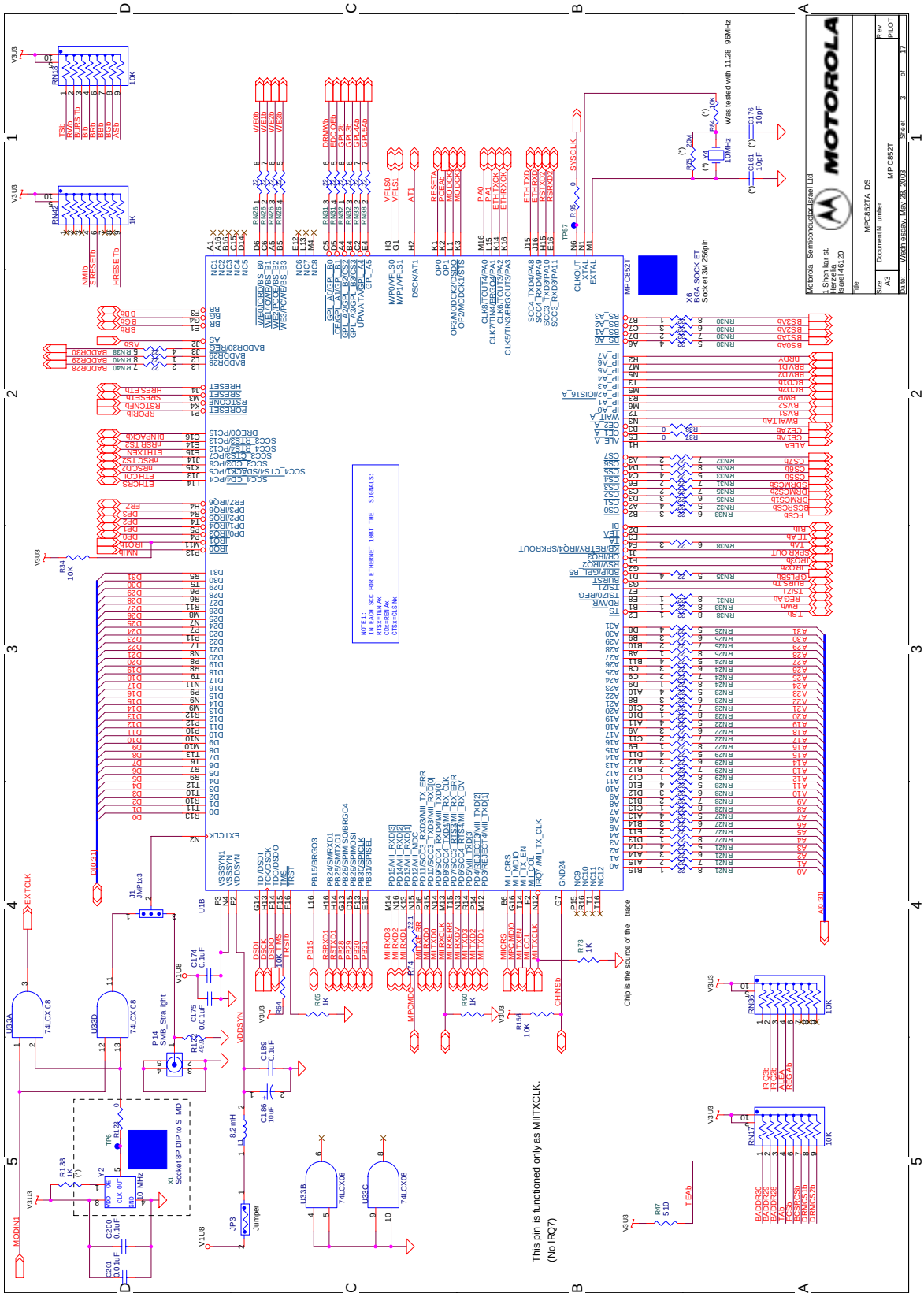

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FIGURE A-4 SDRAM

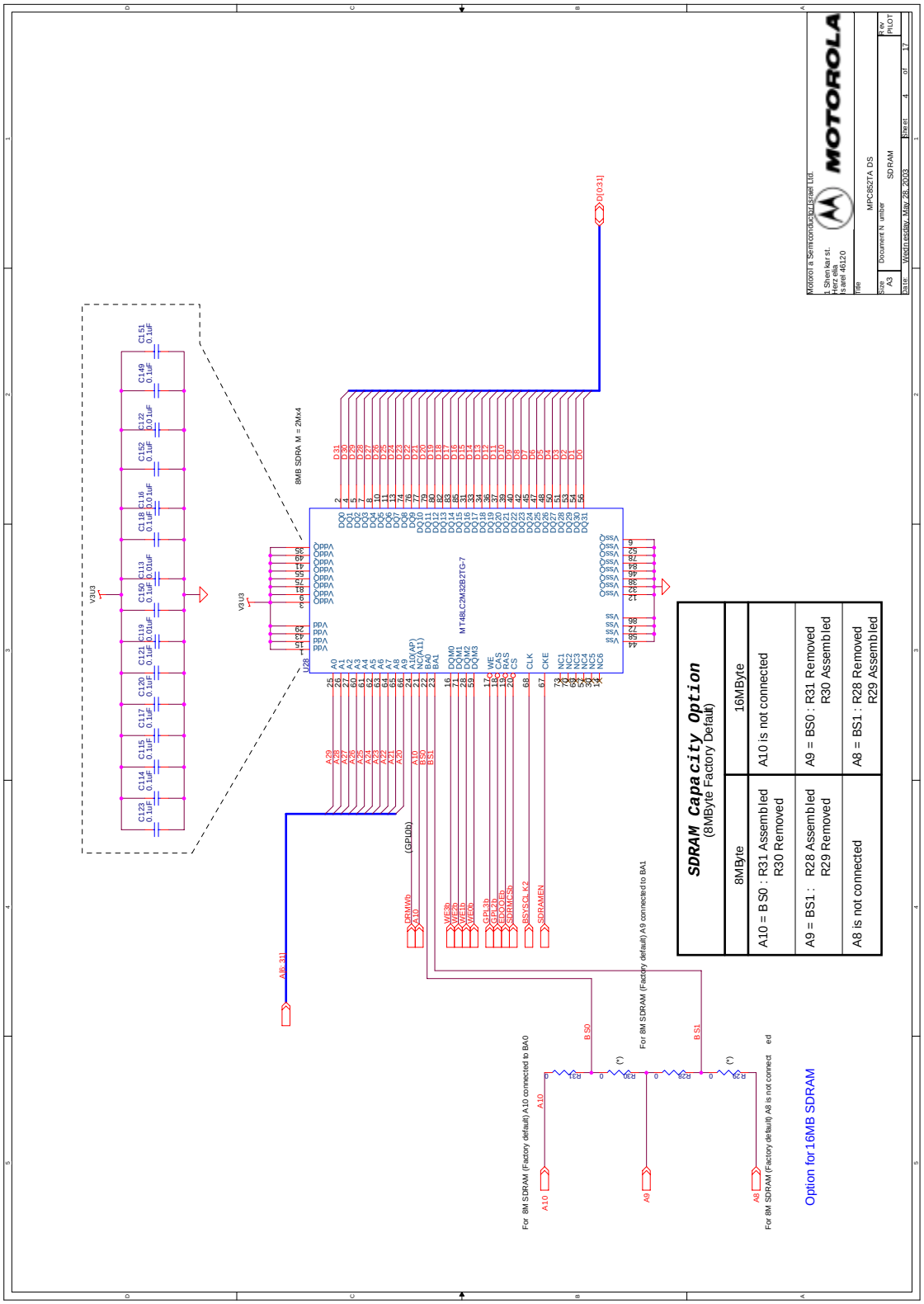

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FIGURE A-5 Buffers

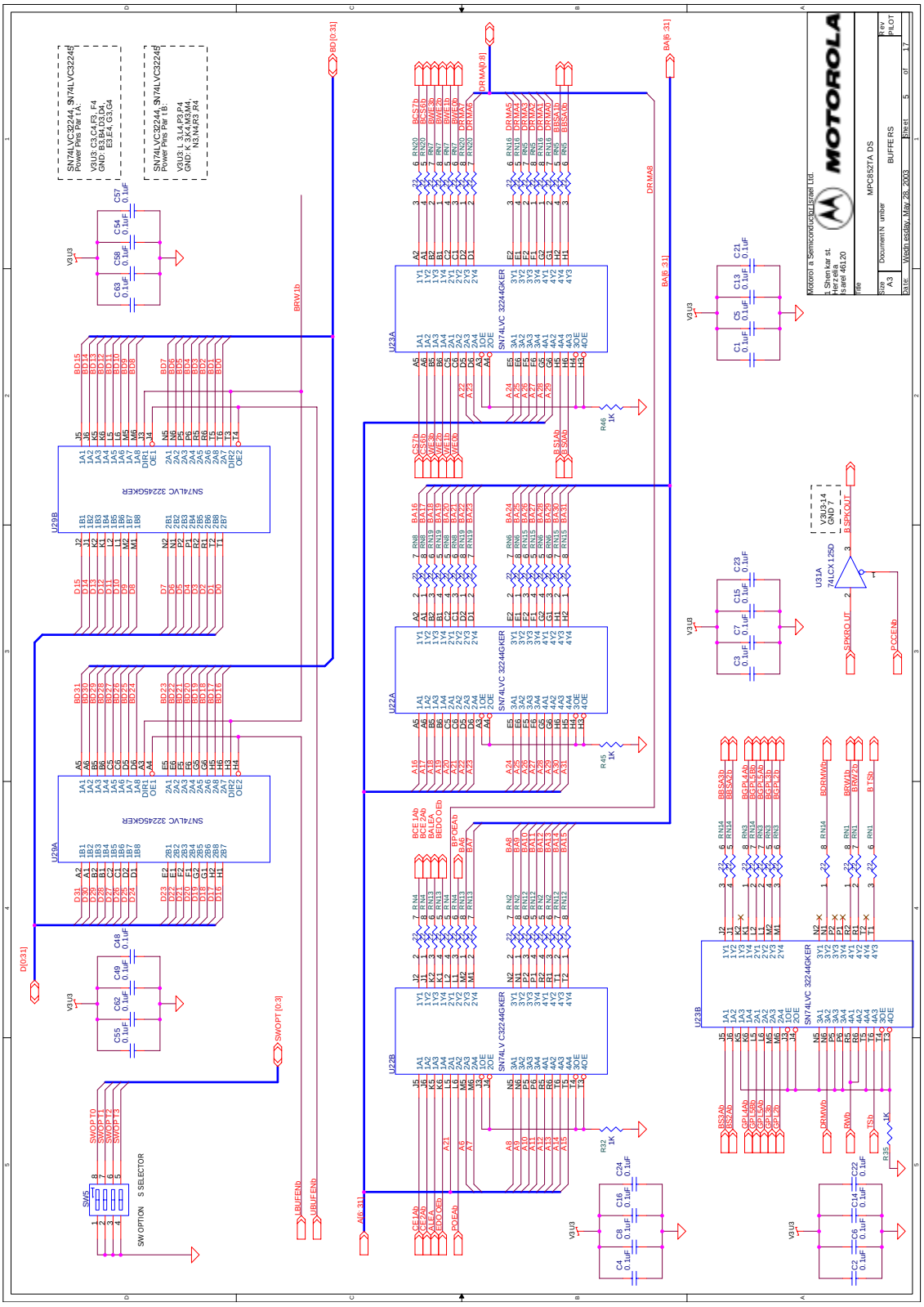

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FIGURE A-6 Flash & DRAM

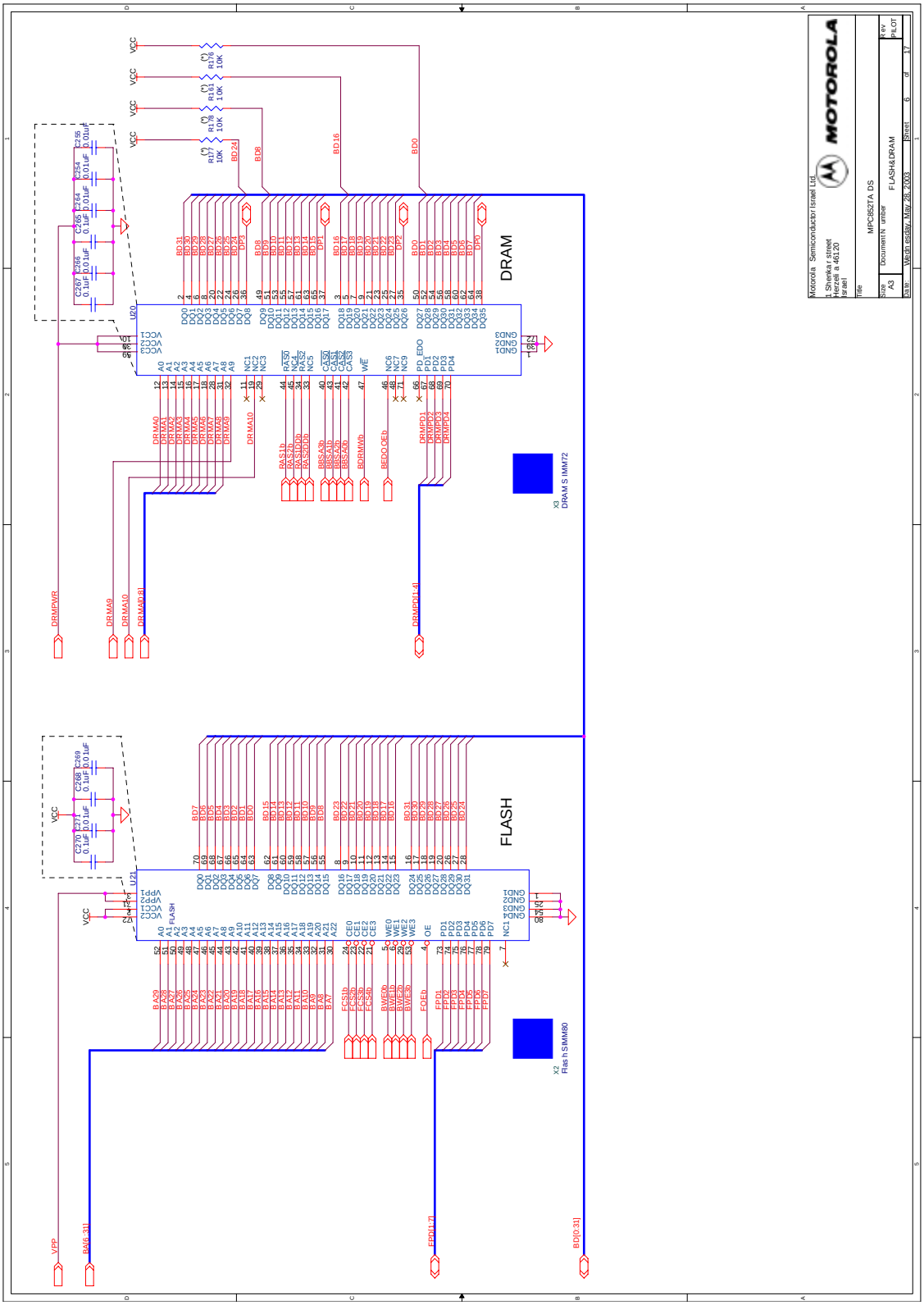

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FIGURE A-7 PCMCIA I/F

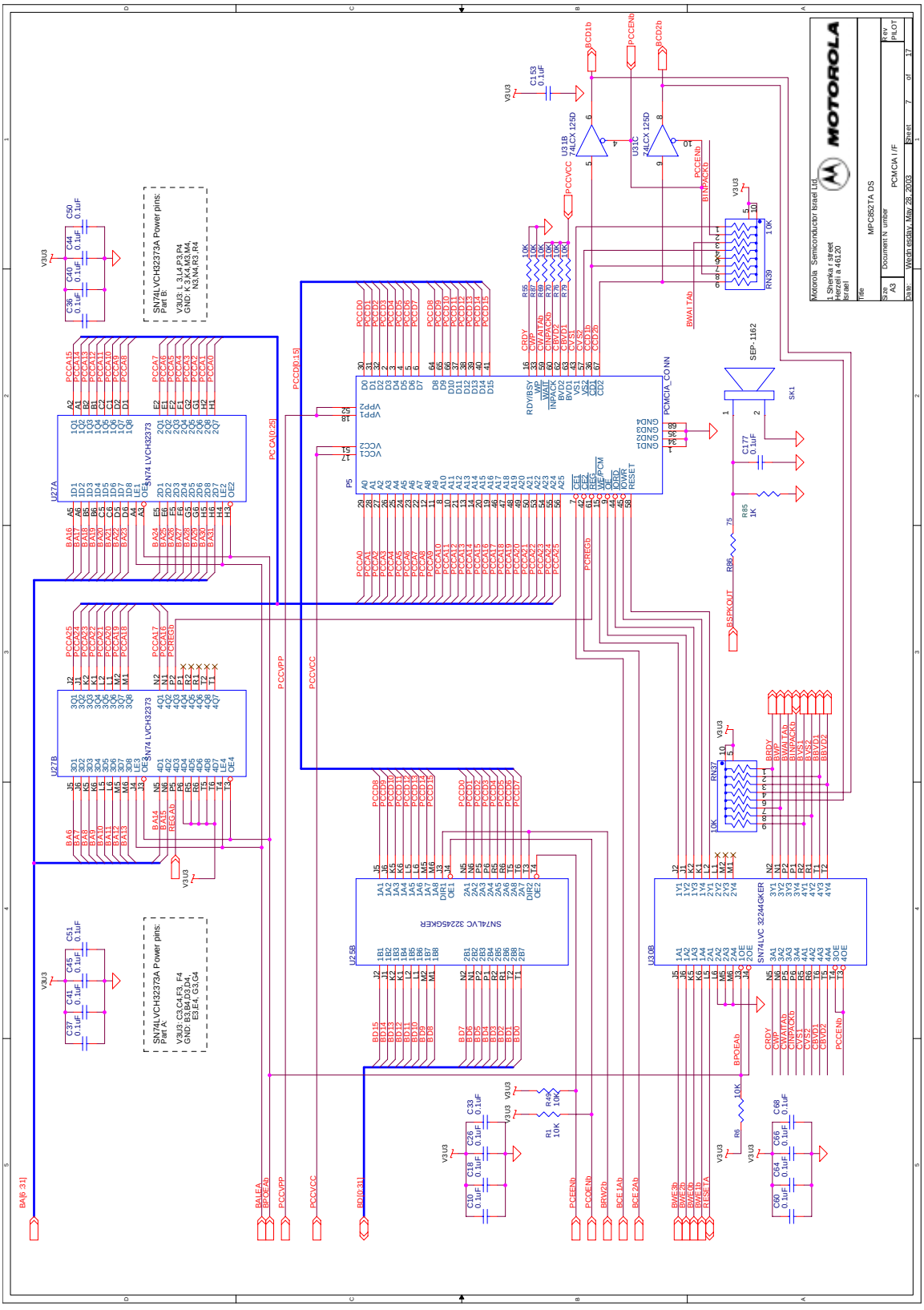

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FIGURE A-8 Devices Power

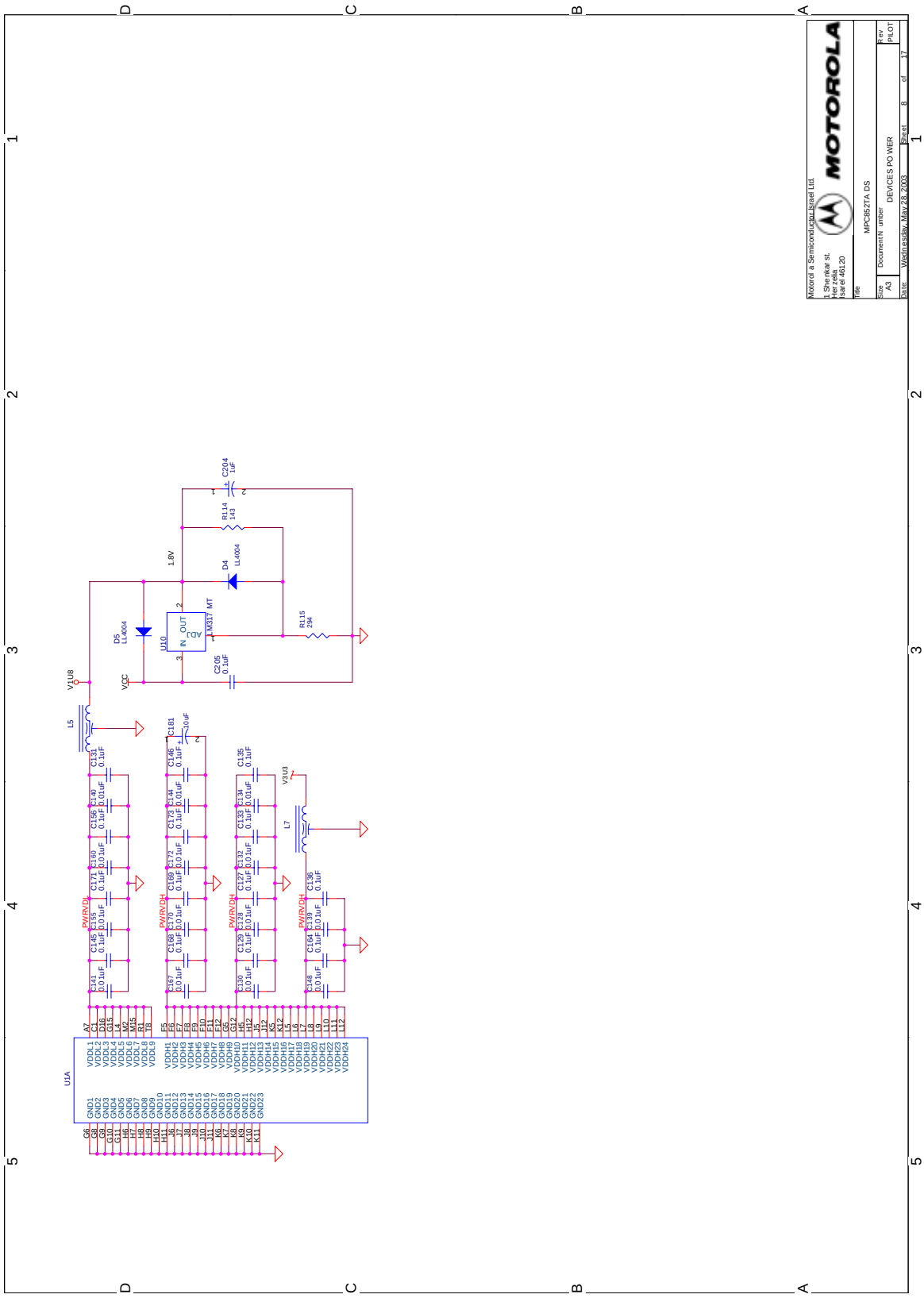

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FIGURE A-9 Power

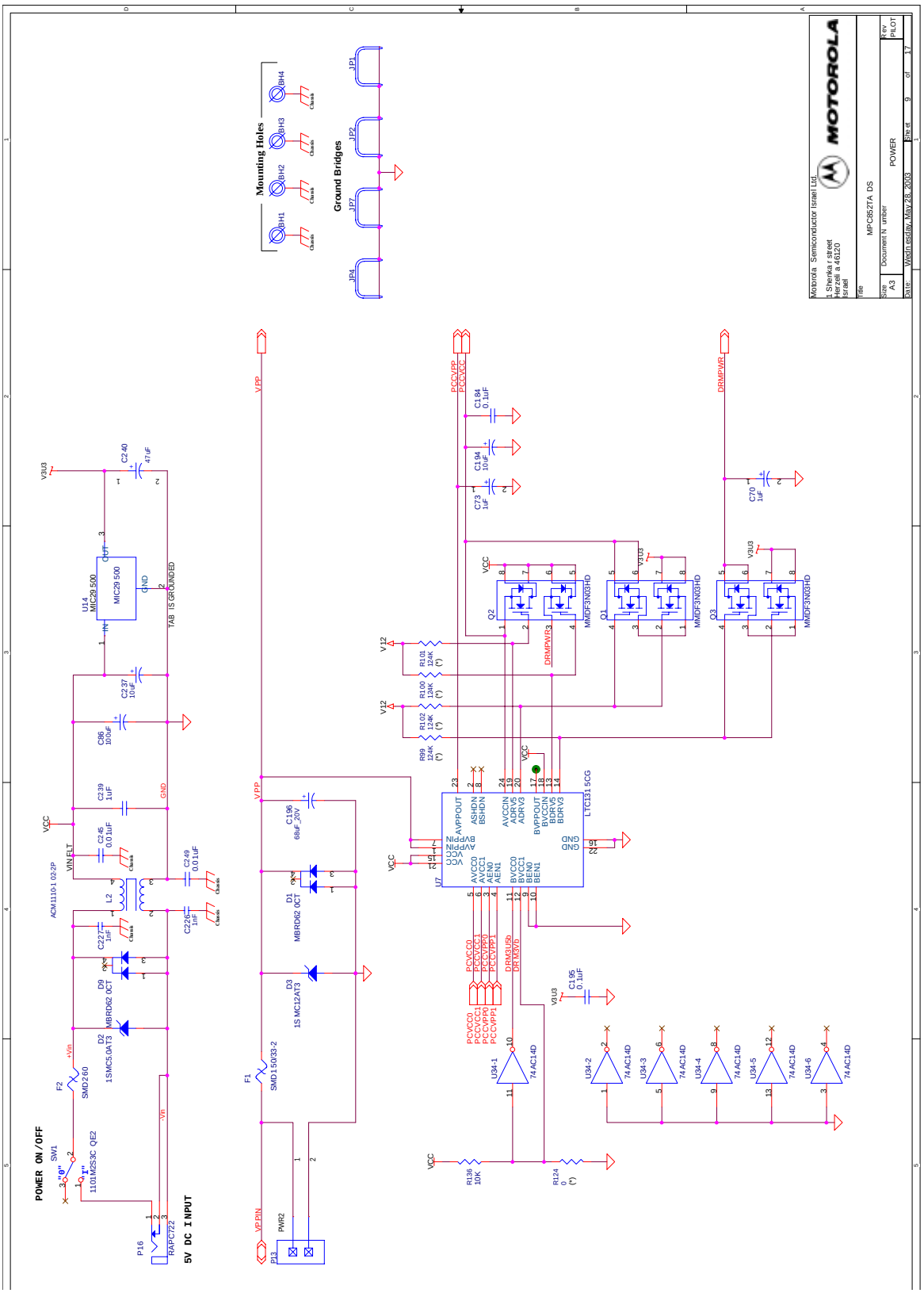

FIGURE A-10 Fast Ethernet & Ethernet

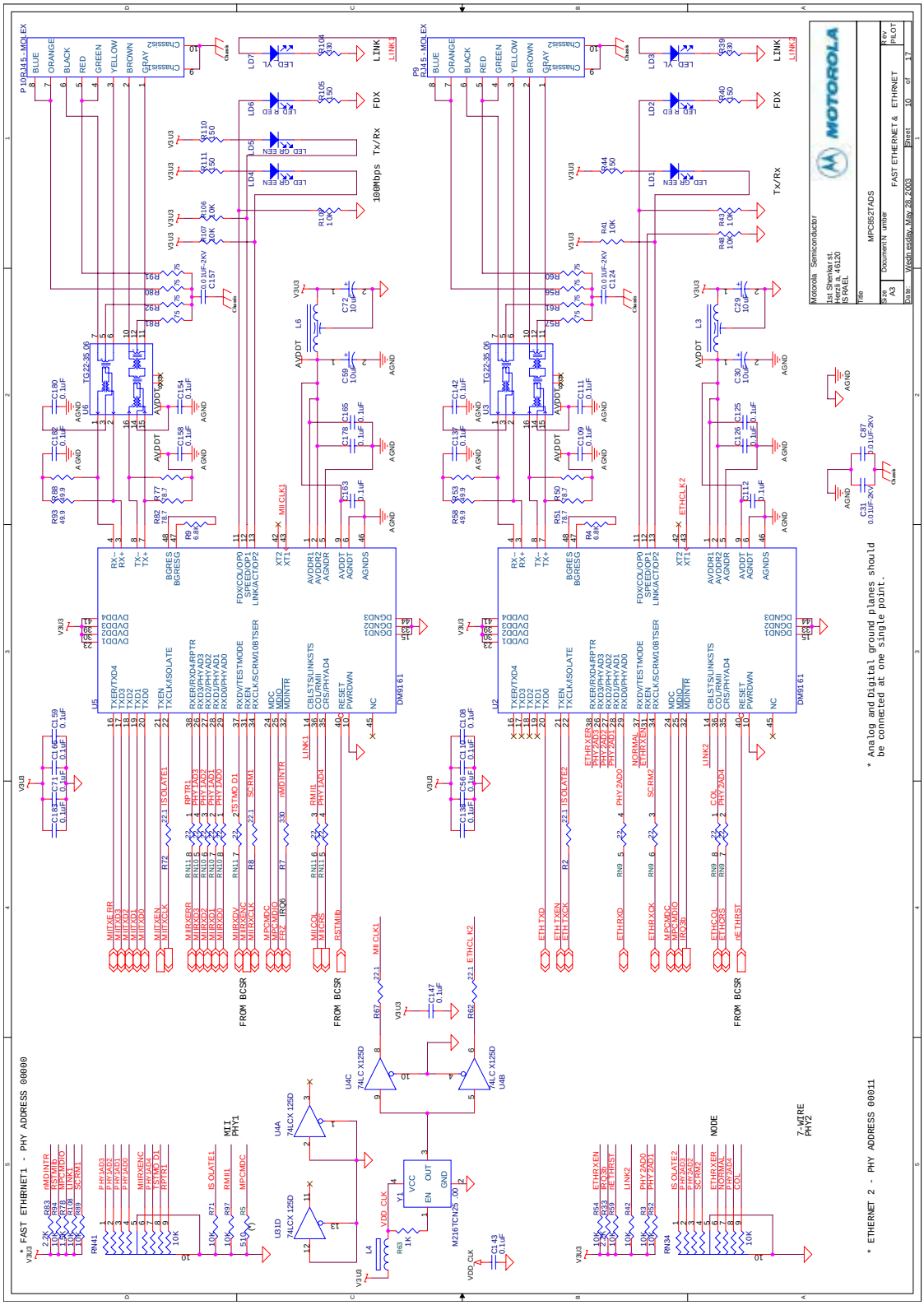

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FIGURE A-11 RESET & INDICATORS

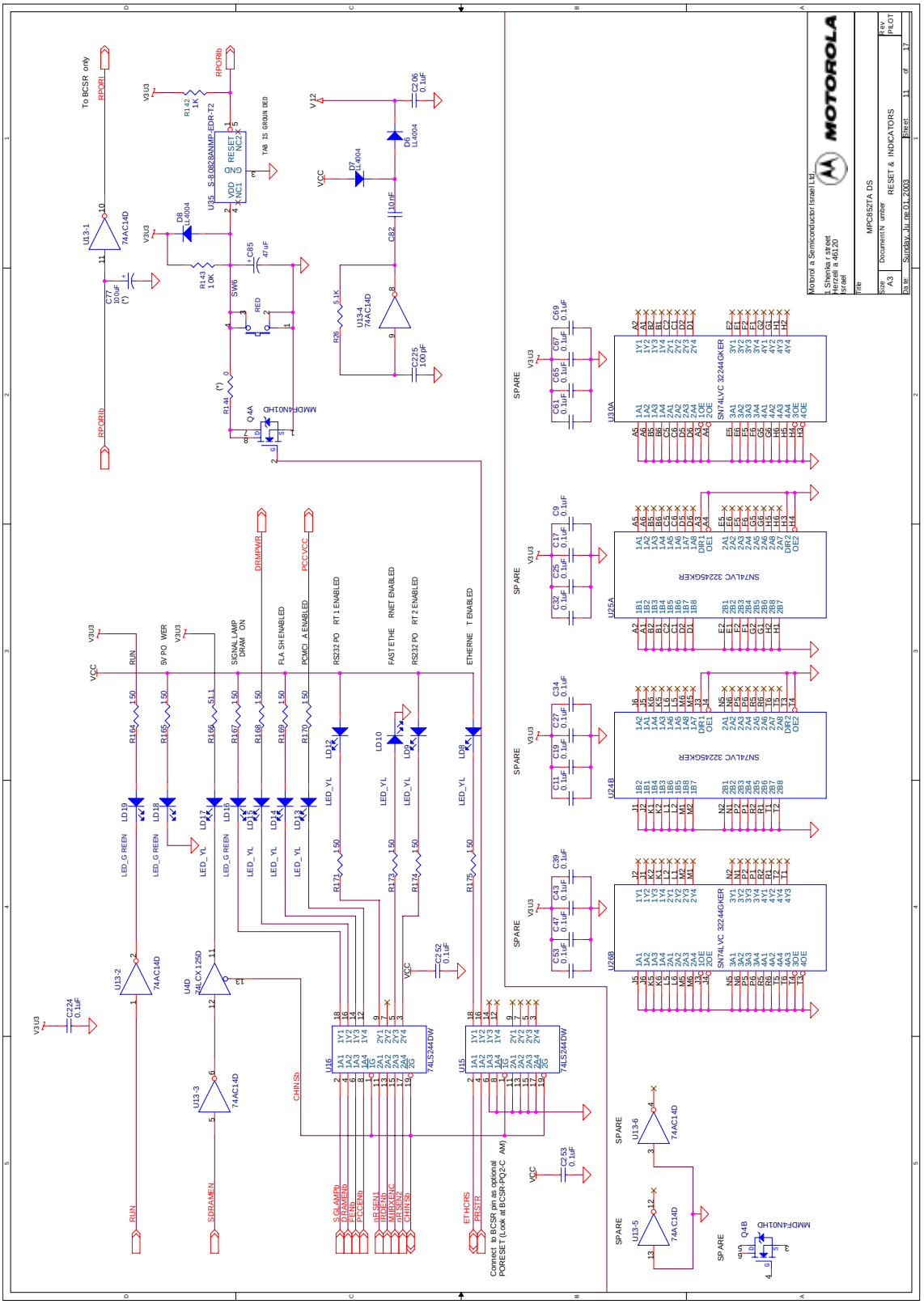

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FIGURE A-12 BCSR

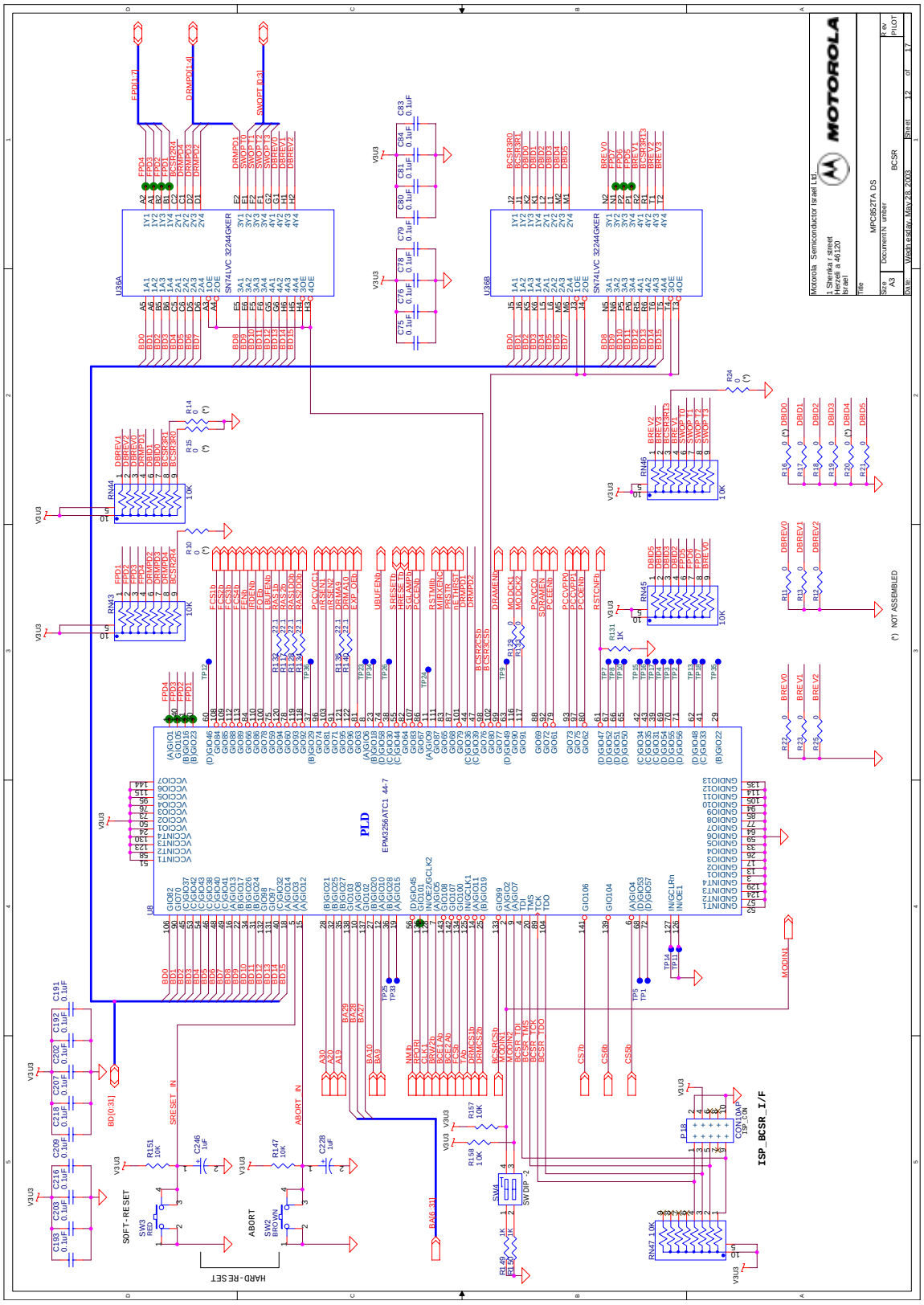

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FIGURE A-13 RS232 & CLOCK

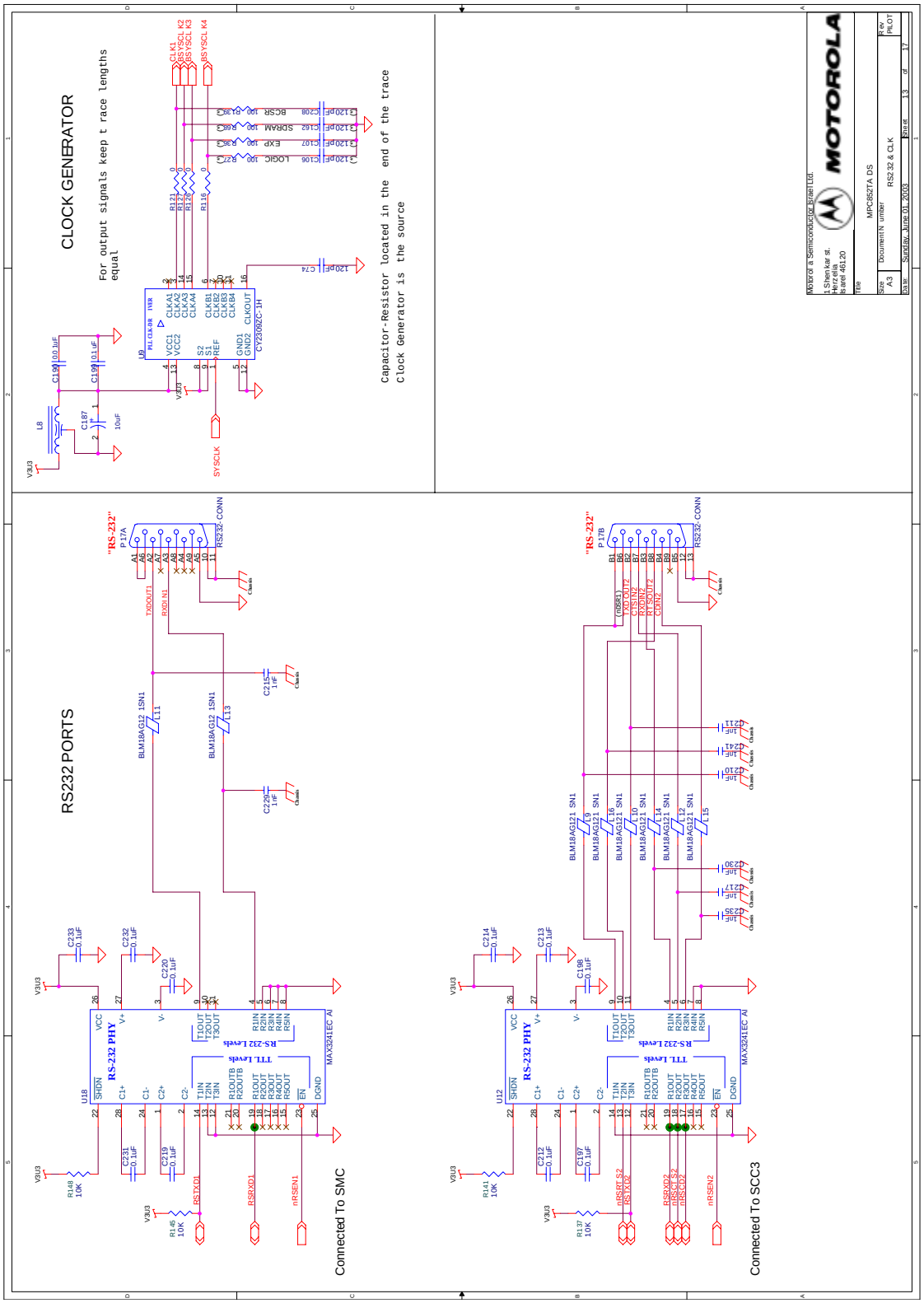

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FIGURE A-14 LOGIC ANALYZER

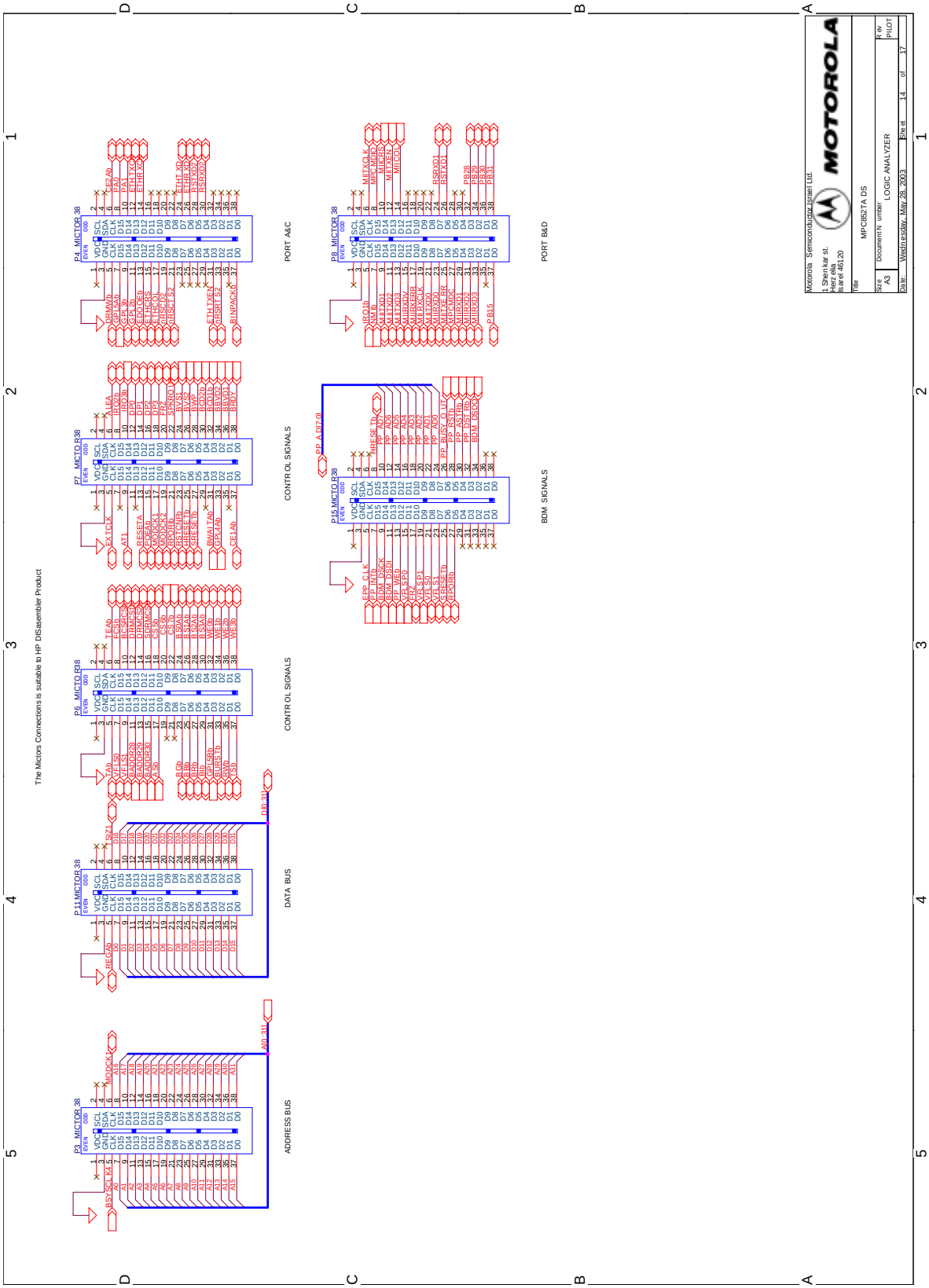

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FIGURE A-15 EXPANSION CONNECTROS

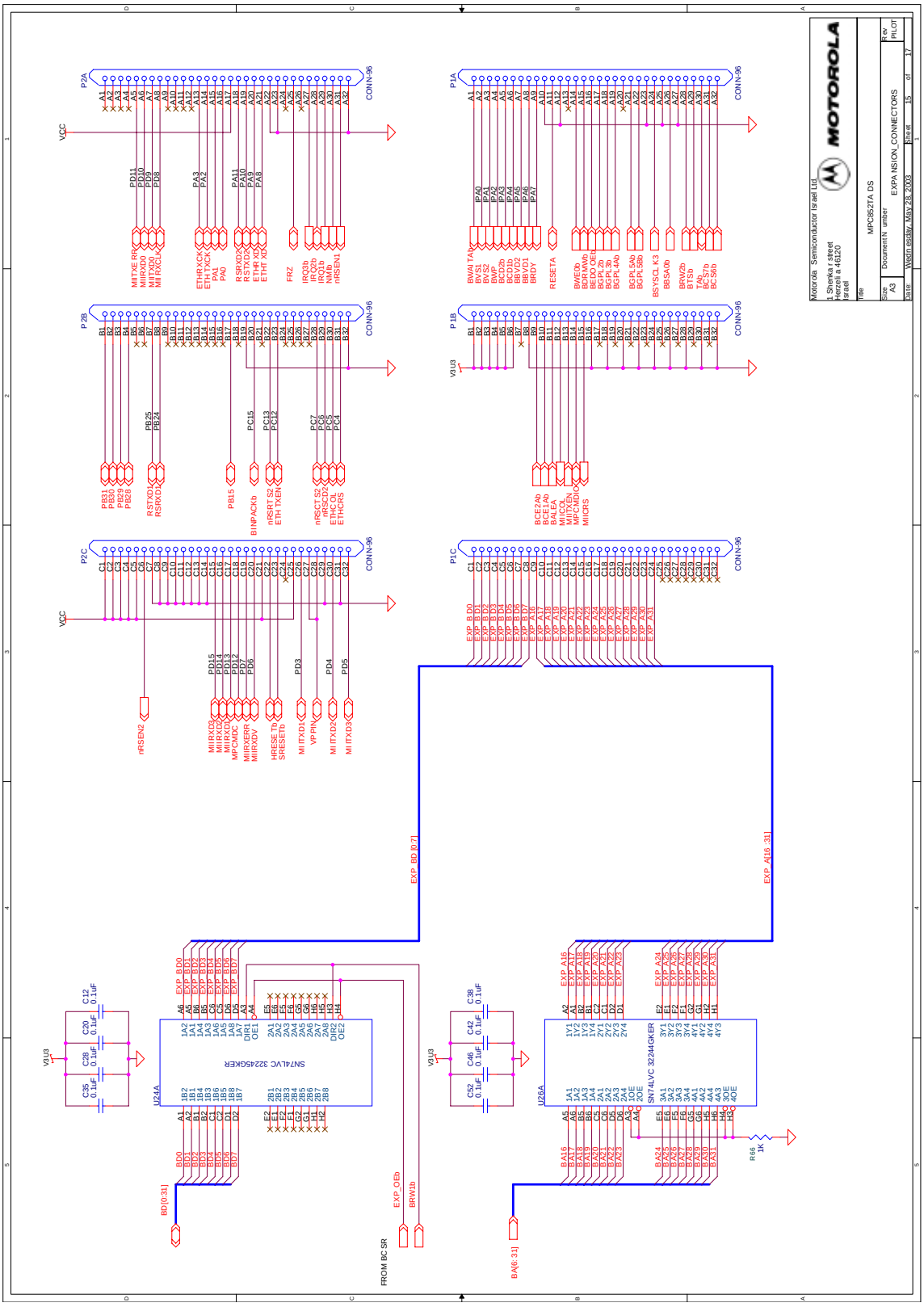

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FIGURE A-16 HOST I/F

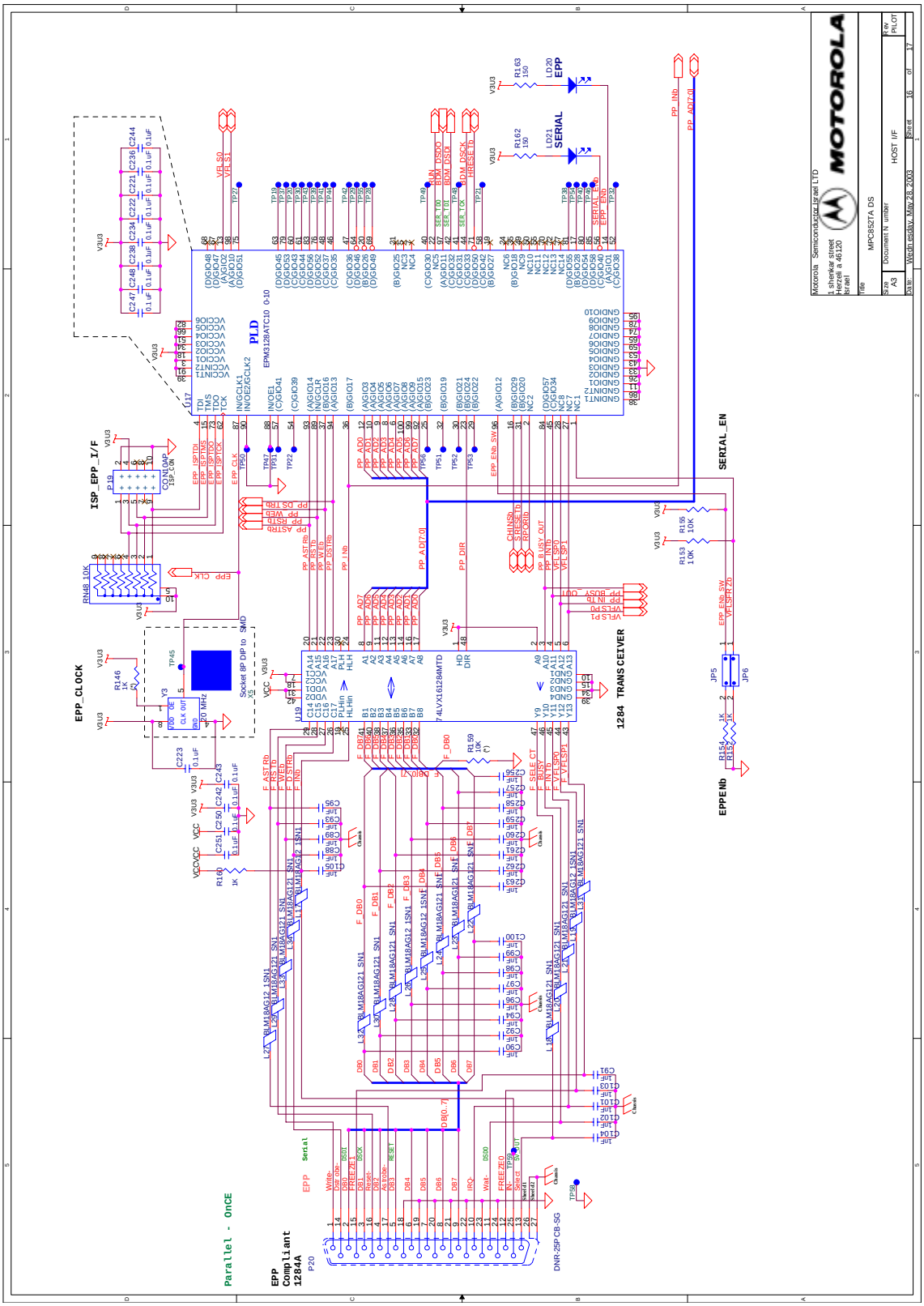

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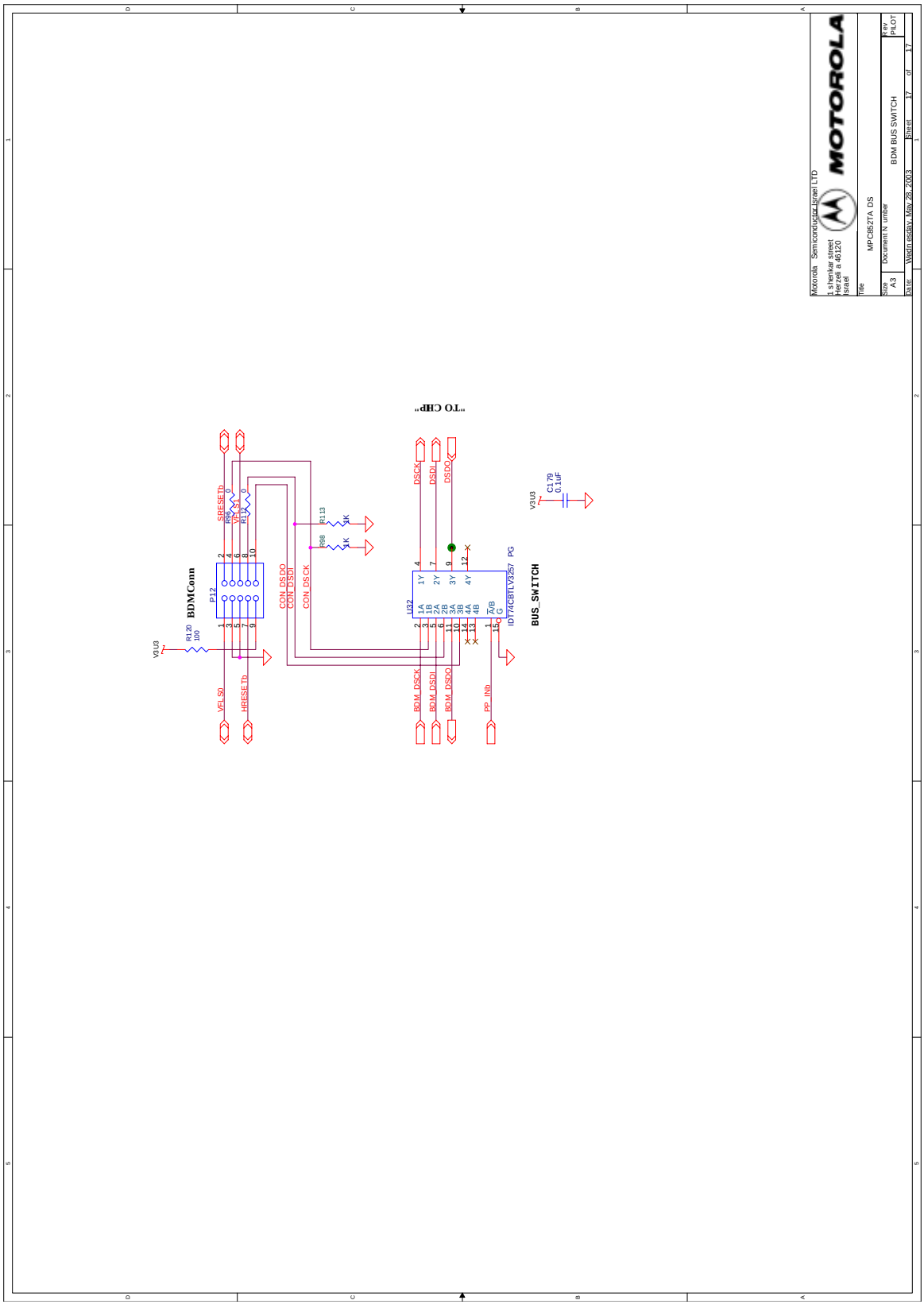
FIGURE A-17 BDM BUS SWITCH



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