International
IOR Rectifier

Feb 21, 2011

IR1153S

FIXED 22.2kHz FREQUENCY, µPFC ONE CYCLE CONTROL IC WITH BROWN-OUT PROTECTION

Features

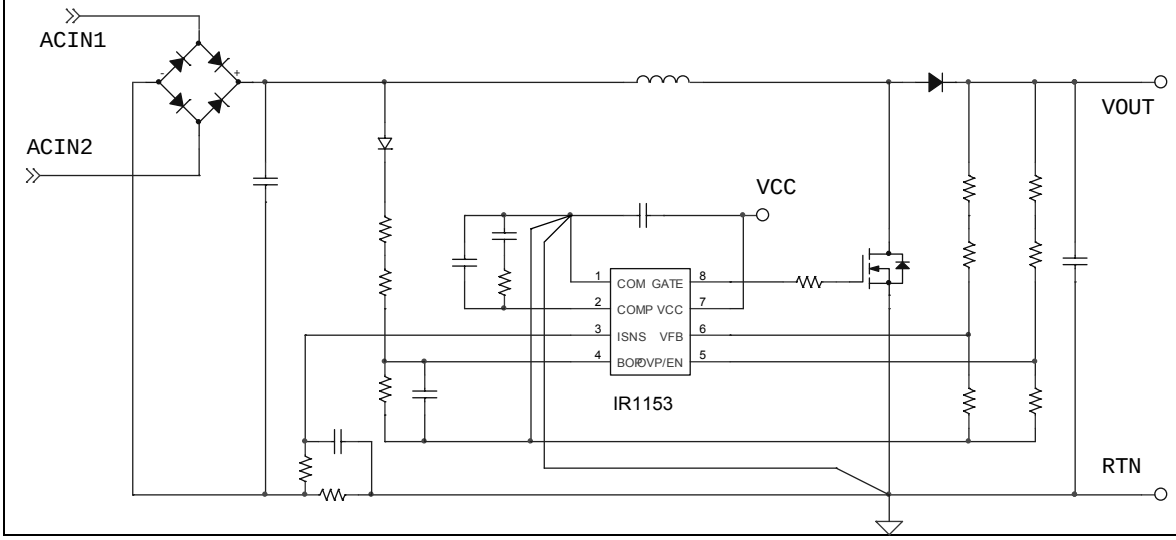
- PFC IC with IR proprietary “One Cycle Control”
- Continuous conduction mode boost type PFC
- Fixed 22.2kHz switching frequency
- Average current mode control
- Input line sensed brownout protection
- Output overvoltage protection
- Open loop protection
- Cycle by cycle peak current limit
- VCC under voltage lockout
- Programmable soft start
- Micropower startup
- User initiated micropower “Sleep Mode”
- 750mA peak gate drive
- Latch immunity and ESD protection

Description

The µPFC IR1153 power factor correction IC, based on IR proprietary "One Cycle Control" (OCC) technique, provides for high PF, low THD and excellent DC Bus regulation while enabling drastic reduction in component count, PCB area and design time as compared to traditional solutions. The IC is designed to operate in continuous conduction mode Boost PFC converters with average current mode control at a fixed 22.2kHz switching frequency. The IR1153 features include input-line sensed brown-out protection, dedicated pin for over voltage protection, cycle by cycle peak current limit, open loop protection, VCC UVLO, soft-start and micropower startup current of less than 75µA. In addition, for standby power requirements, the IC can be driven into a micropower sleep mode by pulling the OVP/EN pin low where the current consumption is less than 75uA. IR1153 is available in SO-8 package.

Package

IR1153 Application Diagram



Qualification Information

Qualification Level		Industrial Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard JESD22-A115)
	Human Body Model	Class 1A (per EIA/JEDEC standard EIA/JESD22-A114)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. All voltages are absolute voltages referenced to COM. Thermal resistance and power dissipation are measured under board mounted and still air conditions.

Parameters	Symbol	Min.	Max.	Units	Remarks
V_{CC} Voltage	V_{CC}	-0.3	20	V	Not internally clamped
ISNS voltage	V_{ISNS}	-10	0.3	V	
ISNS Current	I_{ISNS}	-2	2	mA	
V_{FB} voltage	V_{FB}	-0.3	6.5	V	
V_{OVP} voltage	V_{OVP}	-0.3	6.5	V	
V_{BOP} voltage	V_{BOP}	-0.3	9	V	
COMP voltage	V_{COMP}	-0.3	6.5	V	
Gate Voltage	V_{GATE}	-0.3	18	V	
Junction Temperature Operating Range	T_J	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance	$R_{\theta JA}$		128	°C/W	SOIC-8
Package Power Dissipation	P_D		976	mW	T_{AMB}=25°C SOIC-8

Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25° C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} =15V is assumed for test condition.

Supply Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Supply Voltage Operating Range	V_{CC}		14	17	V	
V_{CC} Turn On Threshold	$V_{CC\ ON}$	12.2	13.1	14	V	
V_{CC} Turn Off Threshold (Under Voltage Lock Out)	$V_{CC\ UVLO}$	9.4	10.1	10.8	V	
V_{CC} Turn On/Off Hysteresis	$V_{CC\ HYST}$	2.4	3	3.6	V	
Operating Current	I_{CC}			7	mA	C_{LOAD} =1nF
				8	mA	C_{LOAD} =4.7nF
			3.5	5	mA	OVP Mode, Inactive gate
Start-up Current	$I_{CC\ START}$		26	75	µA	V_{CC}=$V_{CC\ ON}$ - 0.2V
Sleep current	I_{SLEEP}		26	75	µA	Pin OVP/EN=V_{SLEEP}-0.2V
Sleep Mode Threshold	V_{SLEEP}	0.5		0.8	V	Bias on OVP/EN pin

Oscillator Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Fixed Oscillator Frequency	f_{SW}	20.2	22.2	24.2	kHz	T_{AMB}=25°C
		18.3		25		-25°C < T_{AMB} < 125°C
Maximum Duty Cycle	D_{MAX}	93		99	%	V_{COMP}=5V
Minimum Duty Cycle	D_{MIN}			0	%	Pulse Skipping

Protection Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Open Loop Protection (OLP)Threshold	V_{OLP}	17	19	21	% V_{REF}	Bias on VFB pin
Output Overvoltage Protection (OVP) Threshold	V_{OVP}	104	106	108	% V_{REF}	Bias on OVP/EN pin
Output Overvoltage Protection Reset Threshold	$V_{OVP(RST)}$	101	103	105	% V_{REF}	Bias on OVP/EN pin
OVP Input Bias Current	$I_{OVP(Bias)}$			-0.2	µA	
Brown-out Protection (BOP) Threshold	V_{BOP}	0.66	0.76	0.86	V	Bias on BOP pin
Brown-out Protection Enable Threshold	$V_{BOP(EN)}$	1.46	1.56	1.66	V	Bias on BOP pin
BOP Input Bias Current	$I_{BOP(Bias)}$			-0.2	µA	
Peak Current Limit Protection ISNS Voltage Threshold (IPK LIMIT)	$V_{ISNS(PK)}$	-0.58	-0.51	-0.44	V	Bias on ISNS pin

Internal Voltage Reference Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Reference Voltage	V_{REF}	4.9	5	5.1	V	Regulation Voltage on VFB pin, T_{AMB}=25°C
Line Regulation	R_{REG}		10	20	mV	14V < V_{CC} < 17V
Temp Stability	T_{STAB}		0.4		%	-25°C < T_{AMB} < 125°C, Note 1
Total Variation	ΔV_{TOT}	4.83		5.12	V	Line & Temperature

Voltage Error Amplifier Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Transconductance	g_m	35	49	59	µS	
Source Current (Normal Mode)	$I_{OVEA(SRC)}$	30	44	58	µA	T_{AMB}=25°C
		17		80		-25°C < T_{AMB} < 125°C
Sink Current (Normal Mode)	$I_{OVEA(SNK)}$	-58	-44	-30	µA	T_{AMB}=25°C
		-80		-17		-25°C < T_{AMB} < 125°C
Soft Start Delay Time (calculated)	t_{SS}		35		msec	R_{GAIN}=8kΩ, C_{ZERO}=0.33µF, C_{POLE}=2nF
V_{COMP} Voltage (Fault)	$V_{COMP\ FLT}$		1	1.5	V	@100uA steady state
Effective V_{COMP} voltage	$V_{COMP\ EFF}$	4.7	4.9	5.1	V	
VFB Input Bias Current	$I_{FB(Bias)}$			-0.2	µA	
Output Low Voltage	V_{OL}			0.25	V	
Output High Voltage	V_{OH}	5		5.45	V	
V_{COMP} Start Voltage	$V_{COMP\ START}$	210	325	435	mV	

Current Amplifier Section

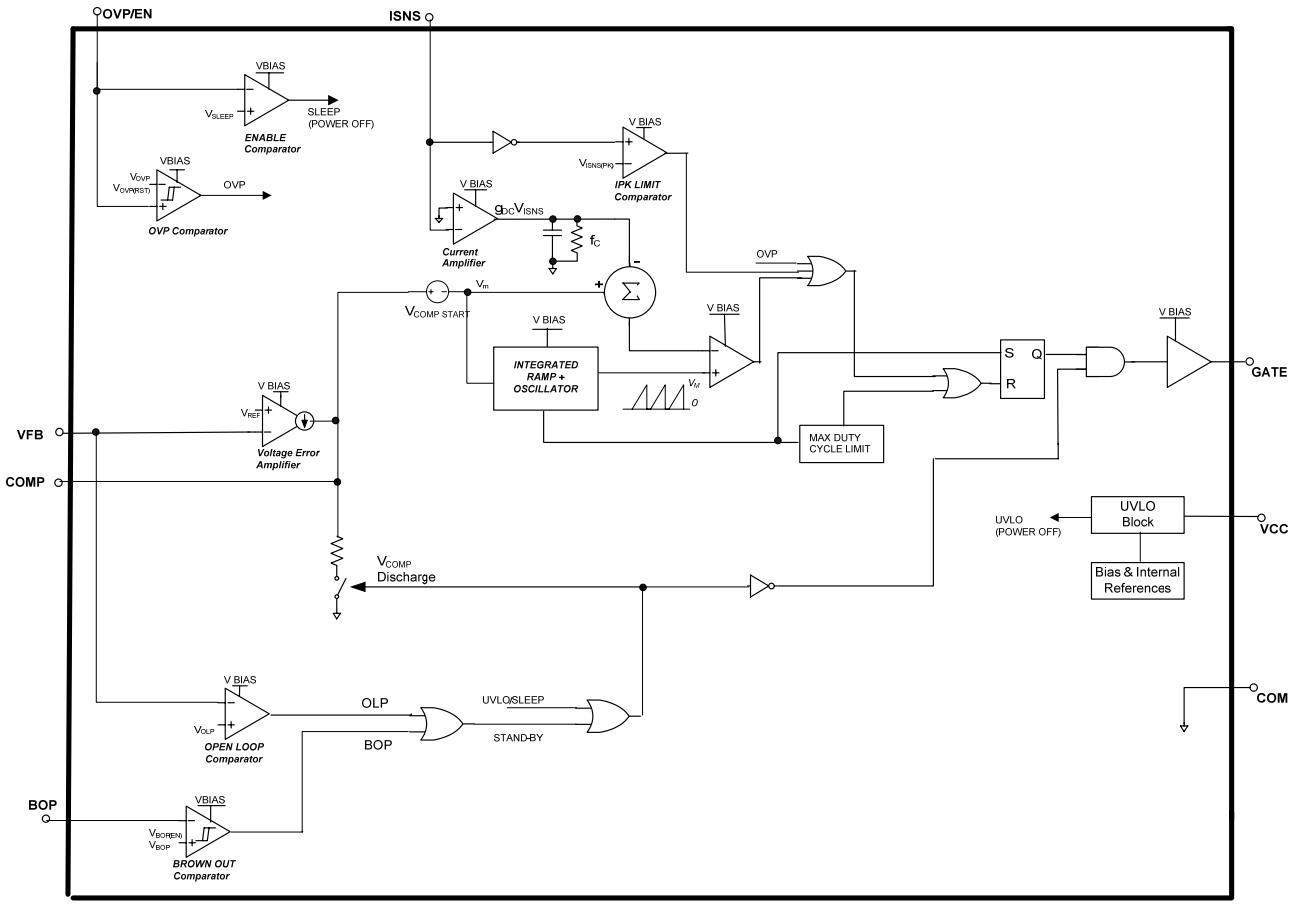
Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
DC Gain	g_{DC}		5.65		V/V	
Corner Frequency	f_C		2		kHz	Average Current Mode, Note 1
Input Offset Voltage	V_{IO}		4	16	mV	Note 1
ISNS Input Bias Current	$I_{ISNS(Bias)}$	-57		-13	µA	
Blanking Time	T_{BLANK}	170	320	470	ns	

Gate Driver Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Gate Low Voltage	V_{GLO}			0.8	V	I_{GATE} = 200mA
Gate High Voltage	V_{GTH}	13.1	14.1	15.1	V	V_{CC}=17V, Internally Clamped
		9.5				V_{CC}=11.5V
Rise Time	t_r		25		ns	C_{LOAD} = 1nF, VCC=15V
			60		ns	C_{LOAD} = 4.7nF, VCC=15V
Fall Time	t_f		35		ns	C_{LOAD} = 1nF, VCC=15V
			65		ns	C_{LOAD} = 4.7nF, VCC=15V
Output Peak Current	I_{OPK}	750			mA	C_{LOAD} = 4.7nF, VCC=15V, Note 1
Gate Voltage at Fault	$V_{G\ fault}$			0.08	V	I_{GATE} = 20mA

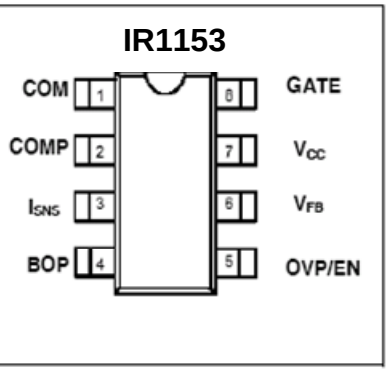
Note 1: Guaranteed by design, but not tested in production

Block Diagram



Lead Assignments & Definitions

PIN	SYMBOL	DESCRIPTION
1	COM	Ground
2	COMP	Voltage Loop Compensation
3	ISNS	Current sense
4	BOP	Brown-out Fault Detect
5	OVP/EN	Overvoltage Fault Detect/Enable
6	VFB	Output Voltage Sense
7	VCC	IC Supply voltage
8	GATE	Gate Drive Output



IR1153 General Description

The µPFC IR1153 IC is intended for power factor correction in continuous conduction mode Boost PFC converters operating at fixed switching frequency with average current mode control. The IC operates based on IR's proprietary "One Cycle Control" (OCC) PFC algorithm based on the concept of resettable integrator.

Theory of Operation

The OCC algorithm based on the resettable integrator concept works using two loops - a slow outer voltage loop and a fast inner current loop. The outer voltage loop monitors the VFB pin and generates an error signal which controls the amplitude of the input current admitted into the PFC converter. In this way, the outer voltage loop maintains output voltage regulation. The voltage loop bandwidth is kept low enough to not track the $2xf_{AC}$ ripple in the output voltage and thus generates an almost DC error signal under steady state conditions.

The inner current loop maintains the sinusoidal profile of the input current and thus is responsible for power factor correction. The information about the sinusoidal variation in input voltage is inherently available in the input line current (or boost inductor current). Thus there is no need to sense the input voltage to generate a current reference. The current loop employs the boost inductor current information to generate PWM signals with a proportional sinusoidal variation. This controls the shape of the input current to be proportional to and in phase with the input voltage. Average current mode operation is envisaged by filtering the switching frequency ripple from the current sense signal using an appropriately sized on-chip RC filter. This filter also contributes to the bandwidth of the current control loop. Thus the filter bandwidth has to be high enough to track the 120Hz rectified, sinusoidal current waveform and also filter out the switching frequency ripple in the inductor current. In IR1153 this averaging function can effectively filter high ripple current ratios (as high as 40% at maximum input current) to accommodate designs with small boost inductances.

The IC determines the boost converter instantaneous duty cycle based on the resettable integrator concept. The required signals are the voltage feedback loop error signal V_m (which is the V_{COMP} pin voltage minus a DC offset of $V_{COMP,START}$) and the current sense signal V_{ISNS}. The resettable integrator generates a cycle-by-cycle, saw-tooth signal called the PWM Ramp which has an amplitude V_m and period $1/f_{SW}$ hence a slope of V_m*f_{SW}.

The current sense signal is amplified by the current amplifier by a factor g_{DC} and fed into the summing node where it is subtracted from V_m to generate the summer voltage (= $V_m–g_{DC}*V_{ISNS}$). The summer voltage is compared with the PWM ramp by the PWM comparator of the IC to determine the gate drive duty cycle. The instantaneous duty is mathematically given by:

$D = (V_m - g_{DC}.V_{ISNS})/V_m$

Assuming steady state condition where the voltage feedback loop is well regulated (V_m & V_{OUT} are DC signals) & hence instantaneous duty cycle follows the boost-converter equation ($D = 1 – V_{IN}(t)/V_{OUT}$), the control equation can be re-written as:

$V_m = g_{DC}.V_{ISNS}/(V_{IN}(t)/V_{OUT})$

Further, recognizing that $V_{ISNS} = I_L(t).R_{SNS}$ and re-arranging yields:

$g_{DC}.I_L(t).R_{SNS} = V_mV_{IN}(t)/V_{OUT}$

Since V_m, V_{OUT} & g_{DC} are constant terms:

$I_L(t) \alpha V_{IN}(t)$

Thus the inductor current follows the input voltage waveform & by definition power factor correction is achieved.

Feature set

Fixed Frequency Operation

The IC is programmed to operate at a fixed frequency of 22.2kHz (Typ). Internalization of the oscillator offers excellent noise immunity even in the noisy PFC environment while integration of the oscillator into the OCC core of the IC eliminates need for digital calibration circuits. Both these factors render the gate drive jitter free thus contributing to elimination of audible noise in PFC magnetics.

IC Supply Circuit & Low start-up current

The IR1153 UVLO circuit maintains the IC in UVLO mode during start-up if VCC pin voltage is less than the VCC turn-on threshold, $V_{CC,ON}$ and current consumption is less than 75uA. Should VCC pin voltage should drop below $V_{CC,UVLO}$ during normal operation, the IC is pushed back into UVLO mode and VCC pin has to exceed $V_{CC,ON}$ again for normal operation. There is no internal voltage clamping of the VCC pin.

User initiated Micropower Sleep mode

The IC can be actively pushed into a micropower Sleep Mode where current consumption is less than 75uA by pulling OVP/EN pin below the Sleep threshold, V_{SLEEP} even while VCC is above $V_{CC,ON}$. This allows the user to disable PFC during application stand-by situations in order to meet stand-by regulations. Since V_{SLEEP} is less than 1V, even logic level signals can be employed.

IR1153 General Description

Programmable Soft Start
The soft start process controls the rate of rise of the voltage feedback loop error signal thus providing a linear increase of the RMS input current that the PFC converter will admit. The soft start time is essentially controlled by voltage error amplifier compensation components selected and is therefore user programmable to some degree based on desired voltage feedback loop crossover frequency.

Gate Drive Capability
The gate drive output stage of the IC is a totem pole driver with 750mA peak current drive capability. The gate drive is internally clamped at 14.1V (Typ). Gate drive buffer circuits (especially cost-effective base-followers) can be easily driven with the GATE pin of the IC to suit any system power level.

System Protection Features
IR1153 protection features include Brown-out protection (BOP), Open-loop protection (OLP), Overvoltage protection (OVP), Cycle-by-cycle peak current limit (IPK LIMIT), Soft-current limit and VCC under voltage lock-out (UVLO).

- BOP is based on direct input line sensing using a resistor divider/RC filter network. If BOP pin falls below the Brown-out protection threshold V_{BOP}, a Brown-out situation is immediately detected the following response is executed - the gate drive pulse is disabled, VCOMP is actively discharged and IC is pushed into Stand-by Mode. The IC re-enters normal operation only after BOP pin exceeds $V_{BOP(EN)}$. During start-up the IC is held in Stand-by Mode until this pin exceeds $V_{BOP(EN)}$.

- OLP is activated whenever the VFB pin voltage falls below V_{OLP} threshold. Once open loop is detected the following response is immediately executed - the gate drive is immediately disabled, VCOMP is actively discharged and the IC is pushed into Stand-by mode. There is no voltage hysteresis associated with this feature. During start-up the IC is held in Stand-by Mode until VFB exceeds V_{OLP}.

- The OVP pin is a dedicated pin for overvoltage protection that safeguards the system even if there is a break in the VFB feedback loop due to resistor divider failure etc. An overvoltage fault is triggered when OVP pin voltage exceeds the V_{OVP} threshold of 106%VREF. The response of the IC is to immediately terminate the gate drive output and hold it in that state. The gate drive is re-enabled only after OVP pin voltage drops below $V_{OVP(RST)}$ threshold of 103% VREF. The exact voltage level at which overvoltage protection is triggered can be programmed by the user by carefully designing the OVP pin resistor divider. It is recommended NOT to set the OVP voltage trigger limit less than 106% of DC bus voltage, since this can endanger the situation where the OVP reset limit will be less than the DC bus voltage regulation point – in this condition the voltage loop can become unstable.

- Soft-current limit is an output voltage fold-back type protection feature encountered when the PFC converter input current exceeds to a point where the V_m voltage saturates. As mentioned earlier, the amplitude of input current is directly proportional to V_m, the error voltage of the feedback loop. V_m is clamped to a certain maximum voltage inside the IC (given by $V_{COMP,EFF}$ parameter in datasheet). If the input current causes the V_m voltage to saturate at its maximum value, then any further increase in input current will cause the duty cycle to droop which immediately forces the V_{OUT} voltage of the PFC converter to fold-back. Since the highest current is at the peak of the AC sinusoid, the droop in duty cycle commences at the peak of the AC sinusoid when the soft-current limit is encountered. In most converters, the design of the current sense resistor is performed based on soft-current limit (i.e. V_m saturation) and at the system condition which demands highest input current (minimum V_{AC} & maximum P_{OUT}).

- Cycle-by-cycle peak current limit protection instantaneously turns-off the gate output whenever the ISNS pin voltage exceeds $V_{ISNS(PK)}$ threshold in magnitude. The gate drive is held in the low state as long as the overcurrent condition persists. The gate drive is re-enabled when the magnitude of ISNS pin voltage falls below the $V_{ISNS(PK)}$ threshold. This protection feature incorporates a leading edge blanking circuit to improve noise immunity.

IR1153 Pin Description

Pin COM: This is ground potential pin of the IC. All internal devices are referenced to this point.

Pin COMP: External circuitry from this pin to ground compensates the system voltage loop and programs the soft start time. The COMP pin is essentially the output of the voltage error amplifier. The voltage loop error signal V_m used in the control algorithm is derived from V_{COMP} ($V_m = V_{COMP} - V_{COMP,START}$). V_{COMP} is actively discharged using an internal resistance to below $V_{COMP,START}$ threshold whenever the IC is pushed into Stand-by mode (BOP or OLP condition) or UVLO/Sleep mode. The gate drive output and logic functions of the IC are inactive if VCOMP is less than $V_{COMP,START}$. Also during start-up, the VCOMP voltage has to be less than $V_{COMP,START}$ in order to commence operation (i.e. a pre-bias on VCOMP will not allow IC to commence operation).

Pin ISNS: ISNS pin is tied to the input of the current sense amplifier of the IC. The voltage at this pin, which provides the current sense information to the IC, has to be a negative voltage wrt the COM pin. Also since the IC is based on average current mode, the entire inductor current information is necessary. A current sense resistor, located below system ground along the return path to the bridge rectifier, is the preferred current sensing method. ISNS pin is also the inverting input to the cycle-by-cycle peak current limit comparator. Whenever V_{ISNS} exceeds $V_{ISNS(PK)}$ threshold in magnitude, the gate drive is instantaneously disabled. Any external filtering of the ISNS pin must be performed carefully in order to ensure that the integrity of the current sense signal is maintained for cycle-by-cycle peak current limit protection.

Pin BOP (Brown-out Protection): This pin is used to sense the rectified AC input line voltage through a resistor divider/capacitor network which is in effect a voltage division and averaging network, representing a scaled down signal of the average rectified input voltage (average DC voltage + $2xf_{AC}$ ripple). During start-up the BOP pin voltage has to exceed $V_{BOP(EN)}$ in order to enable the IC to exit Stand-by mode and enter normal operation. A Brown-out situation is detected whenever the pin voltage falls below V_{BOP} and the IC is pushed into Stand-by mode. Subsequently the pin has to exceed $V_{BOP(EN)}$ for the IC to exit Stand-by and resume normal operation.

Pin OVP/EN: The OVP/EN pin is connected to the non-inverting input of the OVP(OVP) overvoltage comparator shown in the block diagram and thus is used to detect output overvoltage situations. The output voltage information is communicated to the OVP pin using a resistive divider. This pin also serves the second purpose of an ENABLE pin. The OVP/EN pin can be used to activate the IC into "micropower sleep" mode by pulling the voltage on this pin below the V_{SLEEP} threshold.

Pin VFB: The converter output voltage is sensed via a resistive divider and fed into this pin. VFB pin is the inverting input of the output voltage error amplifier. The non-inverting input of this amplifier is connected to an internal 5V reference. The impedance of the divider string must be low enough that it does not introduce substantial error due to the input bias currents of the amplifier, yet high enough to minimize power dissipation. Typical value of external divider total impedance will be around 2MΩ. VFB pin is also the inverting input to the Open Loop comparator. The IC is held in Stand-by Mode whenever VFB pin voltage is below V_{OLP} threshold.

Pin VCC: This is the supply voltage pin of the IC and sense node for the undervoltage lock out circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, $V_{CC(UVLO)}$ without damage to the IC. This pin is not internally clamped.

Pin GATE: This is the gate drive output of the IC. It provides a drive current of ±0.75A peak with matched rise and fall times. The gate drive output of the IC is clamped at 14.1V(Typ).

IR1153 Modes of operation

Referenced to States & Transition Diagram

UVLO/Sleep Mode: The IC is in the UVLO/Sleep mode when VCC pin voltage is below $V_{CC,ON}$ at start-up or when VCC pin voltage drops below $V_{CC,UVLO}$ during normal operation or when OVP/EN pin voltage is below V_{SLEEP}. The UVLO/Sleep mode is accessible from any other state of operation. This mode can be actively invoked by pulling the OVP/EN pin below V_{SLEEP} even if VCC pin voltage is above $V_{CC,ON}$. In the UVLO/Sleep state, the gate drive circuit is inactive, most of the internal circuitry is unbiased and the IC draws a quiescent current of I_{SLEEP} which is less than 75uA. Also, the internal logic of the IC ensures that whenever the Sleep mode is actively invoked, the COMP pin is actively discharged below $V_{COMP,START}$ threshold prior to entering the sleep mode, in order to facilitate soft-start upon resumption of operation.

Stand-by Mode: The IC is placed in Stand-by mode whenever an Open-loop and/or a Brown-out situation is detected. A Brown-out situation is sensed when BOP pin voltage is less than $V_{BOP(EN)}$ prior to system start-up and when BOP pin voltage drops below V_{BOP} after start-up. An Open-loop situation is sensed anytime VFB pin voltage is less than V_{OLP}. All internal circuitry is biased in the Stand-by Mode, but the gate is inactive and the IC draws a few mA of current. This state is accessible from any other state of operation of the IC. COMP pin is actively discharged to below $V_{COMP,START}$ whenever this state is entered from normal operation in order to facilitate soft-start upon resumption of operation.

Soft Start Mode: During system start-up, the soft-start mode is activated once the VCC voltage has exceeded $V_{CC,ON}$, the VFB pin voltage has exceeded V_{OLP} and BOP pin voltage has exceeded $V_{BOP(EN)}$ and VCOMP voltage is less than $V_{COMP,START}$ i.e. a pre-bias on COMP pin greater than $V_{COMP,START}$ threshold will not allow IC to commence operation. The soft start time is the time required for the VCOMP voltage to charge through its entire dynamic range i.e. through $V_{COMP,EFF}$. As a result, the soft-start time is dependent upon the component values selected for compensation of the voltage loop on the COMP pin. To an extent, keeping in mind the voltage feedback loop considerations, the soft-system start time is programmable.

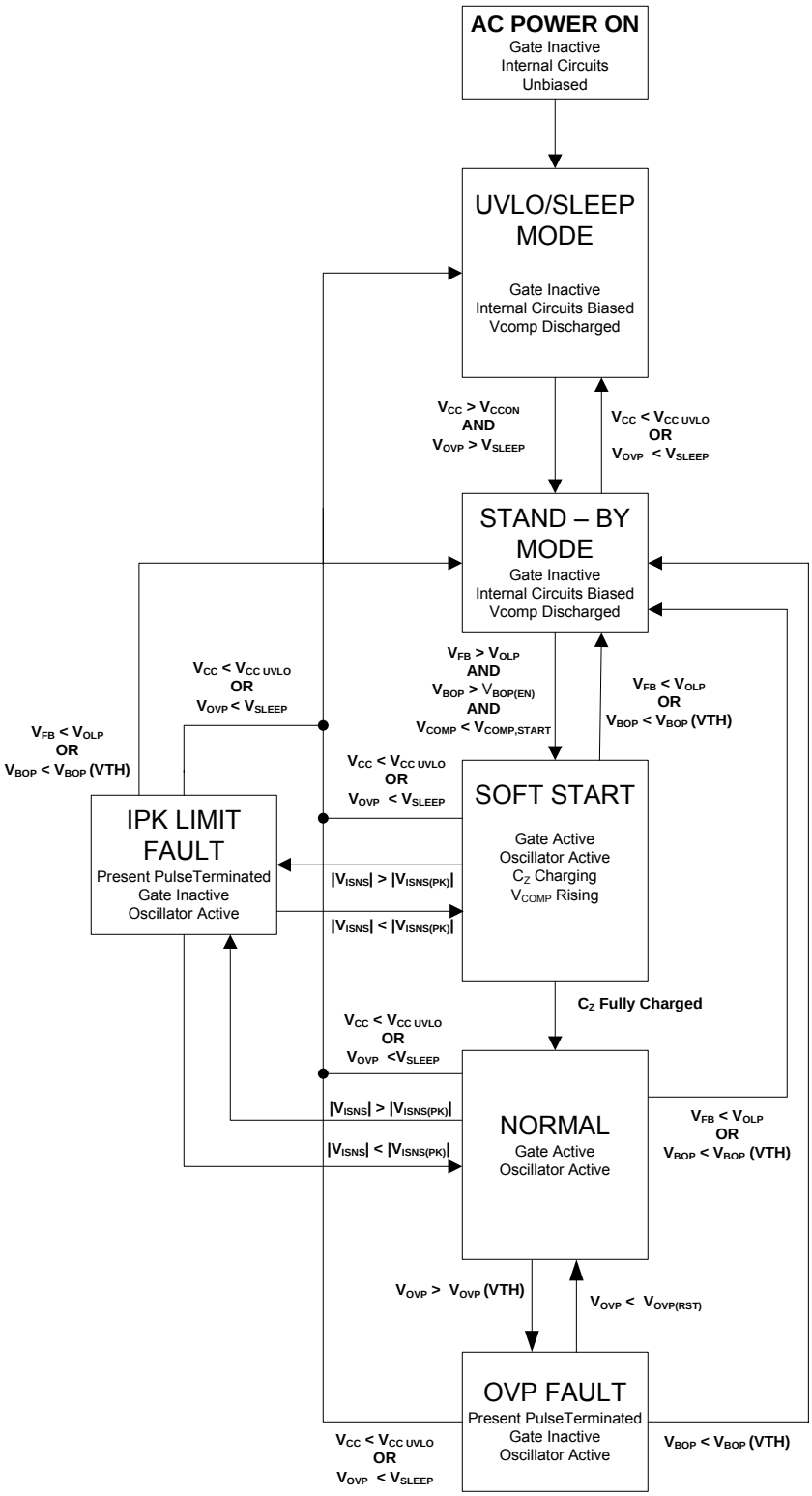
As VCOMP voltage rises gradually, the IC allows a higher and higher RMS current into the PFC converter. This controlled increase of the input current amplitude contributes to reducing system component stress during start-up.

Normal Mode: The IC enters the normal operating mode once the soft start transition has been completed (for all practical purposes there is essentially no difference between the soft-start and normal modes). At this point the gate drive is switching and all protection functions of the IC are active. If, from the normal mode, the IC is pushed into either a Stand-by mode or UVLO/Sleep mode then COMP pin is actively discharged below $V_{COMP,START}$ and system will go through soft-start upon resumption of operation.

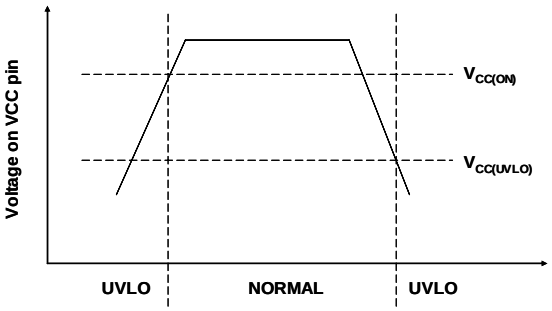
OVP Mode: The IC enters OVP mode whenever an overvoltage condition is detected. A system overvoltage condition is recognized when OVP/EN pin voltage exceeds V_{OVP} threshold. When this happens the IC immediately disables the gate drive and holds it in that state. The gate drive is re-enabled only when OVP/EN pin voltages are less than $V_{OVP(RST)}$ threshold. This state is accessible from both the soft start and normal modes of operation.

IPK LIMIT Mode: The IC enters IPK LIMIT mode whenever the magnitude of ISNS pin voltage exceeds the $V_{ISNS(PK)}$ threshold triggering cycle-by-cycle peak overcurrent protection. When this happens, the IC immediately disables the gate drive and holds it in that state. Gate drive is re-enabled when magnitude of ISNS pin voltage drops below $V_{ISNS(PK)}$ threshold. This state is accessible from both the soft start and normal modes of operation.

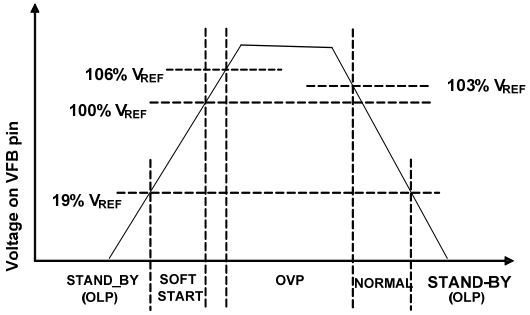
State & Transitions Diagram



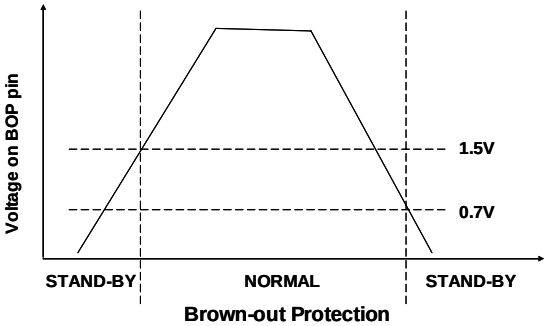
IR1153 Timing Diagrams



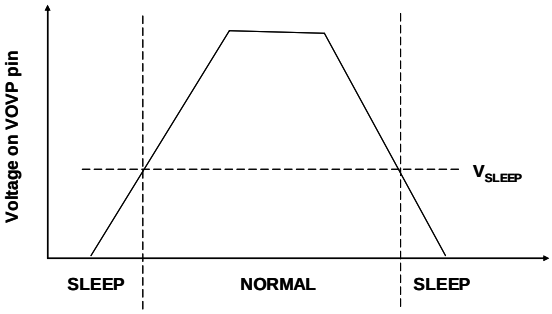
VCC Undervoltage Lockout



Output Protection



Brown-out Protection



Micropower Sleep

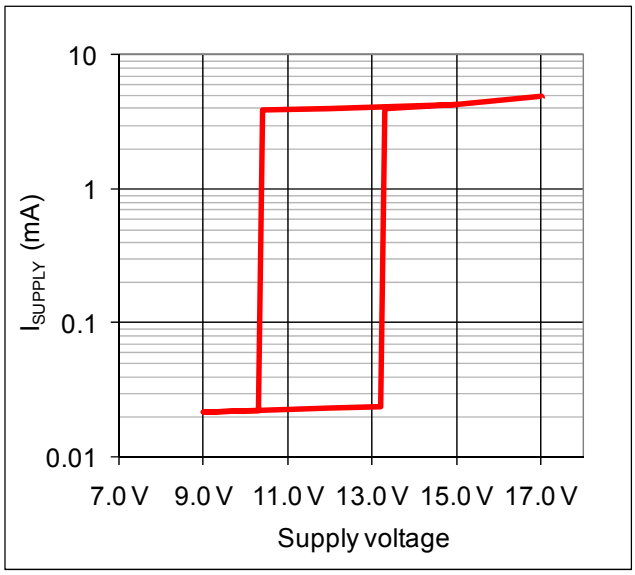


Figure 1: Supply Current vs. Supply Voltage

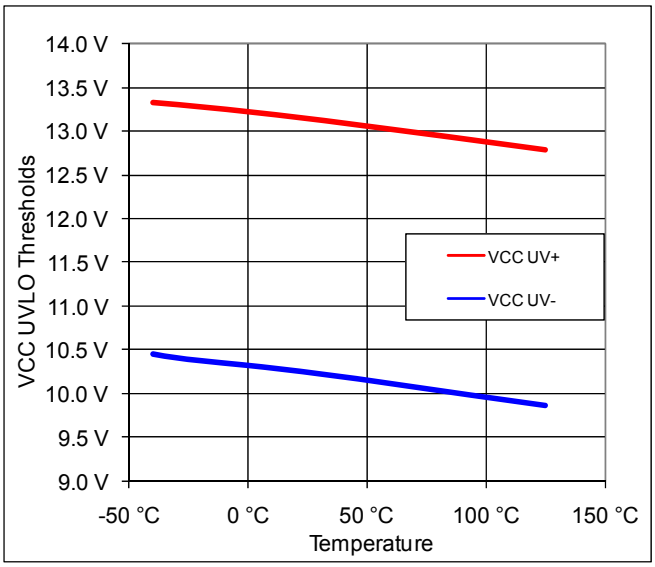


Figure 2: Undervoltage Lockout vs. Temperature

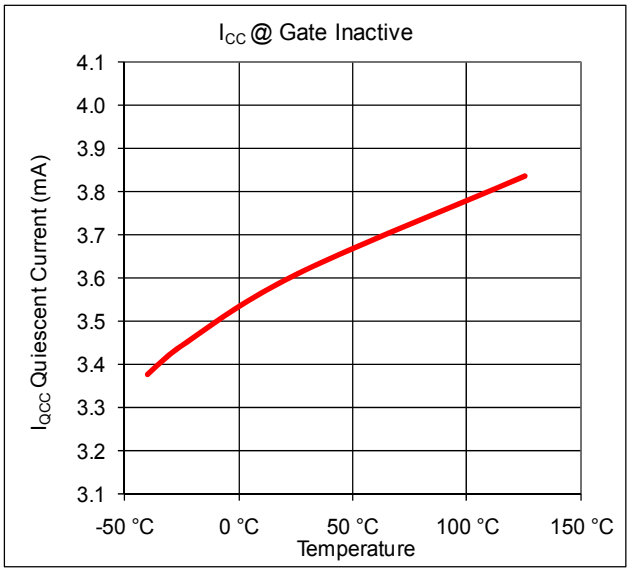


Figure 3: Icc Currrent vs. Temperature

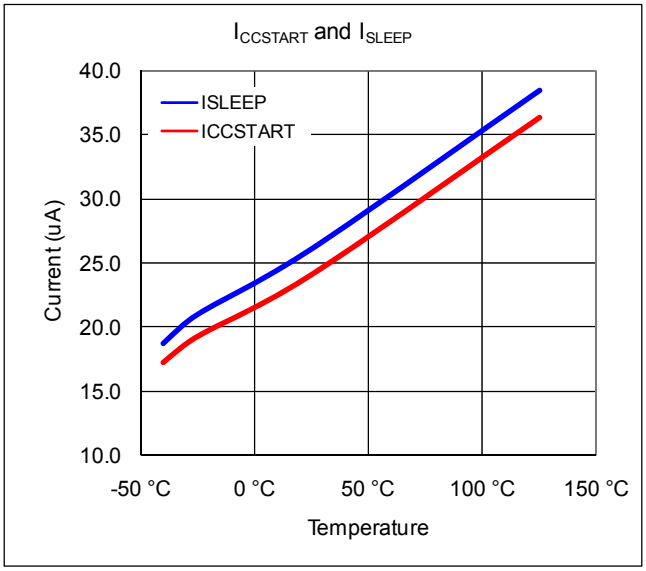


Figure 4: Startup Current and Sleep Current vs. Temperature

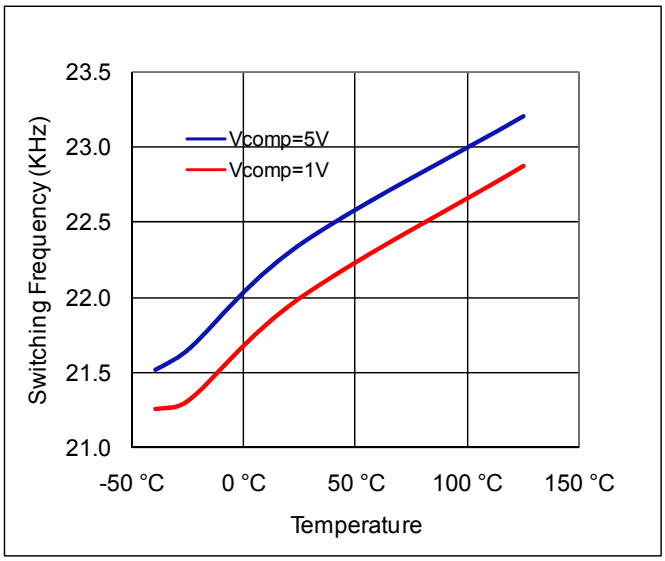


Figure 5: Switching Frequency vs. Temperature

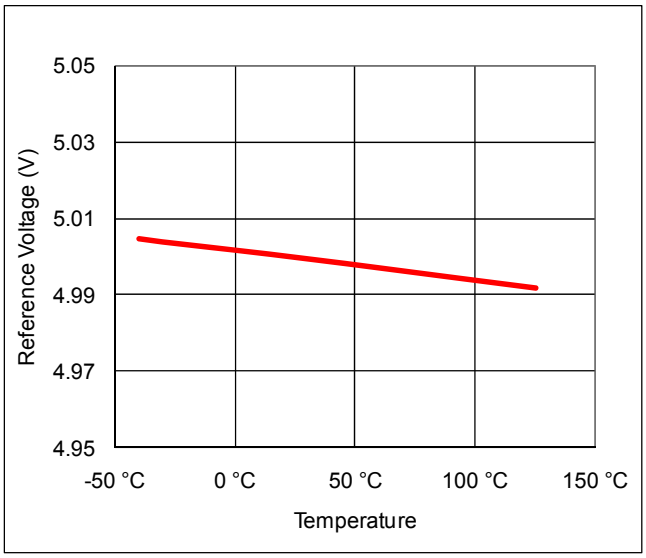


Figure 6: Reference Voltage vs. Temperature

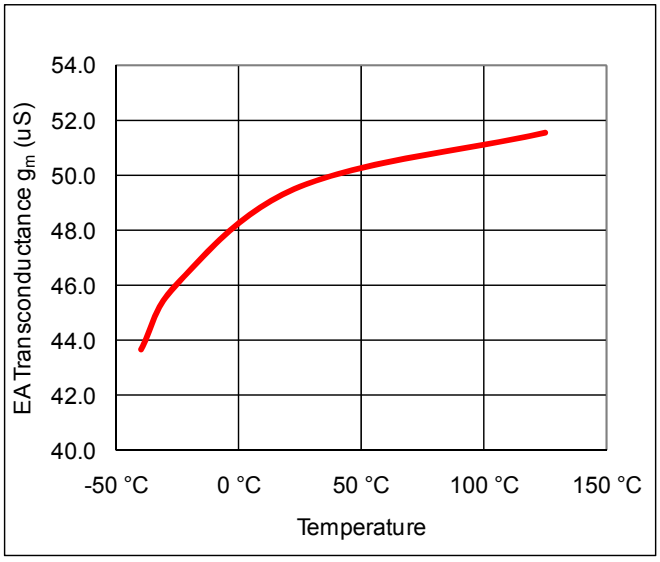


Figure 7: Voltage Error Amplifier Transconductance vs. Temperature

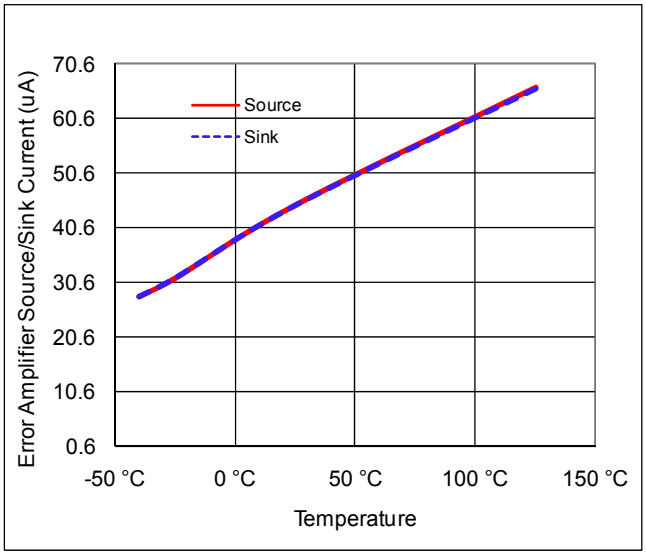


Figure 8: Voltage Error Amplifier Source & Sink Current vs. Temperature

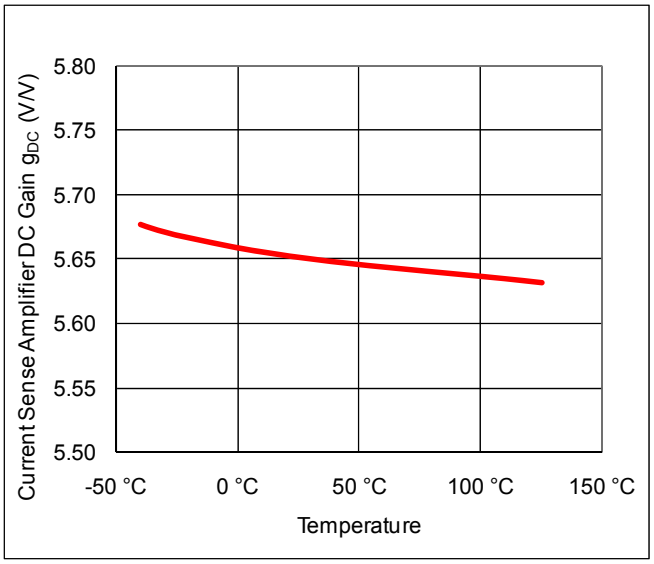


Figure 9: Current Amplifier DC Gain vs. Temperature

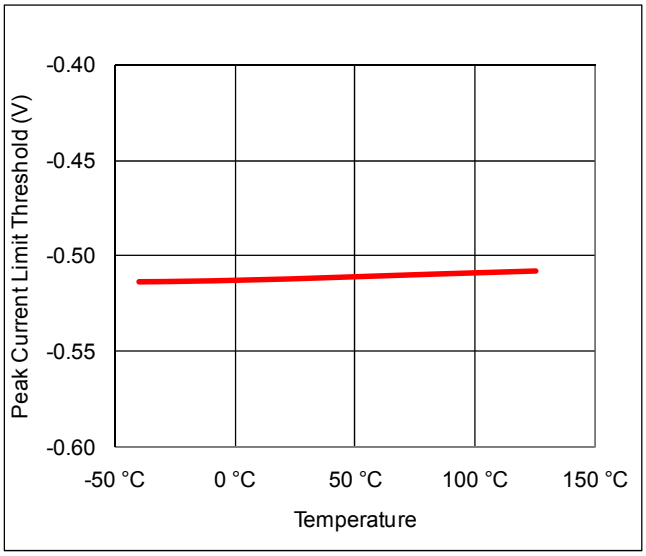


Figure 10: Peak Current Limit Threshold $V_{ISNS(PK)}$ vs. Temperature

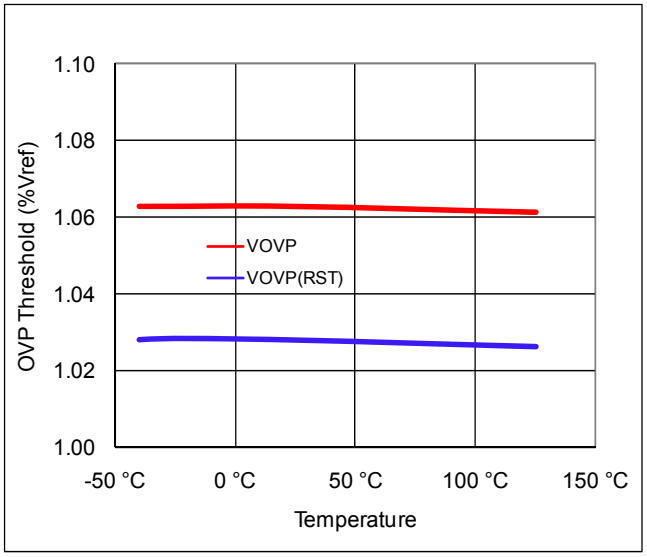


Figure 11: Over Voltage Protection Thresholds vs. Temperature

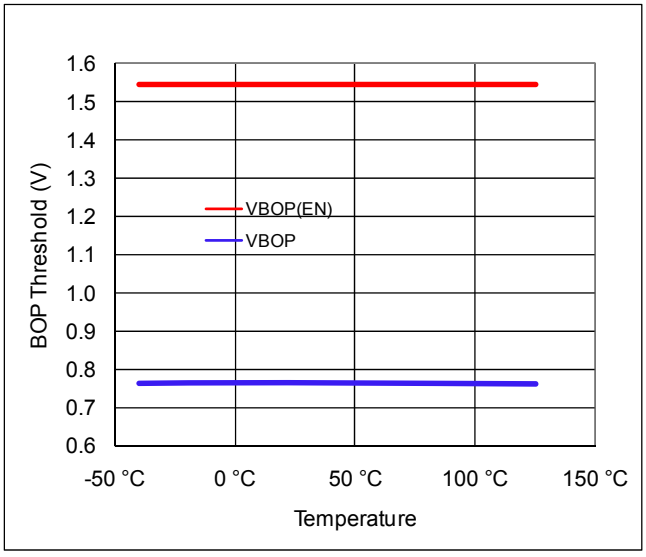
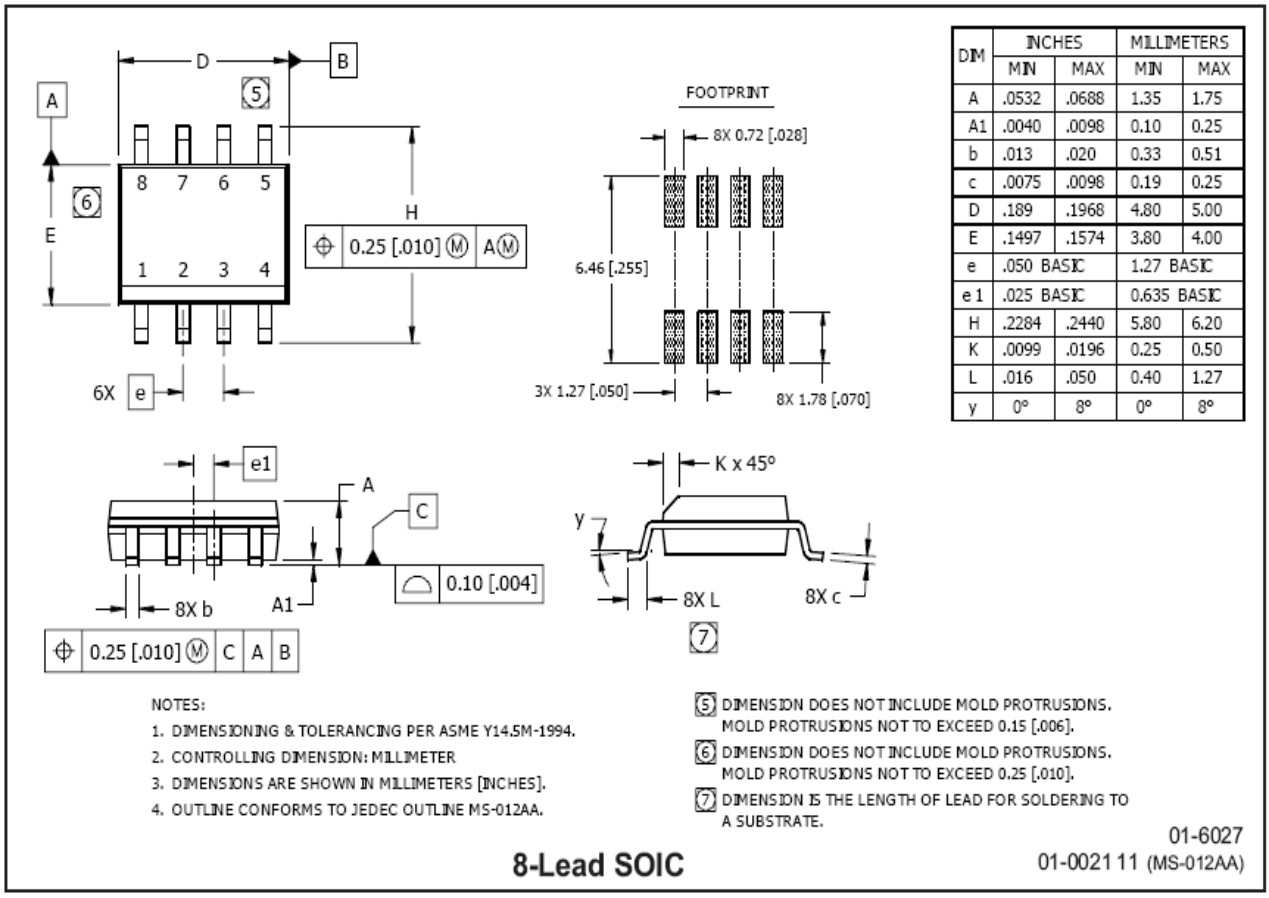


Figure 12: Brown-Out Protection Thresholds vs. Temperature

Package Details: SOIC8N



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

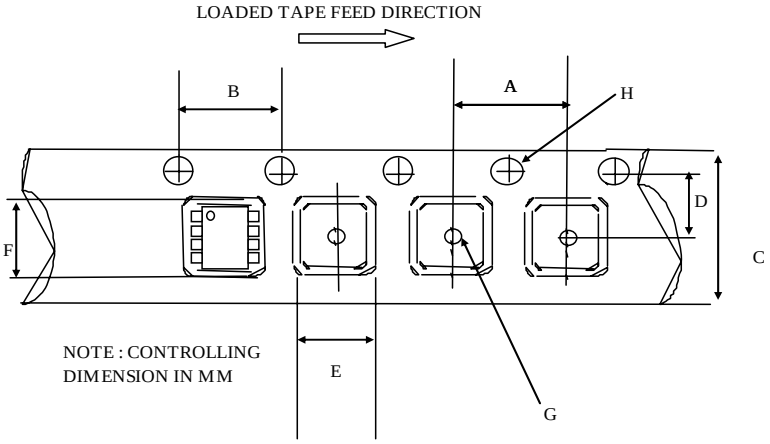
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

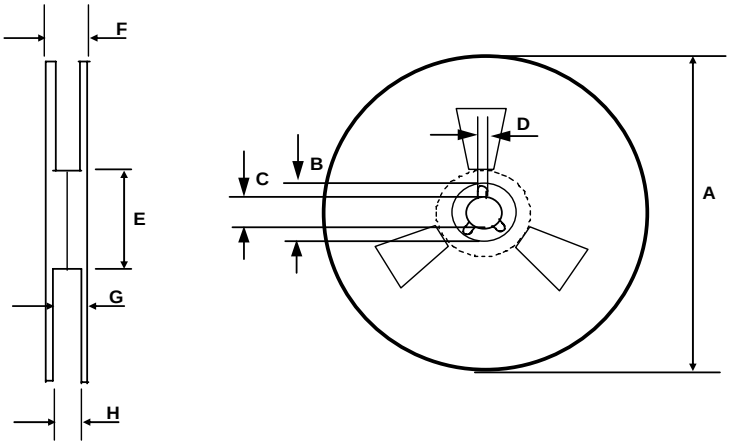
8-Lead SOIC

Tape and Reel Details: SOIC8N



CARRIER TAPE DIMENSION FOR 8SOICN

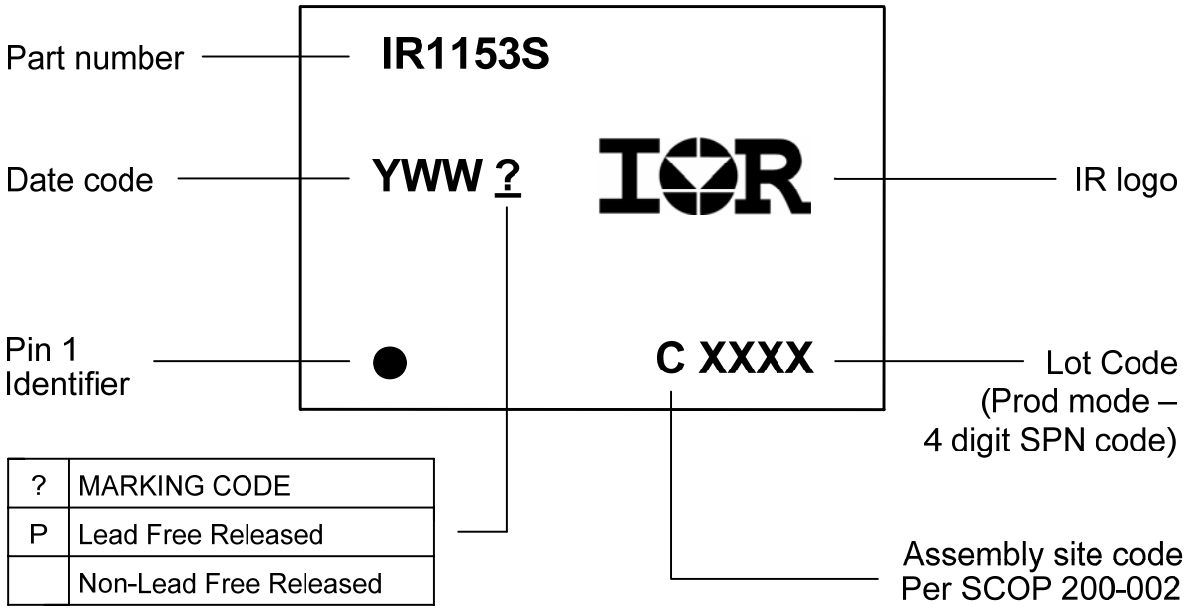
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IR1153S	SOIC8N	Tube/Bulk	95	IR1153SPBF
		Tape and Reel	2500	IR1153STRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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Tel: (310) 252-7105