



#### SUD50N04-05L

Vishay Siliconix

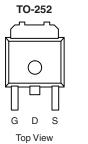
# N-Channel 40-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
V <sub>(BR)DSS</sub> (V)	$r_{\text{DSS}}(V)$ $r_{\text{DS(on)}}(\Omega)$ $I_{\text{DS}}(O)$		
40	0.0054 at V <sub>GS</sub> = 10 V	115	
	0.0069 at V <sub>GS</sub> = 4.5 V	102	

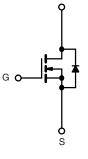
#### **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFETS
- 175 °C Junction Temperature





Drain Connected to Tab



D

Ordering Information: SUD50N04-05L-E3 (Lead (Pb)-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A$	= 25 °C, unless othe	rwise noted			
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	40	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current ( $T_1 = 175 \text{ °C}$ )	T <sub>C</sub> = 25 °C	I_	115 <sup>c</sup>	А	
Continuous Drain Current (1) = 175 C)	T <sub>C</sub> = 100 °C	I <sub>D</sub>	81 <sup>c</sup>		
Pulsed Drain Current		I <sub>DM</sub>	100		
Single Pulse Avalanche Current		I <sub>AS</sub>	50		
L = 0.1 mH		E <sub>AS</sub>	125	mJ	
Power Dissipation	T <sub>C</sub> = 25 °C	PD	136	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
	t ≤ 10 sec	R <sub>thJA</sub>	15	18	°C/W
Junction-to-Ambient <sup>D</sup>	Steady State		40	50	
Junction-to-Case		R <sub>thJC</sub>	0.85	1.1	

Notes:

a. Duty cycle ≤ 1 %.

b. Surface Mounted on 1" FR4 board.

c. Based on maximum allowable Junction Temperature. Package limitation current is 50 A.

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<b>SPECIFICATIONS</b> T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static	T			T	1		
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	40			v	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1		3		
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 40 V, V_{GS} = 0 V$			1	μΑ	
		$V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_{J}$ = 125 °C			50		
		$V_{DS} = 40$ V, $V_{GS} = 0$ V, $T_{J} = 175$ °C			150		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 V, V_{GS} = 10 V$	50			А	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0044	0.0054	Ω	
	r	$V_{GS}$ = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.0083		
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.0130		
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0055	0.0069		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	20	80		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		5600		pF	
Output Capacitance	C <sub>oss</sub>			590			
Reversen Transfer Capacitance	C <sub>rss</sub>			365			
Total Gate Charge <sup>c</sup>	Qg			90	135	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS}$ = 20 V, $V_{GS}$ = 10 V, $I_D$ = 50 A		19			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			19			
Gate Resistance	Rg			1.6		Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			15	25	ns	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 20 \text{ V, } \text{R}_{\text{L}} = 0.4 \Omega$ $\text{I}_{\text{D}} \cong 50 \text{ A}, \text{V}_{\text{GEN}} = 10 \text{ V, } \text{R}_{\text{g}} = 2.5 \Omega$		20	30		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			65	100		
Fall Time <sup>c</sup>	t <sub>f</sub>			11	20		
Source-Drain Diode Ratings and Cha	aracteristics	(T <sub>C</sub> = 25 °C) <sup>b</sup>		<u> </u>			
Continuous Current	ا <sub>S</sub>				50	^	
Pulsed Current	I <sub>SM</sub>				100	A	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		0.90	1.50	V	
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 30 A, di/dt = 100 A/μs		30	45	ns	

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

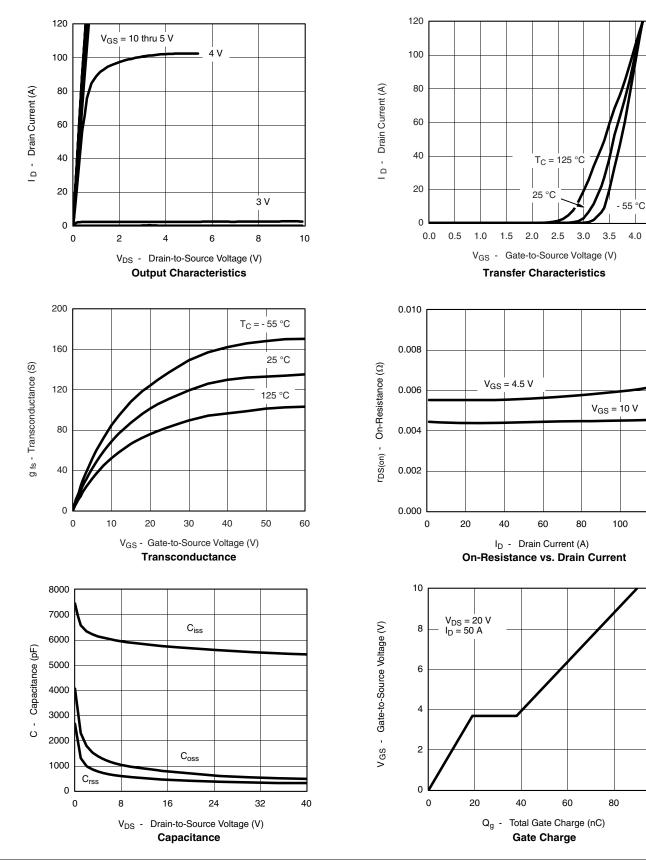


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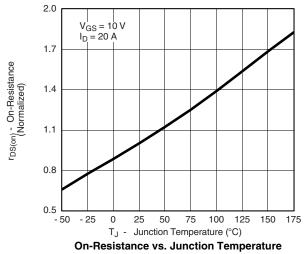
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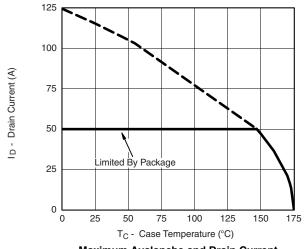
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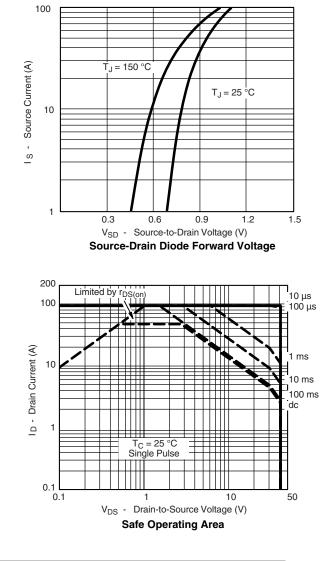
#### TYPICAL CHARACTERISTICS 25 °C unless noted

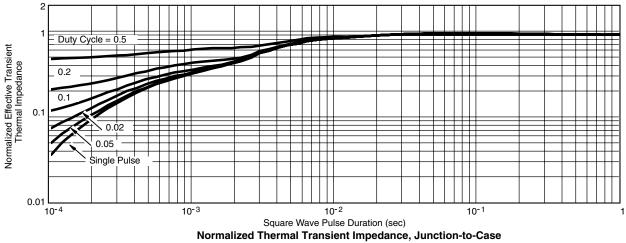


**THERMAL RATINGS** 



Maximum Avalanche and Drain Current vs. Case Temperature





Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72786.



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