



EMIF02-SPK01F1

IPAD™

2 LINES EMI FILTER AND ESD PROTECTION

MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required :

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF02-SPK01 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 flip chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.07mm x 1.47mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging

COMPLIES WITH THE FOLLOWING STANDARDS: IEC 61000-4-2

- Level 4 on input pins 15kV (air discharge)
8kV (contact discharge)
- Level 1 on output pins 2kV (air discharge)
2kV (contact discharge)

MIL STD 883E -Method 3015-6 Class 3

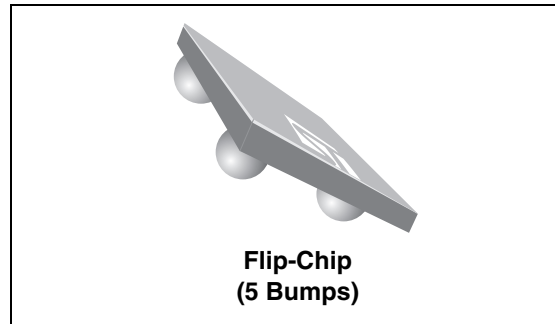


Table 1: Order Code

Part Number	Marking
EMIF02-SPK01F1	FX

Figure 1: Pin Configuration (ball side)

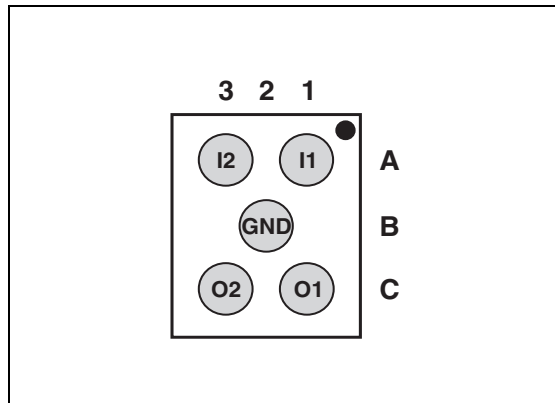
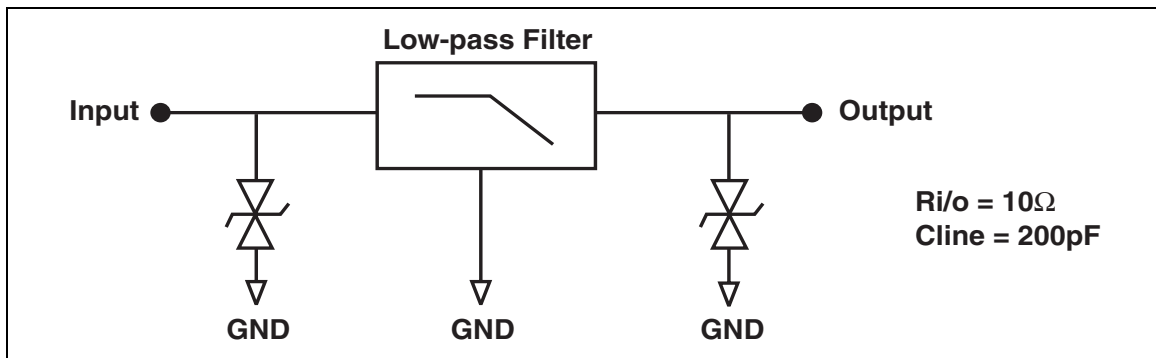


Figure 2: Basic Cell Configuration



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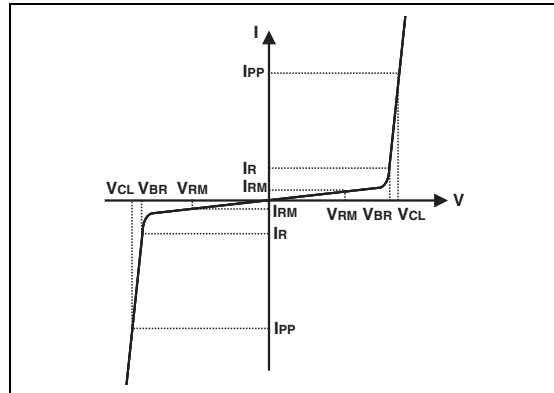
EMIF02-SPK01F1

Table 2: Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to 50	°C

Table 3: Electrical Characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	8		V
I_{RM}	$V_{RM} = 3\text{V per line}$			500	nA
$R_{I/O}$	Tolerance $\pm 20\%$		10		Ω
C_{line}	$V_R = 0\text{V}$		200		pF

Figure 3: S21 (dB) attenuation measurements and ApIac simulation

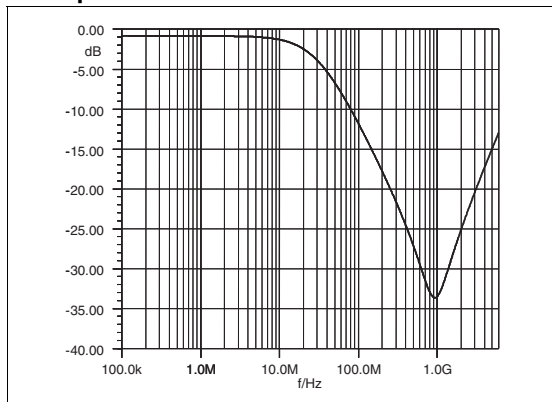


Figure 4: Analog crosstalk measurements

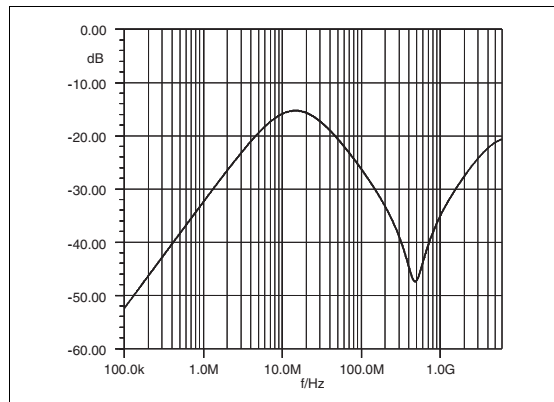


Figure 5: ESD response to IEC61000-4-2 (+ 15kV air discharge) on one input V(in) and one output V(out)

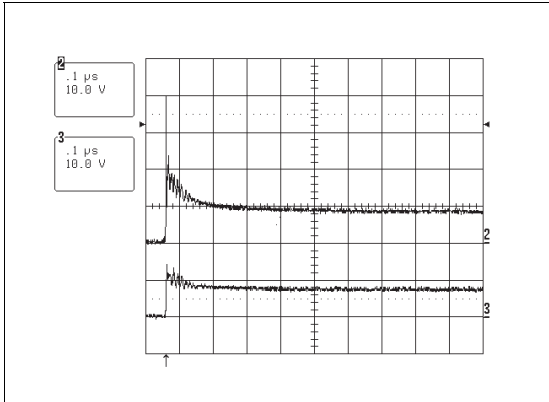


Figure 6: ESD response to IEC61000-4-2 (15kV air discharge) on one input V(in) and one output V(out)

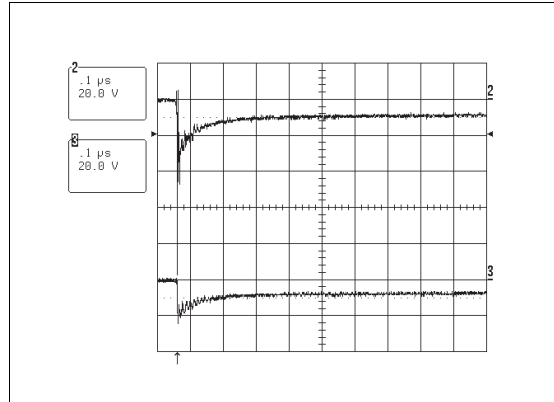


Figure 7: Line capacitance versus applied voltage

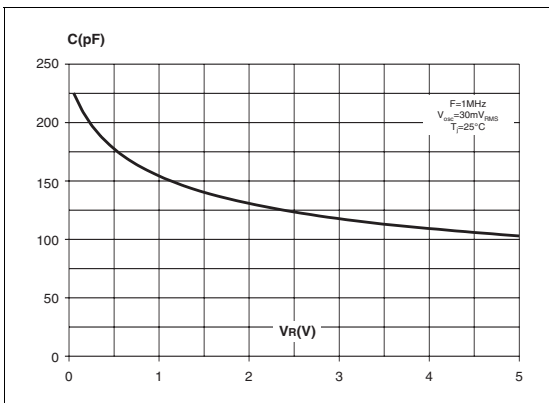


Figure 8: Aplac model

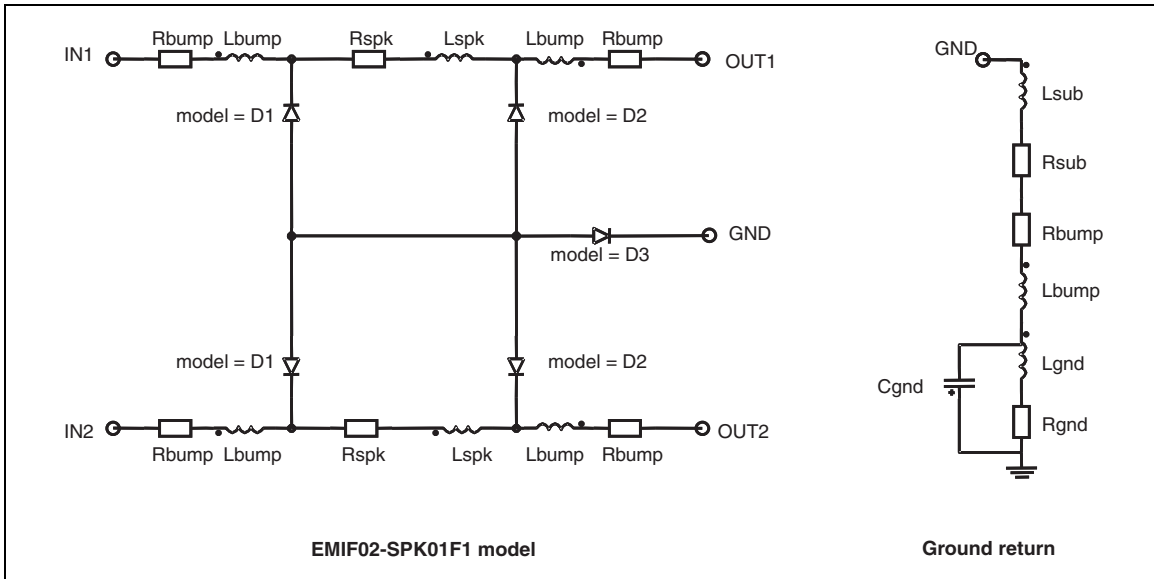


Figure 9: Aplac parameters

Model D1	Model D3	Model D2	aplcvar Ls 1nH
CJO=Cdiode1	CJO=Cdiode3	CJO=Cdiode2	aplcvar Rs 150m
BV=7	BV=7	BV=7	aplcvar Rspk 10
IBV=1u	IBV=1u	IBV=1u	aplcvar Lspk 10p
IKF=1000	IKF=1000	IKF=1000	aplcvar Cdiode1 234pF
IS=10f	IS=10f	IS=10f	aplcvar Cdiode2 3.5ppF
ISR=100p	ISR=100p	ISR=100p	aplcvar Cdiode3 1nF
N=1	N=1	N=1	aplcvar Lbump 50pH
M=0.3333	M=0.3333	M=0.3333	aplcvar Rbump 10m
RS=0.7	RS=0.12	RS=0.3	aplcvar Rsub 0.5m
VJ=0.6	VJ=0.6	VJ=0.6	aplcvar Lsub 10pH
TT=50n	TT=50n	TT=50n	aplcvar Rgnd 1m
			aplcvar Lgnd 50pH
			aplcvar Cgnd 0.15pF

Figure 10: Order code

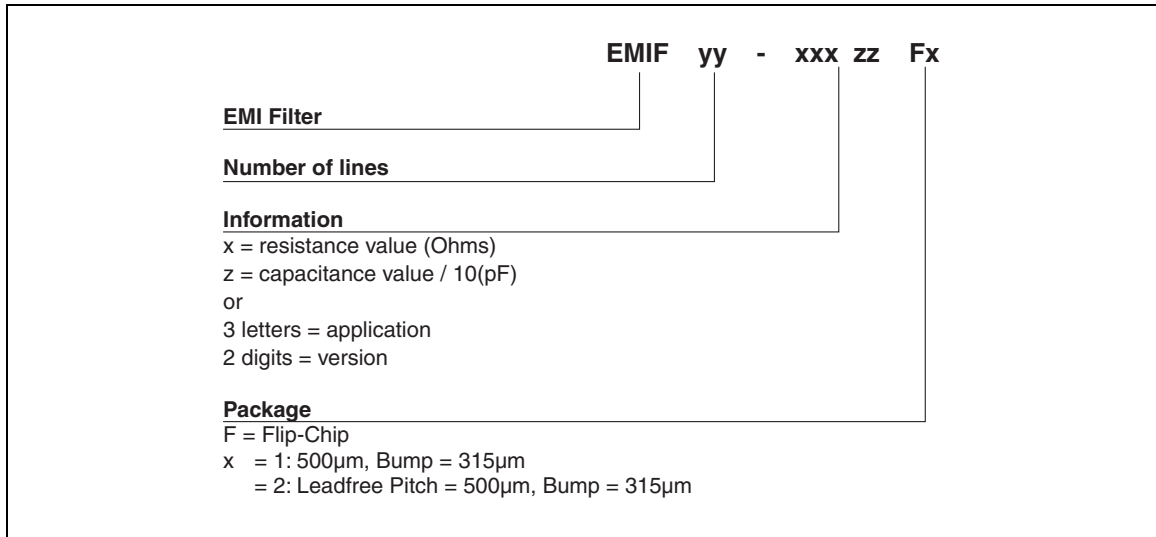


Figure 11: FLIP-CHIP Package Mechanical Data

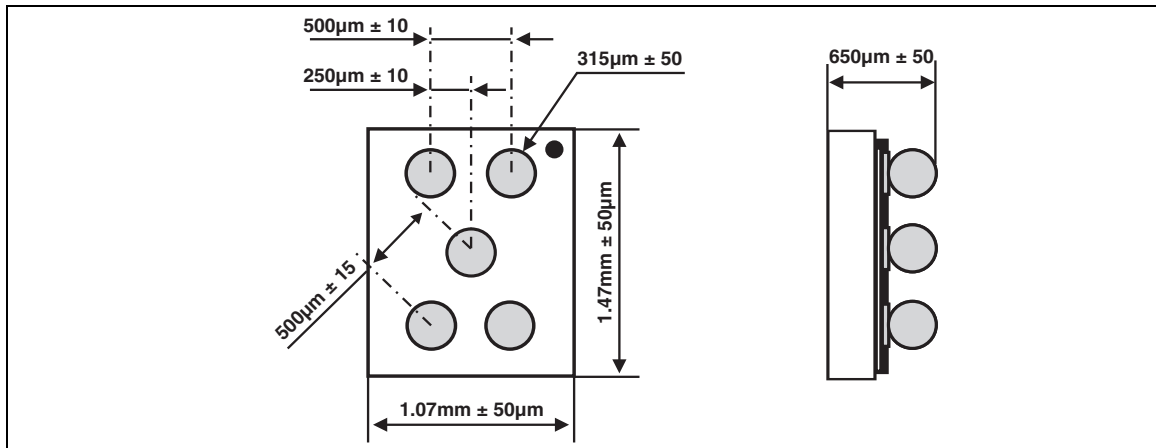


Figure 12: Foot print recommendations

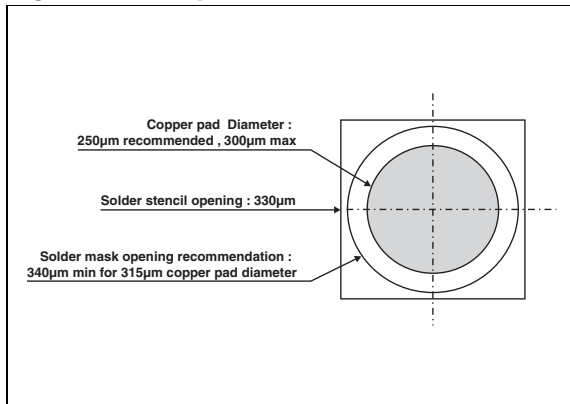


Figure 13: Marking

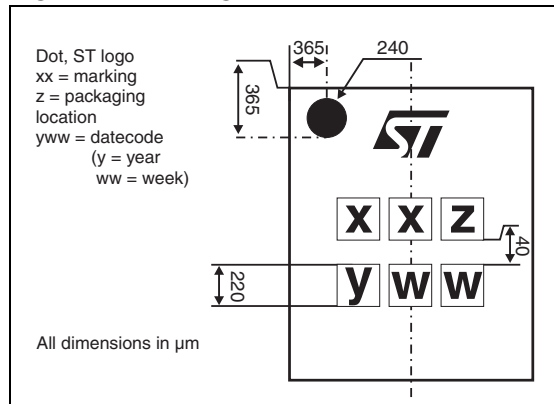


Figure 14: FLIP-CHIP Tape and Reel Specification

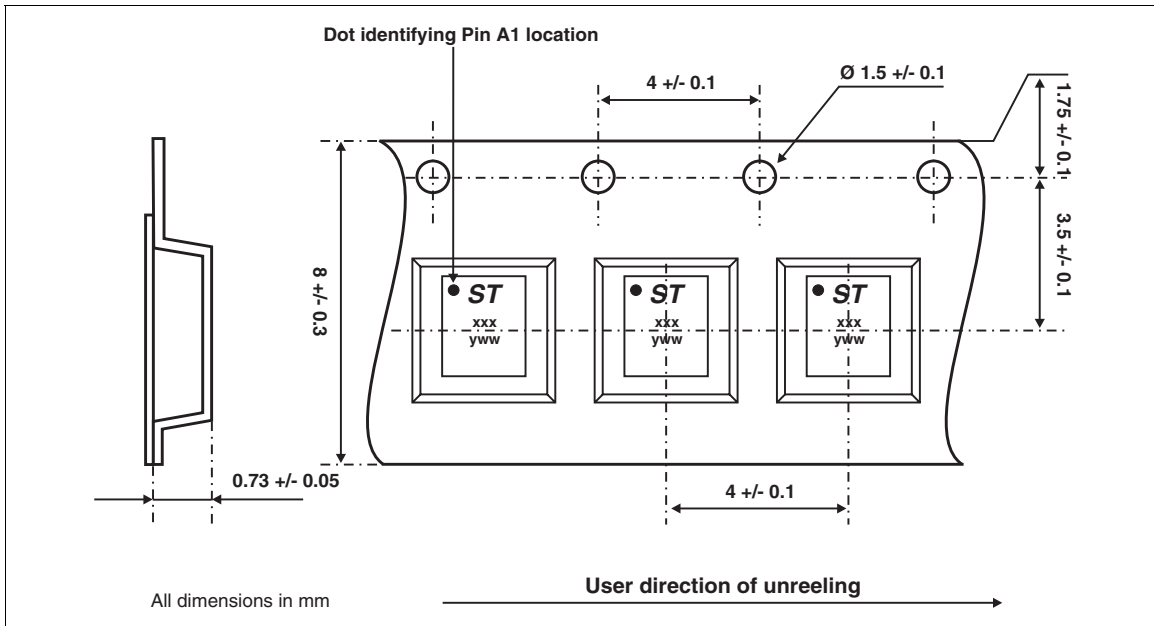


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-SPK01F1	FXT	Flip Chip	2.1 mg	5000	Tape & reel (7")

Note: More packing informations are available in the application notes
 AN1235: "Flip-Chip: Package description and recommendations for use"
 AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
Jan-2004	2A	Last update.
07-Oct-2004	3	Pin configuration figure one page one: "C" bumps range re-allocated

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