

10-line IPAD™, EMI filter including ESD protection

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming:
2.42 mm x 2.42 mm
- Very thin package: 0.650 mm
- High efficiency in ESD suppression on both input and output pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging

Complies with the following standards:

- IEC 61000-4-2 level 4
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883F - Method 3015.7 Class 3

Applications

Where EMI filtering in ESD sensitive equipment is required:

- Mobile Phones
- Computers and printers
- Communication systems
- MCU Boards

Description

The EMIF10-1K010F2 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

Additionally, this filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

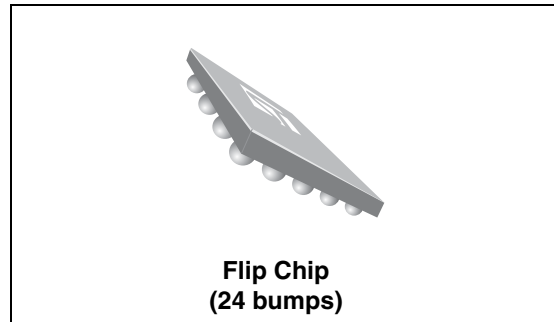


Figure 1. Pin configuration (bump side)

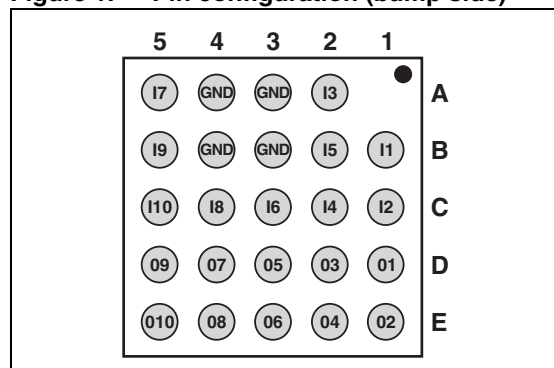
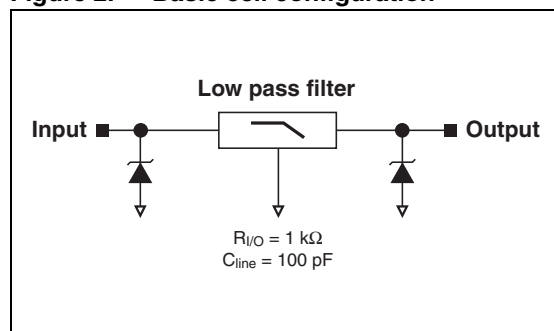


Figure 2. Basic cell configuration



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1 Characteristics

Table 1. Absolute ratings ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2		
	– Air discharge	15	kV
	– Contact discharge	8	
MIL STD 883F - Method 3015.7 Class 3	25		
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter				
V_{BR}	Breakdown voltage				
I_{RM}	Leakage current @ V_{RM}				
V_{RM}	Stand-off voltage				
V_{CL}	Clamping voltage				
R_d	Dynamic impedance				
I_{PP}	Peak pulse current				
$R_{I/O}$	Resistance between Input and Output				
C_{line}	Input capacitance per line				
V_{BR}	$I_R = 1\text{ mA}$				
I_{RM}	$V_{RM} = 3\text{ V per line}$			200	nA
R_d	$I_{PP} = 10\text{ A}, t_p = 2.5\text{ }\mu\text{s}$		1		Ω
$R_{I/O}$		900	1000	1100	Ω
C_{line}	$F = 1\text{ MHz } V_{OSC} = 30\text{ mV } V_{line} = 0\text{ V}$	80	100	120	pF

Figure 3. S21(db) attenuation measurement

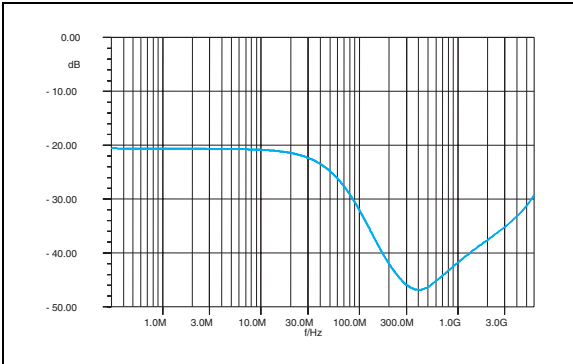


Figure 4. Analog cross talk measurements

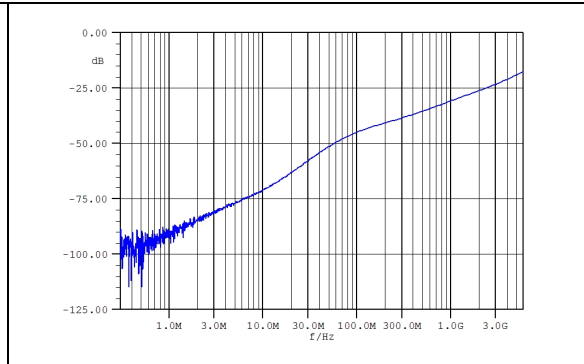


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

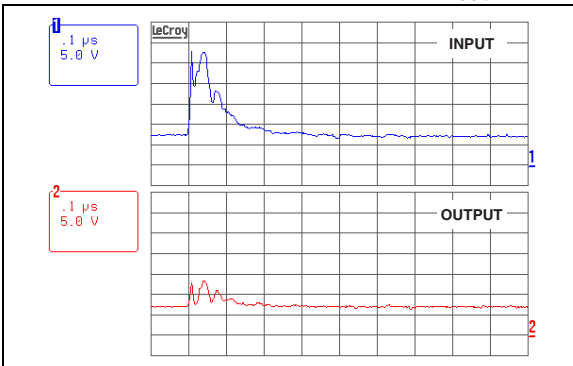


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

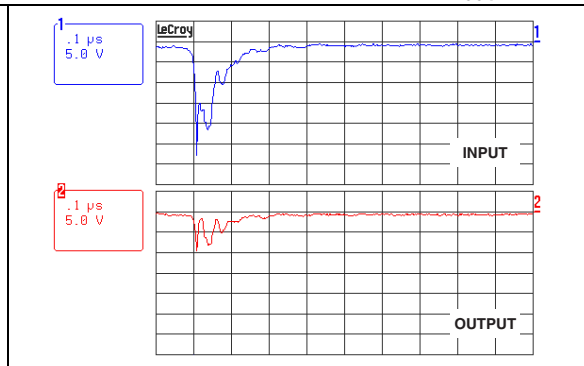
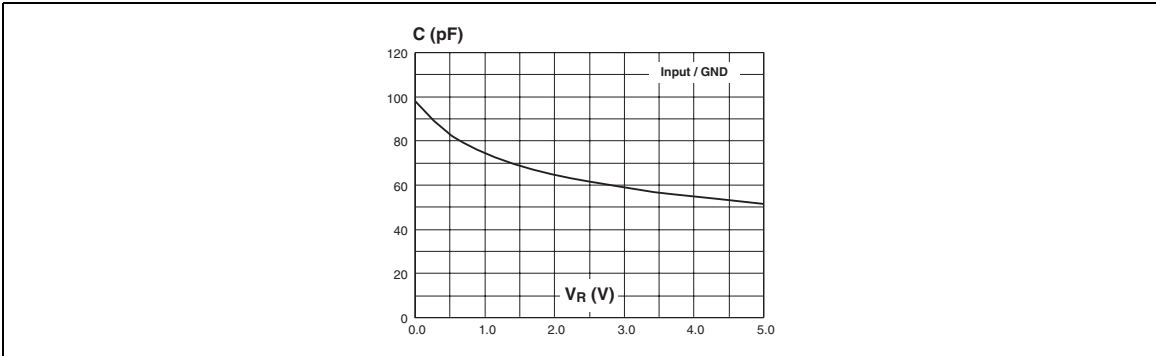


Figure 7. Capacitance versus reverse applied voltage



2 Application information

Figure 8. Aplac model

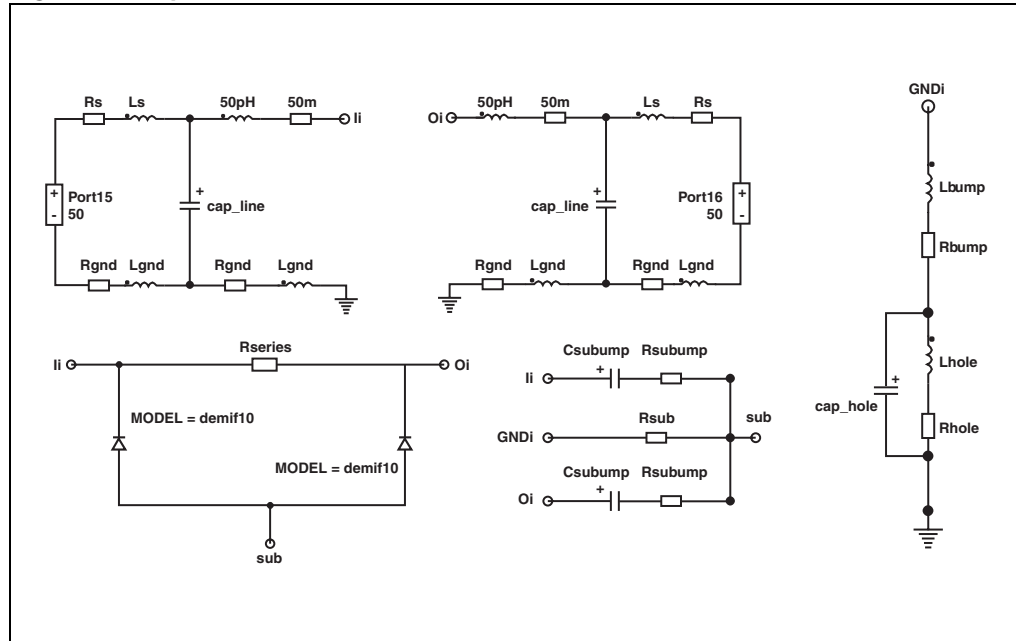
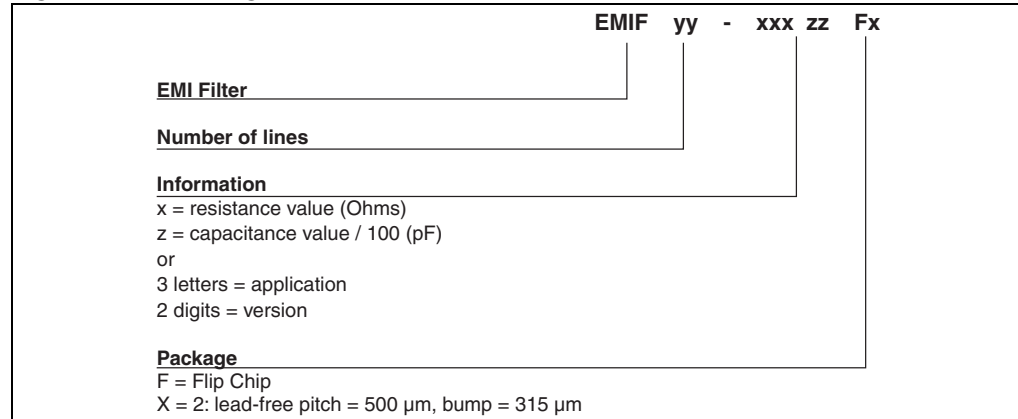


Figure 9. Aplac parametersl

Cz	57pF	Model demif10
Rseries	960	BV = 7
cap_line	0.8pF	IBV = 1m
Ls	0.6nH	CJO = Cz
Rbump	50m	M = 0.3333
Lbump	50pH	Rs = 1
Rs	0.15	VJ = 0.6
Csubump	15pF	TT = 100n
Rsubump	0.15	
Rsub	0.1	
lhole	1.2nH opt	
Rhole	0.15	
cap_hole	0.15pF	
Rgnd	0.25	
lgnd	0.4nH	

3 Ordering information scheme

Figure 10. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 11. Flip Chip package dimensions

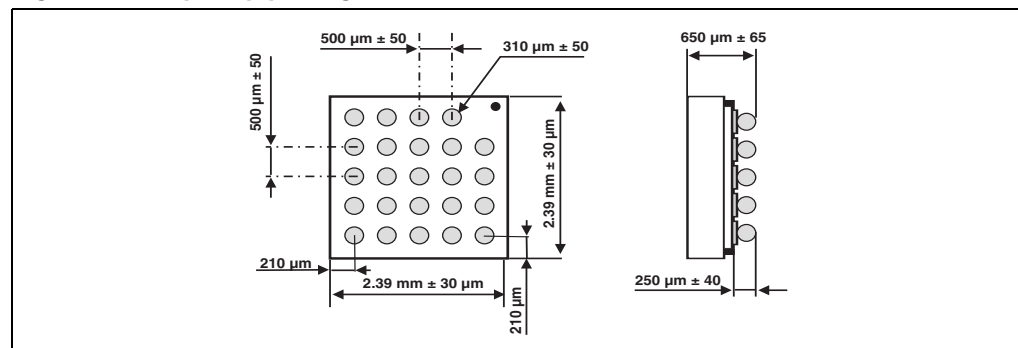


Figure 12. Footprint recommendations Figure 13. Marking

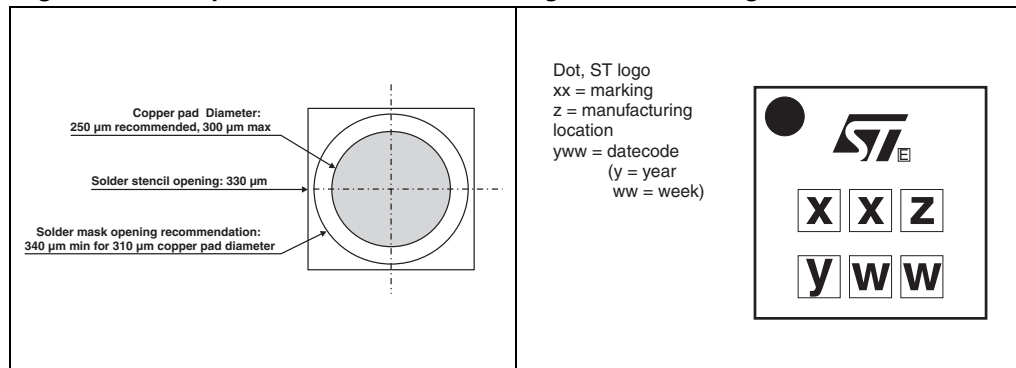
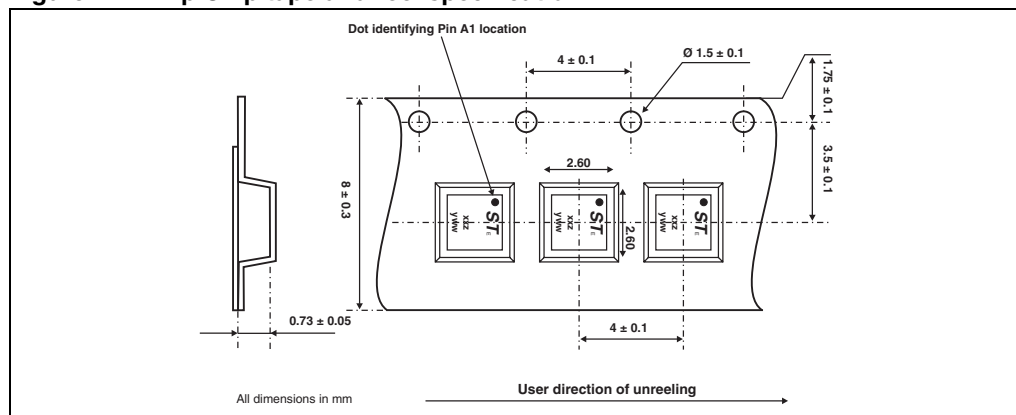


Figure 14. Flip Chip tape and reel specification



5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-1K010F2	FD	Flip Chip	7.9 mg	5000	Tape and reel

Note: More information is available in the application notes:
 AN1235: "Flip Chip: Package description and recommendations for use"
 AN1751: "EMI Filters: Recommendations and measurements"

6 Revision history

Table 4. Document revision history

Date	Revision	Description of changes
12-Oct-2004	1	First issue.
28-Aug-2006	2	Die layout upgrade.
18-Sep-2006	3	Added pocket dimensions to Figure 11.
17-Apr-2008	4	Updated ECOPACK statement. Updated Figure 10 , Figure 11 , Figure 12 , and Figure 14 . Reformatted to current standards.

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