



## METAL DIP CLOCK OSCILLATOR

### FEATURES

- Standard 14 Pin or 8 Pin DIP Footprint
- HCMOS/TTL Compatible
- **Fundamental and 3<sup>RD</sup> Overtone Crystals**
- Frequency Range 1.0 – 105.561 MHz
- Frequency Stability,  $\pm 50$  ppm Standard ( $\pm 25$  ppm and  $\pm 20$  ppm available)
- +5.0Vdc Operation
- Operating Temperature to  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Output Enable Option
- **RoHS/Green Compliant (6/6)**

### DESCRIPTION

The MXO45/MXO45HS is a DIP packaged Clock oscillator offering reliable performance at an economical cost. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.



### ORDERING INFORMATION



Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.

Example Part Number: MXO45-3C-32M7680 or MXO45HS-3C-32M7680

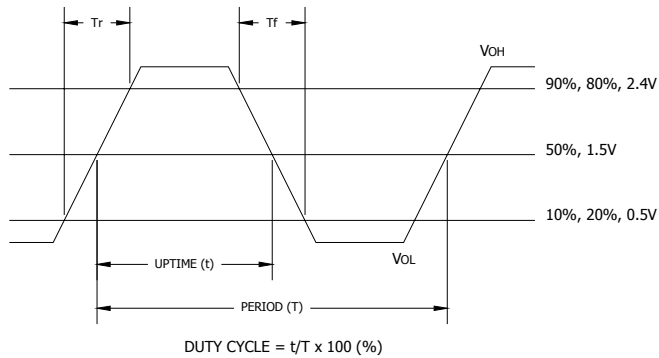
**ELECTRICAL CHARACTERISTICS**

|                                    | PARAMETER  | SYMBOL                             | CONDITIONS                         | MIN                                      | TYP | MAX                | UNIT          |    |
|------------------------------------|--|------------------------------------|------------------------------------|--|-----|--------------------|---------------|----|
| Absolute Maximums                  | Maximum Supply Voltage                                       | $V_{CC}$                           | -                                  | -0.5                                     | -   | 7.0                | V             |    |
|                                    | Storage Temperature  | $T_{STG}$                          | -                                  | -55                                      | -   | 125                | °C            |    |
|                                    | Frequency Range  | $f_0$                              | -                                  | 1.0                                      | -   | 105.561            | MHz           |    |
|                                    | Frequency Stability<br>(See Note 1 and Ordering Information) | $\Delta f/f_0$                     | -                                  | -  | -   | 20,25,50<br>or 100 | ± ppm         |    |
|                                    | Operating Temperature<br>Commercial<br>Industrial            | $T_A$                              | -                                  | -20<br>-40                               | 25  | 70<br>85           | °C            |    |
| Electrical and Waveform Parameters | Supply Voltage   | $V_{CC}$                           | ± 10 %                             | 4.5                                      | 5.0 | 5.5                | V             |    |
|                                    | Supply Current   | $I_{CC}$                           | 1.0 MHz to 20 MHz $C_L=50pF$       | -  | 10  | 25                 | mA            |    |
|                                    |  |                                    | 20.1 MHz to 80 MHz $C_L=30pF$      | -  | 30  | 50                 |               |    |
|                                    |  |                                    | 80.1 MHz to 105.561 MHz $C_L=15pF$ | -  | 40  | 100                |               |    |
|                                    | Output Load<br>CMOS  | $C_L$                              | 1.0 MHz to 50 MHz                  | -  | -   | 50                 | pF            |    |
|                                    |  |                                    | 50.1 MHz to 80 MHz                 | -  | -   | 30                 |               |    |
|                                    | TTL  |                                    | 80.1 MHz to 105.561 MHz            | -  | -   | 15                 | TTL           |    |
|                                    |  |                                    | 1.0 MHz to 105.561 MHz             | -  | -   | 10                 |               |    |
|                                    | Output Voltage Levels<br>Logic '1' Level                     | $V_{OH}$                           | CMOS Load                          | 0.9* $V_{CC}$<br>$V_{CC}-0.6V$           | -   | -                  | -             | V  |
|                                    |  |                                    | 10 TTL LOAD                        |  | -   | -                  | -             |    |
|                                    | Logic '0' Level  | $V_{OL}$                           | CMOS                               | -  | -   | -                  | 0.1* $V_{CC}$ | V  |
|                                    |  |                                    | TTL Load                           |  | -   | -                  | 0.4           |    |
|                                    | Output Current<br>Logic '1' Level                            | $I_{OH}$                           | $V_{OH} = 3.9V$ $V_{CC} = 4.5V$    | -  | -   | -16                | mA            |    |
|                                    |  |                                    | Logic '0' Level                    | $I_{OL}$ $V_{OL} = 0.4V$ $V_{CC} = 4.5V$ | -   | -                  |               | 16 |
|                                    | Output Duty Cycle  | SYM                                | @ 50% Level                        | 45                                       | -   | 55                 | %             |    |
| Rise and Fall Time                 | $T_{R}$ $T_{F}$  | @ 10% - 90% Levels                 | -                                  | -  | -   | ns                 |               |    |
|                                    |  | 1.0 MHz to 50 MHz $C_L=50pF$       | -                                  | 8  | 10  |                    |               |    |
|                                    |  | 50.1 MHz to 80 MHz $C_L=30pF$      | -                                  | 4  | 8   |                    |               |    |
|                                    |  | 80.1 MHz to 105.561 MHz $C_L=15pF$ | -                                  | 2.5                                      | 5   |                    |               |    |
| Start Up Time                      | $T_S$  | Application of $V_{CC}$            | -                                  | -  | 10  | ms                 |               |    |
| Enable Function (See Note 2)       |  |                                    |                                    |  |     |                    |               |    |
| Enable Input Voltage               | $V_{IH}$   | Pin 1 Logic '1', Output Enabled    | 2.0                                | -  | -   | V                  |               |    |
| Disable Input Voltage              | $V_{IL}$   | Pin 1 Logic '0', Output Disabled   | -                                  | -  | 0.8 | V                  |               |    |
| Enable Time                        | $T_{PLZ}$  | Pin 1 Logic '1'                    | -                                  | -  | 100 | ns                 |               |    |
| Period Jitter, Pk-Pk               | -  | -                                  | -                                  | -  | 50  | ps                 |               |    |
| Period Jitter, RMS                 | -  | -                                  | -                                  | -  | 5   |                    |               |    |
| Phase Jitter, RMS                  | -  | Bandwidth 12 kHz - 20 MHz          | -                                  | -  | 1   |                    |               |    |

**Notes:**

- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and first year aging.
- Reference CTS Application Note 014-0002-0.

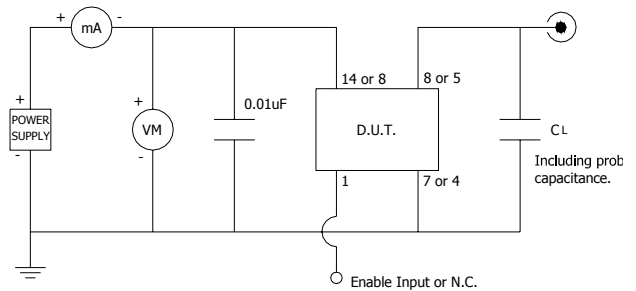
### CMOS/TTL OUTPUT WAVEFORM



### ENABLE TRUTH TABLE

| PIN 1     | PIN 5 or PIN 8 |
|-----------|----------------|
| Logic '1' | Output         |
| Open      | Output         |
| Logic '0' | High Imp.      |

### TEST CIRCUIT, CMOS LOAD

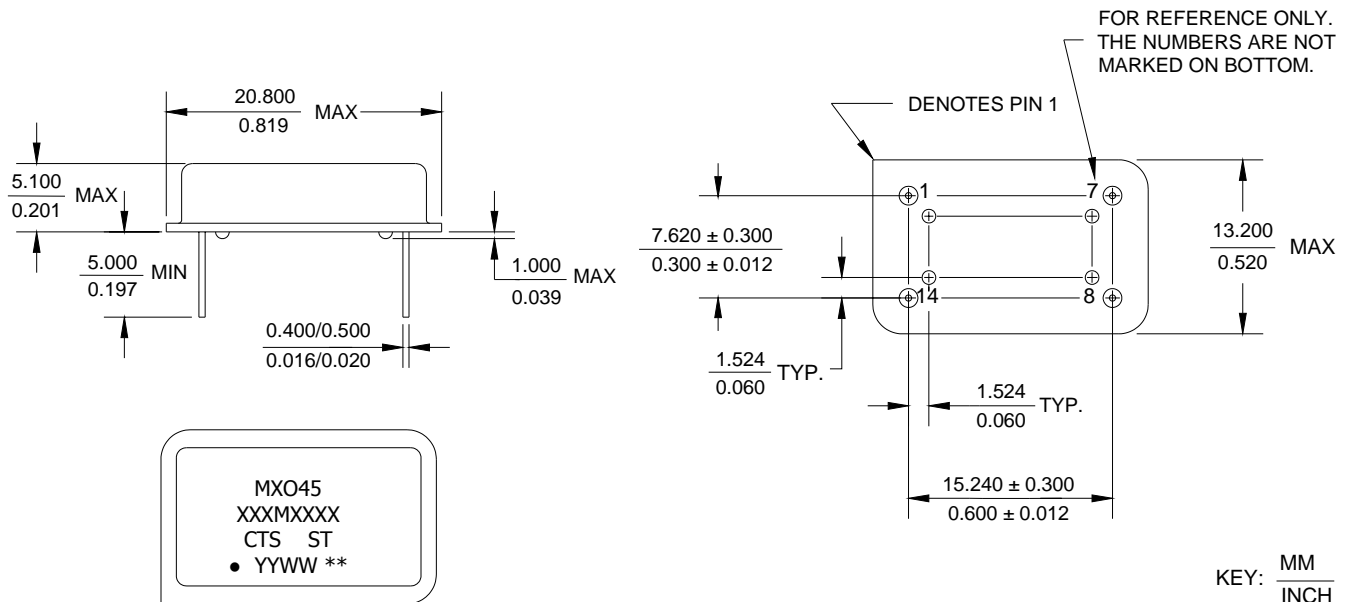


### D.U.T. PIN ASSIGNMENTS

| PIN     | SYMBOL          | DESCRIPTION                |
|---------|-----------------|----------------------------|
| 1       | EOH             | Enable Input or No Connect |
| 7 or 4  | GND             | Circuit & Package Ground   |
| 8 or 5  | Output          | RF Output                  |
| 14 or 8 | V <sub>CC</sub> | Supply Voltage             |

## MECHANICAL SPECIFICATIONS

### PACKAGE DRAWING DIP-14



### MARKING INFORMATION

1. Model Name: MXO45 or MXO45T.
2. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.
3. ST - Frequency stability/temperature code. (Reference Ordering Information.)
4. YYWW - Date code, YY - year, WW - week.
5. \*\* - Manufacturing Site Code.

### NOTES

1. Lead finish (e1), SnAgCu.
2. Reflow conditions per JEDEC J-STD-020.



**ENVIRONMENTAL SPECIFICATIONS**

|                                  |  |
|----------------------------------|--|
| Temperature Cycle:               | 400 cycles from -55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.                     |
| Mechanical Shock:                | 1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).                 |
| Sinusoidal Vibration:            | 0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total). |
| Gross Leak:                      | No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.  |
| Fine Leak:                       | Mass spectrometer leak rates less than $2 \times 10^{-8}$ ATM cc/sec air equivalent.   |
| Resistance to Solder Heat:       | Product must survive 3 reflows of +260°C peak, 10 seconds maximum.   |
| High Temperature Operating Bias: | 2,000 hours at +125°C, maximum bias, disregarding frequency shift.   |
| Frequency Aging:                 | 1,000 hours at +85°C, full bias, less than ±5 ppm shift.   |
| Moisture Sensitivity Level:      | Level 1 per JEDEC J-STD-020.   |

**QUALITY AND RELIABILITY**

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.