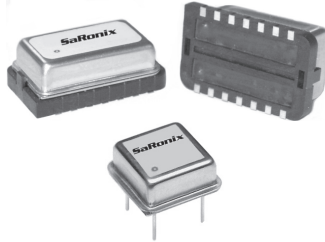## Crystal Clock Oscillator

5V, HCMOS
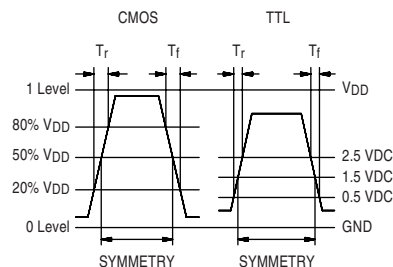
Technical Data

NTH / NCH Series

ACTUAL SIZE

Description

A 5V crystal controlled, low current, low jitter and high frequency oscillator with precise rise and fall times demanded in networking applications, such as Gigabit Ethernet and Fibre Channel. The tri-state function on the NTH enables the output to go high impedance. Device is packaged in a 14 or an 8-pin DIP compatible resistance welded, all metal grounded case, to reduce EMI. True SMD DIL 14 version also available, utilizing new adaptor technology (see separate data sheet for package dimensions)

Applications & Features

- ADSL, DSL
- DS3, ES3, E1, STS-1, T1
- Ethernet Switch, Gigabit Ethernet
- Fibre Channel Controller
- MPEG
- Network Processors
- Voice Over Packet
- 32 Bit Microprocessors
- Tri-State output on NTH
- True SMD version available, see part number builder for package option

Output Waveform

Frequency Range:	500 kHz to 106.25 MHz
Frequency Stability: *See Part Numbering Guide	±20*, ±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, 30 day aging, shock and vibration.

Temperature Range:

Operating:	0 to +70°C or -40 to +85°C
Storage:	-55 to +125°C

Supply Voltage:

Recommended Operating:	+5VDC ±10%

Supply Current:

0.5 to 8 MHz:	12mA
8+ to 24 MHz:	20mA
24+ to 50 MHz:	35mA
50+ to 80 MHz:	50mA
80+ to 106.25 MHz:	65mA

Output Drive:

HCMOS

Symmetry:	measured @ 50%V_{DD}, See Part Numbering Guide
Rise & Fall Times:	8ns max, 0.5 to 24 MHz, 20% to 80% V_{DD}
	5ns max, 24+ to 80 MHz
	2ns max, 80+ to 106.25 MHz
Logic 0:	10% V_{DD} max
Logic 1:	90% V_{DD} min
Load:	50pF to 50MHz, 30pF 50+ to 70 MHz, 15pF 70+ to 106.25 MHz
RMS Period Jitter:	8ps max

TTL

Symmetry:	measured @ 1.5V level, See Part Numbering Guide
Rise & Fall Times:	6ns max, 0.5 to 24 MHz, 0.5 to 2.5V
	3ns max, 24+ to 80 MHz
	1.5ns max, 80+ to 106.25 MHz
Logic 0:	0.5 V max
Logic 1:	V_{CC} -0.6V min
Load:	10TTL to 50MHz, 5TTL 50+ to 106.25 MHz
RMS Period Jitter:	8ps max

Mechanical:

Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-883, Method 2004, Conditions B2
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition A, B or C (I or J for Gull Wing and SMD)

Environmental:

Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

Tri-State Logic Table (NTH only)

Pin 1 Input	Pin 8 (5) Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 1:
Logic 1 = 3.0 V min
Logic 0 = 0.5 V max

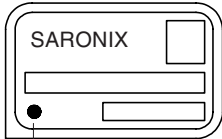| Output:	Oscillation @ V_{IN}, 2.2V min
Output:	High Impedance @ V_{IN}, 0.8V max
Internal Pullup Resistance	50KΩ min
Control Input:	Disable Output Delay: 100ns max

DS-104   REV F

Crystal Clock Oscillator

5V, HCMOS

Technical Data

NTH / NCH Series

Package Details
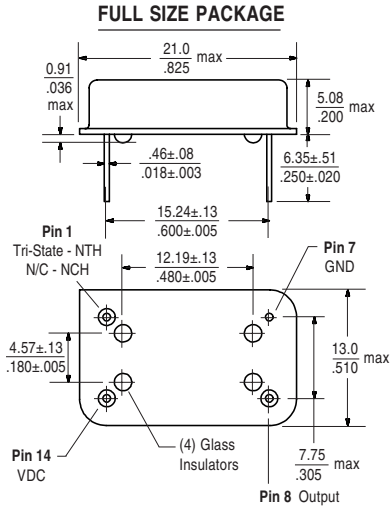
FULL SIZE PACKAGE

21.0 / .825 max
0.91 / .036 max
5.08 / .200 max
.46±.08 / .018±.003
6.35±.51 / .250±.020
15.24±.13 / .600±.005

Pin 1 Tri-State - NTH N/C - NCH
Pin 7 GND
12.19±.13 / .480±.005
4.57±.13 / .180±.005
13.0 / .510 max
Pin 14 VDC
(4) Glass Insulators
7.75 / .305 max
Pin 8 Output

Marking Format **
Includes Date Code, Frequency, Part Number

SARONIX

Denotes Pin 1

HALF SIZE PACKAGE

13.0 / .510 max
10.87 / .428 max
0.91 / .036 max
5.08 / .200 max
.46±.08 / .018±.003
6.35±.051 / 0.25±0.02
7.62±.20 / .300±.008

Pin 1 Tri-State - NTH N/C - NCH
Pin 4 GND
⌀ 1.5 / .059
13.0 / .510 max
120° 120° 120°
7.62±.20 / .300±.008
Pin 8 VDC
⌀ 1.7 / .067
⌀ 6.0 / .236
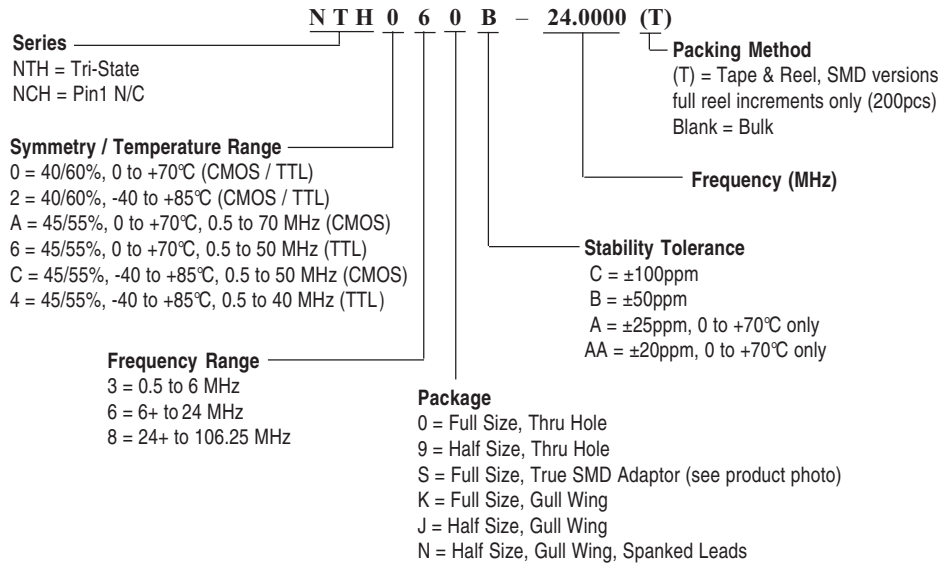**Pin 5** Output

Marking Format **
Includes Date Code, Frequency, Part Number

SARONIX

Denotes Pin 1
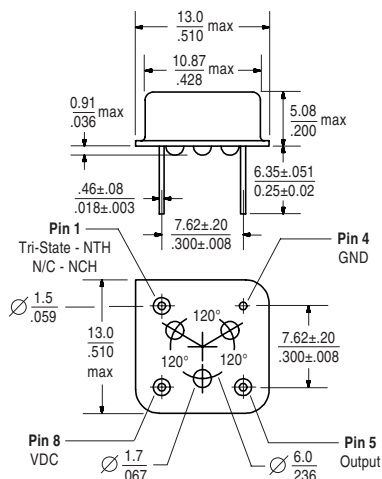
** Exact location of items may vary

Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

N T H 0 6 0 B – 24.0000 (T)

Series
NTH = Tri-State
NCH = Pin1 N/C

Symmetry / Temperature Range
0 = 40/60%, 0 to +70℃ (CMOS / TTL)
2 = 40/60%, -40 to +85℃ (CMOS / TTL)
A = 45/55%, 0 to +70℃, 0.5 to 70 MHz (CMOS)
6 = 45/55%, 0 to +70℃, 0.5 to 50 MHz (TTL)
C = 45/55%, -40 to +85℃, 0.5 to 50 MHz (CMOS)
4 = 45/55%, -40 to +85℃, 0.5 to 40 MHz (TTL)

Frequency Range
3 = 0.5 to 6 MHz
6 = 6+ to 24 MHz
8 = 24+ to 106.25 MHz

Package
0 = Full Size, Thru Hole
9 = Half Size, Thru Hole
S = Full Size, True SMD Adaptor (see product photo)
K = Full Size, Gull Wing
J = Half Size, Gull Wing
N = Half Size, Gull Wing, Spanked Leads

Stability Tolerance
C = ±100ppm
B = ±50ppm
A = ±25ppm, 0 to +70℃ only
AA = ±20ppm, 0 to +70℃ only

Frequency (MHz)

Packing Method
(T) = Tape & Reel, SMD versions full reel increments only (200pcs)
Blank = Bulk

Test Circuits

mA M
+ −
POWER SUPPLY
+
−
V M
+
−
Pin 14 (8)
Vcc   OUT
OSCILLATOR
GND
Pin 1 (1)*
TEST POINT
Pin 8 (5)
Pin 7 (4)
C_L = see specs on previous pg (Note A)
TRI-STATE INPUT (NTH only)
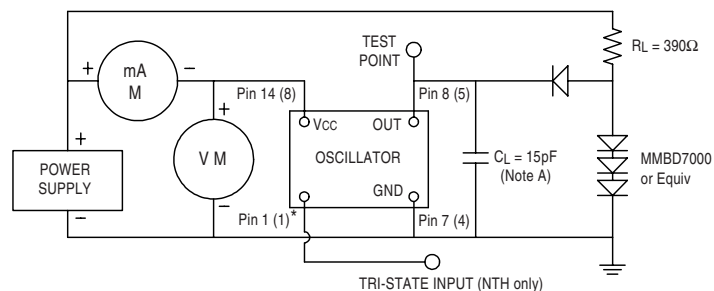
NOTE A: C_L includes probe and fixture capacitance
*( ) Indicates pin numbers for half-size package
HCMOS (Used at SaRonix)

mA M
+ −
POWER SUPPLY
+
−
V M
+
−
Pin 14 (8)
Vcc   OUT
OSCILLATOR
GND
Pin 1 (1)*
TEST POINT
Pin 8 (5)
Pin 7 (4)
R_L = 390Ω
C_L = 15pF (Note A)
MMBD7000 or Equiv
TRI-STATE INPUT (NTH only)

NOTE A: C_L includes probe and fixture capacitance
*( ) Indicates pin numbers for half-size package
TTL (Optional load)

All specifications are subject to change without notice.

DS-104   REV F

Technical Data

RECOMMENDED LAND PATTERN

REV A