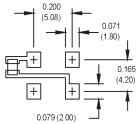


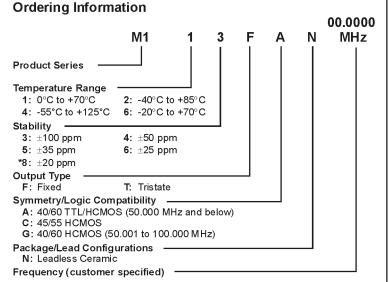
SUGGESTED SOLDER PAD LAYOUT



NOTE: A capacitor of value $0.01~\mu F$ or greater between Vdd and Ground is recommended.

Pin Connections

PIN	FUNCTION			
1	N/C or Tristate			
2	Ground			
3	Output			
4	+Vdd			



*Contact Factory for Availability M2010Sxxx - Contact factory for datasheet.

Г	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes		
tions	Frequency Range	F	1.5		100	MHz			
	Operating Temperature	TA	(See order	(See ordering information)					
	Storage Temperature	Ts	-55		+125	°C			
	Frequency Stability	ÄF/F	(See ordering information)						
	Aging								
	1 st Year			3		ppm			
	Thereafter (per year)			2		ppm			
	Input Voltage	Vdd	4.5	5.0	5.5	V			
	Input Current	ldd							
	1.500 to 20 MHz				20	mA			
	20.001 to 50 MHz				35/45	mA	TTL/HCMOS		
	50.001 to 100 MHz				65	mA			
l ca	Output Type						HCMOS/TTL		
Electrical Specifications	Load						See Note 1		
	1.500 to 50 MHz		10 TTL or	10 TTL or 50 pF					
	50.001 to 67 MHz		50 pF Max	50 pF Max					
	67.001 to 100 MHz			15 pF Max					
12	Symmetry (Duty Cycle)		(See order	(See ordering information)			See Note 2		
======================================	Logic "1" Level	Voh	90% Vdd			V	HCMOS Load		
			Vdd -0.5			V	TTL Load		
	Logic "0" Level	Vol			10% Vdd	V	HCMOS Load		
					0.5	V	TTL Load		
	Output Current				±16	mA			
	Rise/Fall Time	Tr/Tf					See Note 3		
	1.500 to 67 MHz				10	ns			
	67.001 to 125 MHz				3	ns			
	Tristate Function		Input Logic "1" or floating; output active						
			Input Logic "0"; output disables to high-Z						
	Start up Time				10	ms			
	Random Jitter	Rj		5	12	ps RMS	1-Sigma		
Ital	Mechanical Shock				6 mS duration, ½ sinewave)				
nen	Vibration		Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)						
l no	Hermeticity		STD-202, M						
Environmental	Thermal Cycle		Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell,						
ᇤ	Solderability		J-STD-002	****************					
	Max Soldering Conditions See solder profile, Figure 1								

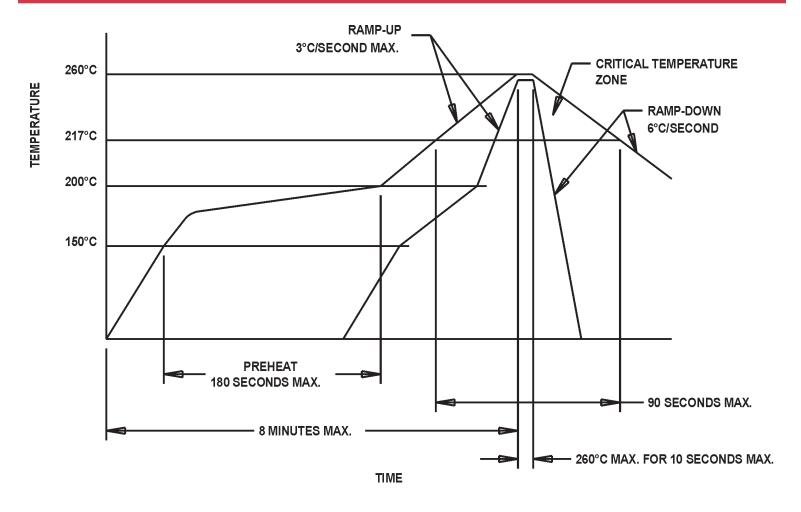
- 1. TTL load See load circuit diagram #1. HCMOS load See load circuit diagram #2.
- 2. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
- Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load.

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MtronPTI Lead Free Solder Profile



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