

# **Crystal Clock Oscillator**

3.3V, CMOS / TTL

## Technical Data S1633 Series





#### Description

The 3.3V S1633 is a crystal-controlled, low-current, low voltage oscillator providing precise rise and fall times to drive high performance applications. The miniature, low profile leadless ceramic package has gold-plated contact pads, ideal for today's pick-and-place SMT environments. These oscillators are contained in a rugged, subcompact 3.2x5mm package ideal for high density applications requiring tight frequency stability over a range of operating conditions.

#### **Applications & Features**

- Miniature, 1.3mm high ceramic package ideal for SMT applications
- 3.3V operation
- Extended frequency range and low jitter for a variety of networking, computing and communications applications requiring compact size or low power
- Low-power standby function included
- Perfect for high density, low power switches, routers, base stations, and storage devices
- Ideal for 802.11 applications
- Anywhere small size, low power, surface mountability are a priority
- Available on tape & reel; 16mm tape, 1000pcs per reel

Frequency Range:	1.8432 MHz to 125 MHz (as specified)

Frequency Stability: ±25ppm, ±50ppm over all conditions; calibration tolerance, operating temperature, rated input (supply) voltage changes,

load change, aging\*, shock and vibration

Aging\*: 1 year @ 25°C average ambient operating temperature

Temperature Range:

Operating: -20 to +70°C or -40 to +85°C (as specified)

Storage: -55 to +125°C

Supply Voltage:  $3.3V \pm 5\%$ 

Stand-by:

Supply Current:

Oscillation: 15mA max (1.8432 to 39.9999 MHz)

10mA max (40 to 59.9999 MHz) 40mA max (60 to 79.9999 MHz) 55mA max (80 to 125 MHz) 0.01mA max (1.8432 to 125 MHz)

#### **Output (LVCMOS / LVTTL Compatible)**

Symmetry: 45/55% measured @ 50% V<sub>DD</sub> (-20 to +70°C)

45/55% measured @ 50% V<sub>DD</sub> (-40 to +85°C, up to 79.9999 MHz) 40/60% measured @ 50% V<sub>DD</sub> (-40 to +85°C, 80 to 125 MHz)

Rise & Fall Times: 7ns max (1.8432 to 39.9999 MHz)

5ns max (40 to 79.9999 MHz)

3ns max (80 to 125 MHz)

Logic 0: 10% V<sub>DD</sub> max Logic 1: 90% V<sub>DD</sub> min

Load: 15pF max or 10LSTTL

Jitter (1.8432 to 80 MHz): 5ps RMS ( $1\Sigma$ ) max, accumlated in 20,0000 adjacent periods

1.5ps RMS ( $\overline{1}\Sigma$ ) max phase jitter computed in 10 kHz-20 MHz freq. band 50ps peak-to-peak max total jitter, sampled in 100,000 random periods

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Jitter (80 to 125 MHz): 3ps RMS ( $1\Sigma$ ) max, accumlated in 20,0000 adjacent periods

1ps RMS ( $1\sum$ ) max phase jitter computed in  $10 \text{ kHz} \sim 20 \text{ MHz}$  freq. band 30ps peak-to-peak max total jitter, sampled in 100,000 random periods

**Standby Function (pad 1):** 

Oscillation:  $V_{IN} \ge 2.2V$  or open

Stand-by:  $V_{IN} \le 0.8V$  (output is high impedance)

Oscillation Output Delay: 10ms max Standby Output Delay: 0.1 $\mu$ s max Internal Pullup Resistance: 50K $\Omega$  min

Mechanical:

Shock: MIL-STD-883, Method 2002, Condition B

Solvent Resistance: MIL-STD-883, Method 2003 MIL-STD-202, Method 215

Terminal Strength: MIL-STD-883, Method 2004, Condition D Gross Leak: MIL-STD-883, Method 1014, Condition C

Fine Leak: MIL-STD-883, Method 1014, Condition A2 ( $R_I = 2x10^{-8}$  atm cc/s)

**Environmental:** 

Thermal Shock: MIL-STD-883, Method 1011, Condition A

Moisture Resistance: MIL-STD-883, Method 1004

Vibration: MIL-STD-883, Method 2007, Condition A
Resitance to Soldering Heat: MIL-STD-202, Method 210, Condition I or J

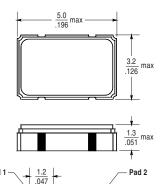


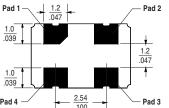
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#### **Package Details**

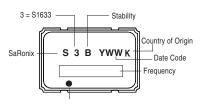




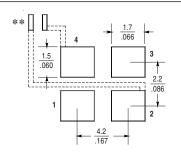
Pad Functions:

Pad 1: En/Disable (Standby) Pad 3: Output Pad 2: GND Pad 4: VDD

Marking Format (exact location of items may vary)



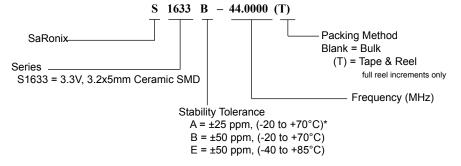
#### **Recommended Land Pattern**



\*\*External high frequency power supply decoupling required.

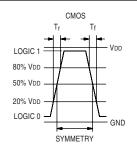
Scale: None (Dimensions in  $\frac{mm}{inches}$ 

#### Part Numbering Guide

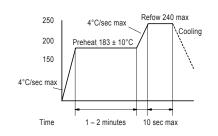


\*(Confirm availability by frequency)

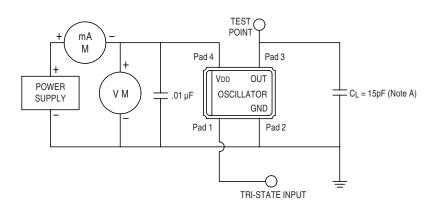
#### **Output Waveform**



#### **Solder Reflow Guide**



#### **Test Circuit**



Note A:  $C_L$  includes probe and jig capacitance.

\*All specfications subject to changes without notice