



Actual Size = 7 x 5mm



Product Features

- 5V CMOS/TTL compatible logic levels
- Pin-compatible with standard 7x5mm packages
- Designed for standard reflow and washing techniques
- Output Tri-state function
- Pb-free and RoHS/Green compliant (seam seal package only)

Product Description

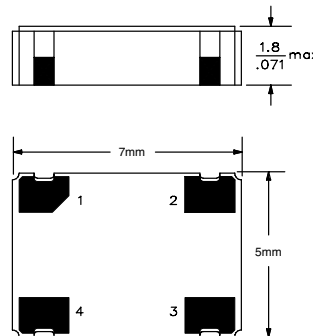
The S1700 and S1750 are 5V crystal clock oscillators. The output clock signal is compatible with CMOS/TTL logic levels. The device, available on tape and reel, is contained in a 7x5mm surface-mount ceramic package.

Applications

The S1700 and S1750 are an ideal reference clock for SMT applications requiring 5V CMOS & TTL logic levels

- PCs, notebooks, palmtop computers
- Portable applications
- PCMCIA cards and HDD

Packaging Outline



Pin Functions

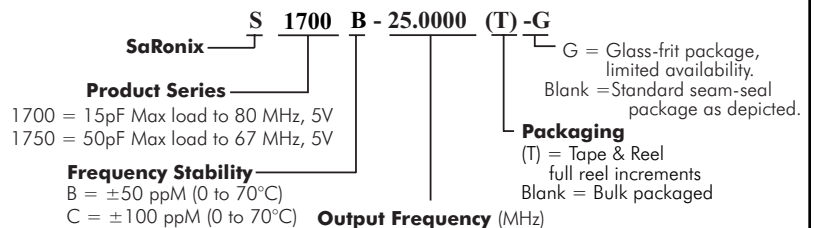
| Pin | Function |
|-----|-----------------|
| 1 | OE Function |
| 2 | Ground |
| 3 | Clock Output |
| 4 | V _{DD} |

Common Frequencies

Contact SaRonix for additional frequencies

| | | |
|-------------|-------------|-------------|
| 3.6864 MHz | 22.0000 MHz | 40.0000 MHz |
| 8.0000 MHz | 24.5760 MHz | 48.0000 MHz |
| 10.0000 MHz | 25.0000 MHz | 50.0000 MHz |
| 14.3181 MHz | 32.0000 MHz | 60.0000 MHz |
| 16.0000 MHz | 32.7680 MHz | 66.0000 MHz |
| 18.4320 MHz | 33.0000 MHz | 66.6667 MHz |
| 20.0000 MHz | 35.3280 MHz | 75.0000 MHz |

Ordering Information



*Note: Legacy glass frit package may continue to ship until inventory is depleted. See S1615 series to guarantee seam seal package.

Electrical Performance

| Parameter | Min. | Typ. | Max. | Units | Notes |
|--|---------------------|------|---------------------|-------|---------------------------------------|
| Output frequency | 1.8432 | | 80 | MHz | S1750 Max Frequency 67 MHz |
| Supply voltage | +4.5 | +5.0 | +5.5 | V DC | |
| Supply current, output enabled 1700 | | | 15 | mA | 1.8 to 35 MHz |
| | | | 30 | | >35 to 66.0 MHz |
| | | | 50 | | >66 to 80.0 MHz |
| Supply current, output enabled 1750 | | | 20 | mA | 1.8 to 20 MHz |
| | | | 35 | | >20 to 50 MHz |
| | | | 60 | | >50 to 67.0 MHz |
| Frequency stability | | | ±50 to ±100 | ppM | See Note 1 below |
| Operating temperature | 0 | | +70 | °C | |
| Output logic 0, VOL | | | 10% V _{DD} | V | HCMOS |
| | | | 0.5 | V | TTL, S1750 only |
| Output logic 1, VOH | 90% V _{DD} | | | V | HCMOS |
| | 2.5 | | | V | TTL, S1750 only |
| Output load | | | 15 | pF | S1700 |
| | | | 50 | pF | S1750 |
| | | | 5 | TTL | TTL, S1750 only |
| Duty cycle | CMOS | 45 | 55 | % | 0 to 70°C measured 50%V _{DD} |
| | TTL | 40 | 60 | % | 0 to 70°C measured 1.5V, S1750 only |
| Rise and fall time | CMOS | | 10 | ns | measured 20/80% of waveform |
| | TTL | | 5 | ns | measured 0.5V to 2.5V, S1750 only |

Note:
 1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

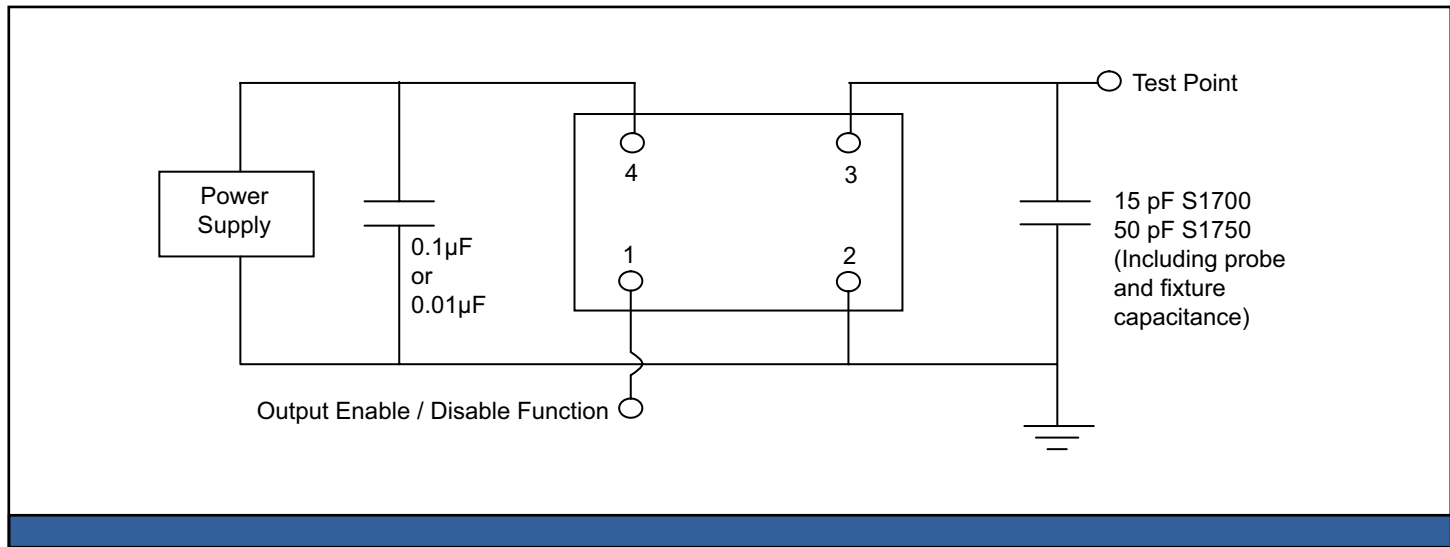
Output Enable / Disable Function

| Parameter | Min. | Typ. | Max. | Units | Notes |
|---|---------------------|------|---------------------|-------|----------------|
| Input Voltage (pin 1), Output Enable (HCMOS) | 90% V _{DD} | | | V | or open |
| Input voltage (pin 1), Output Disable (HCMOS) | | | 10% V _{DD} | V | Output is Hi-Z |
| Input voltage (pin 1), Output Enable (TTL) | 2.2 | | | V | or open |
| Input voltage (pin 1), Output Disable (TTL) | | | 0.8 | V | Output is Hi-Z |
| Internal pullup resistance | 50 | | | kΩ | |
| Output disable delay | | | 100 | ns | |
| Output enable delay | | | 100 | ns | |

Absolute Maximum Ratings

| Parameter | Min. | Typ. | Max. | Units | Notes |
|---------------------|------|------|------|-------|-------|
| Storage temperature | -55 | | +125 | °C | |

Test Circuit

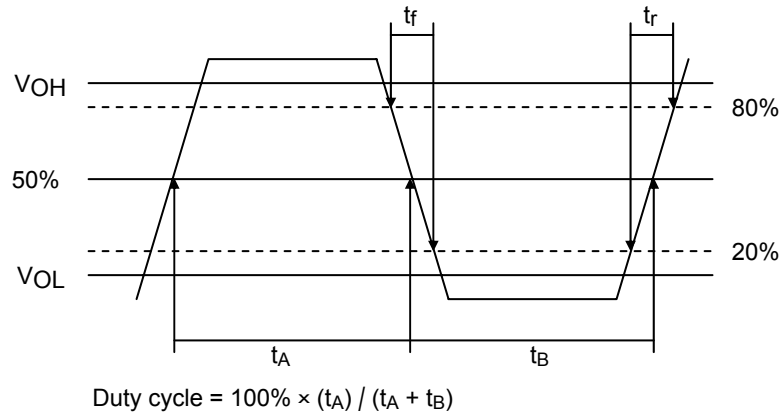


Reliability Test Ratings

This product is rated to meet the following test conditions (Applies to seam-seal package only):

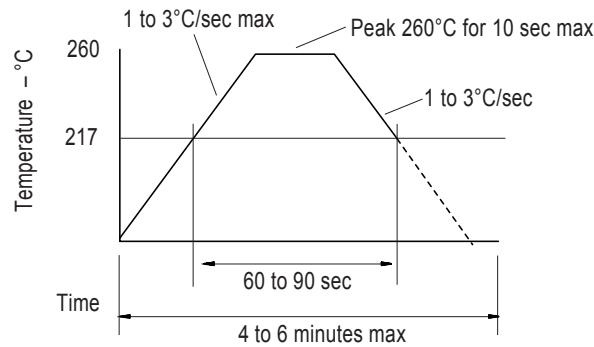
| Type | Parameter | Test Condition |
|---------------|------------------------------|---|
| Mechanical | Shock | MIL-STD-883, Method 2002, Condition B |
| Mechanical | Solderability | JESD22-B102-D Method 2 (Preconditioning E) |
| Mechanical | Terminal strength | MIL-STD-883, Method 2004, Condition D |
| Mechanical | Gross leak | MIL-STD-883, Method 1014, Condition C |
| Mechanical | Fine leak | MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2 \times 10^{-8}$ atm cc/s) |
| Mechanical | Solvent resistance | MIL-STD-202, Method 215 |
| Environmental | Thermal shock | MIL-STD-883, Method 1011, Condition A |
| Environmental | Moisture resistance | MIL-STD-883, Method 1004 |
| Environmental | Vibration | MIL-STD-883, Method 2007, Condition A |
| Environmental | Resistance to soldering heat | J-STD-020C Table 5-2 Pb-free devices (2 cycles max) |

Output Waveform

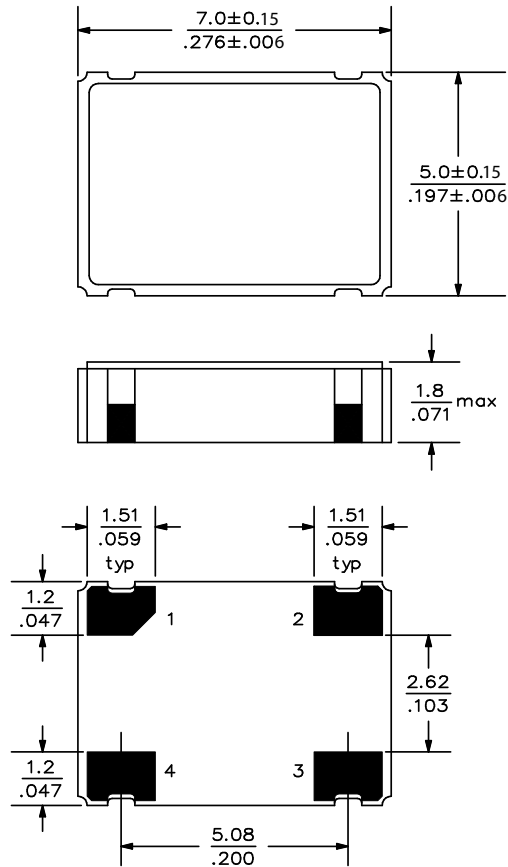


Reflow Soldering Profile (Applies to seam-seal package only)

As per IPC/JEDEC J-STD-020C

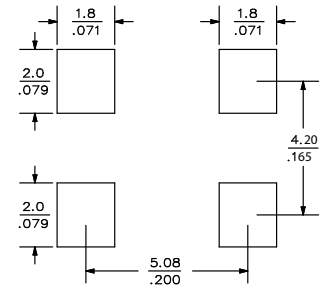


Mechanical Drawings



Note: Seam-seal package is depicted. Legacy glass-frit package has limited availability, please inquire if needed.

Recommended Land Pattern*



*External high-frequency power decoupling is recommended. (see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1: S XX YY WW X (SaRonix, Model, Stability, Year, Week, Origin)
Marking LINE 2: • Frequency (Pin #1, Frequency code)

Note: S2YYYYWWX S1700
S7YYYYWWX S1750

**Exact location of markings may vary.