

Model CB3 & CB3LV

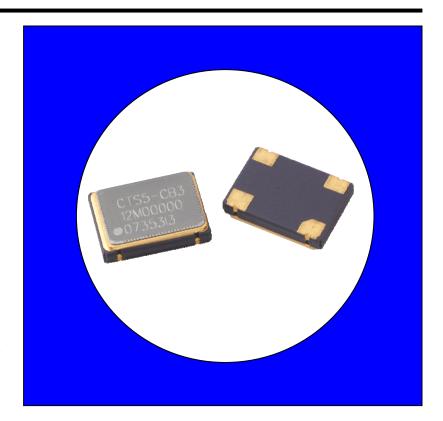
HCMOS/TTL CLOCK OSCILLATOR

FEATURES

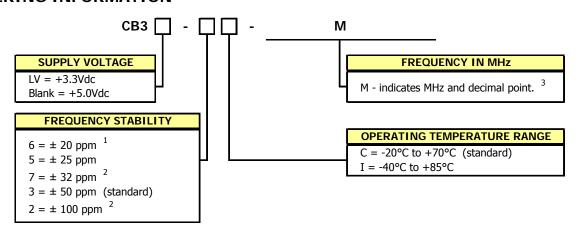
- Standard 7.0x5.0mm Surface Mount Footprint
- HCMOS/TTL Compatible
- Fundamental and 3RD Overtone Crystals
- Frequency Range 1.5 160 MHz
- Frequency Stability, ±50 ppm Standard $(\pm 25 \text{ ppm and } \pm 20 \text{ ppm available})$
- +3.3Vdc or +5.0Vdc Operation
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging
- RoHS/Green Compliant (6/6)

DESCRIPTION

The CB3/CB3LV is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.



ORDERING INFORMATION



- 1] 6I Stability/Temperature combination is not available.
- 2] These stabilities are not recommended for new designs.
- 3] Frequency is recorded with only leading significant digits before the 'M' and 4 6 significant digits after the 'M' (including zeros). [Ex. XMXXXXXX (3M579545), XXMXXXXX (14M31818), XXXMXXXX (125M0000)]
- 4] CTS Distributors may add a -T or -1 at the end of the part number to indicate Tape and Reel packaging.

Not all performance combinations and frequencies may be available. Contact your local CTS Representative or CTS Customer Service for availability.

Example Part Number: CB3LV-3C-32M7680 or CB3-3I-32M7680

Document No. 008-0256-0 Page 1 - 4 Rev. F



ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
	Storage Temperature	T_{STG}	-	-55	1	125	°C
	Frequency Range						
	CB3	f_{O}	-	1.5	-	107	MHz
	CB3LV		-	1.5	-	160	
	Frequency Stability	$\Delta f/f_O$	See Note 1 and Ordering Information	-	-	20, 25 or 50	± ppm
	Aging	Δf	First year	-	3	5	± ppm
psq	Operating Temperature						1.1
4	Commercial	T_A	-	-20	25	70	°C
	Industrial			-40	23	85	
	Supply Voltage	W	± 10 %	4.5	г о		V
	CB3 CB3LV			4.5 3.0	5.0 3.3	5.5 3.6	V
			Frequency Range, rested load condition noted	5.0	٥.5	3.0	
	Supply Current		for typical values.				· mA
	CB3		1.5 MHz to 20 MHz C_L =50pF	-	10	25	
		.	20.1 MHz to 80 MHz C_L =50pF	-	30	50	
		I_{CC}	80.1 MHz to 107 MHz $C_L=15pF$	-	40	80	
	CB3LV		1.5 MHz to 20 MHz $C_L=15pF$	-	7	12	
			20.1 MHz to 80 MHz $C_L=15pF$	-	20	40	
			80.1 MHz to 160 MHz C_L =15pF	-	30	60	
	Output Load		1.5 MHz to 50 MHz	-	-	50	
		C_L	50.1 MHz to 80 MHz	-	-	30	pF
SIS			80.1 MHz to 160 MHz	-	-	15	
ete	Output Voltage Levels Logic '1' Level		CMOC L d	0.9*V _{CC}			
am	Logic 1 Level	V_{OH}	CMOS Load 10 TTL LOAD	V _{CC} -0.6V	-	-	
Jar				v _{CC} -0.0v		0.1*V _{CC}	V
Ε	Logic '0' Level	V_{OL}	CMOS TTL Load	-	-	0.1 · V _{CC}	
for	Output Current		Load			0.7	
ave	Logic '1' Level	I_{OH}	$V_{OH} = 3.9V/2.2V$ $V_{CC} = 4.5V/3.0V$	-	-	-16/-8	
Ŋ	Logic '0' Level	I _{OL}	$V_{OL} = 0.4V$ $V_{CC} = 4.5V/3.0V$	-	-	+16/+8	mA
Electrical and Waveform Parameters	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
al a	Rise and Fall Time		@ 10% - 90% Levels, Tested load condition				
rica			noted for typical values.			40	
ect	CB3		1.5 MHz to 20 MHz	-	8	10	
Ĕ		T_R , T_F	20.1 MHz to 80 MHz	-	5 2.5	8 5	
	CDOLV	K/ I	80.1 MHz to 160 MHz C _L =15pF			_	ns
	CB3LV		1.5 MHz to 20 MHz	-	6	8	
			20.1 MHz to 80 MHz	_	3 1.5	5 3	
			80.1 MHz to 160 MHz C _L =15pF				
	Start Up Time	T _S	Application of V _{CC}	-	-	10	ms
	Enable Function Enable Input Voltage	V_{IH}	Din 1 Logic '1' Output Enabled	2.0			V
			Pin 1 Logic '1', Output Enabled Pin 1 Logic '0', Output Disabled	2.0	-	- 0.0	v
	Disable Input Voltage	V _{IL}	Pin 1 Logic '0', Output Disabled Pin 1 Logic '1'		-	0.8	ms
	Enable Time	T _{PLZ}	Pin 1 Logic 1 Pin 1 Logic '0', Output Disabled	-	-	10	ms
	Standby Current Period Jitter, Pk-Pk	I _{ST}	Fili 1 Logic 0 , Output Disabled	-	-	10 50	μA
	Period Jitter, PK-PK Period Jitter, RMS	-	<u>-</u>	-	-	50	ps
	Phase Jitter, RMS	-	Bandwidth 12 kHz - 20 MHz	_	-	1	ρS
	Notes:		Panaman IE NIE ZO FILE			1	

Notes:

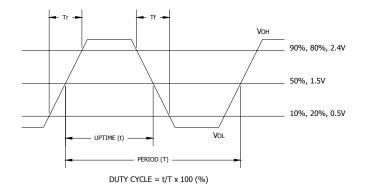
<u>Document No. 008-0256-0</u> Page 2 - 4 Rev. F

^{1.} Inclusive of calibration @ 25°C, operating temperature range, supply voltage variation, load variation, and first year aging.



Model CB3 & CB3LV 7.0x5.0mm Low Cost HCMOS/TTL Clock Oscillator

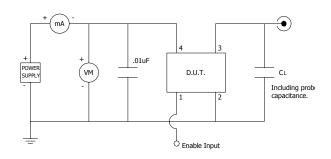
CMOS/TTL OUTPUT WAVEFORM



ENABLE TRUTH TABLE

PIN 1	PIN 3			
Logic '1'	Output			
Open	Output			
Logic '0'	High Imp.			

TEST CIRCUIT, CMOS LOAD

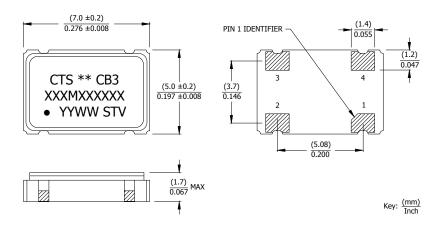


D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V_{CC}	Supply Voltage

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



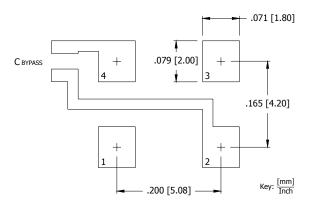
MARKING INFORMATION

- 1. ** Manufacturing Site Code.
 [Note a dash may follow the site code and is acceptable.]
- XXXMXXXXXX Frequency is marked with only leading significant digits before the 'M' and 4 - 6 digits after the 'M' (including zeros).
 Ex. XMXXXXXX (3M579545) XXMXXXXX (14M31818) XXXMXXXXX (125M0000)
- 3. YYWW Date code, YY year, WW week.
- 4. ST Frequency stability/temperature code. (Refer to Ordering Information.)
- 5. V Voltage code. 3 = 3.3V, 5 = 5.0V.

NOTES

- 1. Termination pads (e4). Barrier-plating is nickel (Ni) with gold (Au) flash plate.
- 2. Reflow conditions per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY

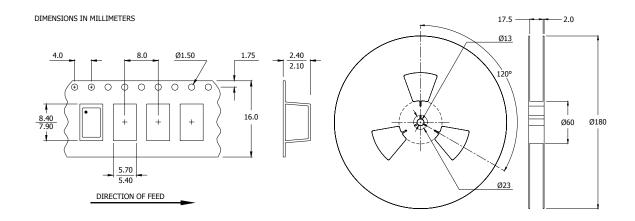


 C_{RYPASS} should be \geq 0.01 uF.



TAPE AND REEL INFORMATION

Standard packaging is tape and reel for this product family. Device quantity is 1,000 pieces per 180mm reel.



ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle: 400 cycles from -55°C to +125°C, 10 minute dwell at each temperature, 1

minute transfer time between temperatures.

Mechanical Shock: 1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3

mutually perpendicular planes (18 total shocks).

Sinusoidal Vibration: 0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles

each in 3 mutually perpendicular planes (9 times total).

Gross Leak: No leak shall appear while immersed in an FC40 or equivalent liquid at

+125°C for 20 seconds.

Fine Leak: Mass spectrometer leak rates less than 2x10⁻⁸ ATM cc/sec air equivalent.

Resistance to Solder Heat: Product must survive 3 reflows of +260°C peak, 10 seconds maximum.

High Temperature Operating Bias: 2,000 hours at +125°C, maximum bias, disregarding frequency shift.

Frequency Aging: 1,000 hours at $+85^{\circ}$ C, full bias, less than ± 5 ppm shift.

Moisture Sensitivity Level: Level 1 per JEDEC J-STD-020.