

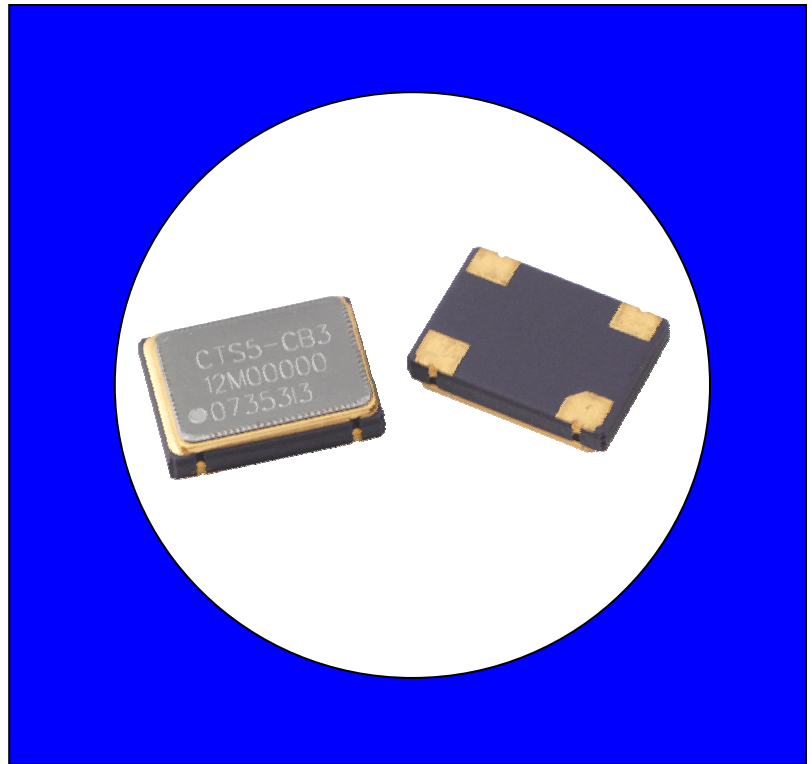


### FEATURES

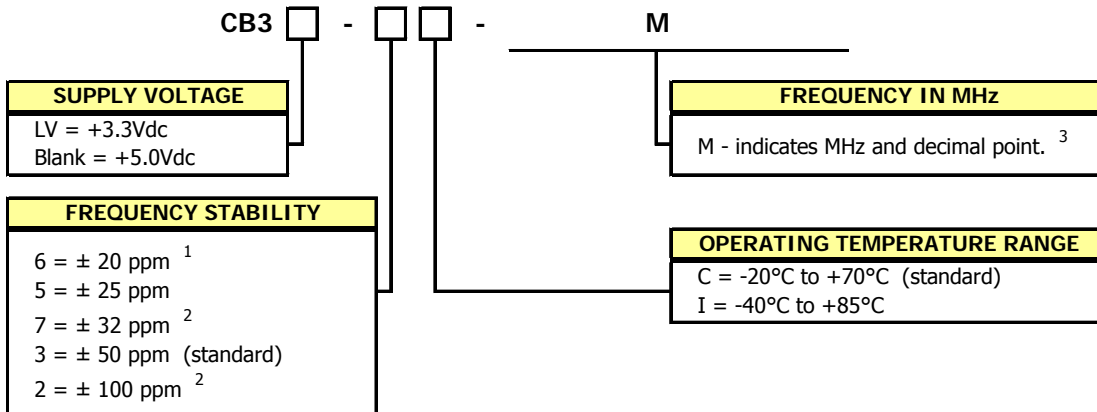
- Standard 7.0x5.0mm Surface Mount Footprint
- HCMOS/TTL Compatible
- **Fundamental and 3<sup>RD</sup> Overtone Crystals**
- Frequency Range 1.5 – 160 MHz
- Frequency Stability,  $\pm 50$  ppm Standard ( $\pm 25$  ppm and  $\pm 20$  ppm available)
- +3.3Vdc or +5.0Vdc Operation
- Operating Temperature to  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Output Enable Standard
- Tape & Reel Packaging
- **RoHS/Green Compliant (6/6)**

### DESCRIPTION

The CB3/CB3LV is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.



### ORDERING INFORMATION



- 1] 6I Stability/Temperature combination is not available.
- 2] These stabilities are not recommended for new designs.
- 3] Frequency is recorded with only leading significant digits before the 'M' and 4 - 6 significant digits after the 'M' (including zeros).  
[Ex. XMXXXXXX (3M579545), XXMXXXXX (14M31818), XXXMXXXX (125M0000)]
- 4] CTS Distributors may add a -T or -I at the end of the part number to indicate Tape and Reel packaging.

**Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.**

Example Part Number: CB3LV-3C-32M7680 or CB3-3I-32M7680

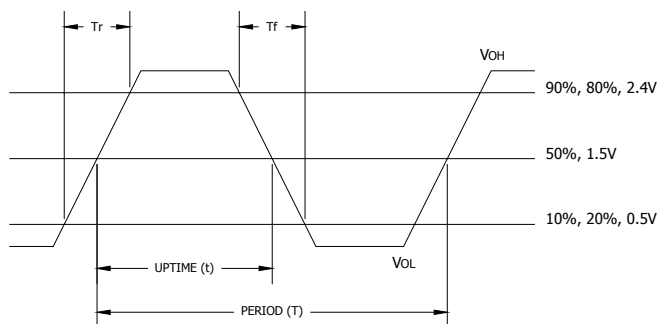
## ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
<b>Absolute Maximums</b>	Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	7.0	V	
	Storage Temperature	$T_{STG}$	-	-55	-	125	°C	
	Frequency Range	$f_0$	-	1.5	-	107	MHz	
	CB3LV		-	1.5	-	160		
	Frequency Stability	$\Delta f/f_0$	See Note 1 and Ordering Information	-	-	20, 25 or 50	± ppm	
	Aging	$\Delta f$	First year	-	3	5	± ppm	
	Operating Temperature	$T_A$	-	-20	25	70	°C	
Commercial Industrial	-		-40	-	85			
<b>Electrical and Waveform Parameters</b>	Supply Voltage	$V_{CC}$	± 10 %	4.5	5.0	5.5	V	
	CB3LV			3.0	3.3	3.6		
	Supply Current	$I_{CC}$	Frequency Range, tested load condition noted for typical values.		-	10	25	mA
	CB3		1.5 MHz to 20 MHz	$C_L=50pF$	-	30	50	
			20.1 MHz to 80 MHz	$C_L=50pF$	-	40	80	
			80.1 MHz to 107 MHz	$C_L=15pF$	-	7	12	
	CB3LV		1.5 MHz to 20 MHz	$C_L=15pF$	-	20	40	
			20.1 MHz to 80 MHz	$C_L=15pF$	-	30	60	
		80.1 MHz to 160 MHz	$C_L=15pF$	-	-	-		
	Output Load	$C_L$	1.5 MHz to 50 MHz	-	-	50	pF	
	50.1 MHz to 80 MHz		-	-	30			
	80.1 MHz to 160 MHz		-	-	15			
	Output Voltage Levels	$V_{OH}$	CMOS Load	10	$0.9*V_{CC}$	-	-	V
	Logic '1' Level		TTL LOAD		$V_{CC}-0.6V$	-	-	
	Logic '0' Level	$V_{OL}$	CMOS Load	TTL	-	-	$0.1*V_{CC}$	0.4
	Output Current	$I_{OH}$	$V_{OH} = 3.9V/2.2V$	$V_{CC} = 4.5V/3.0V$	-	-	-16/-8	mA
	Logic '0' Level		$I_{OL}$	$V_{OL} = 0.4V$	$V_{CC} = 4.5V/3.0V$	-	-	
Output Duty Cycle	SYM	@ 50% Level		45	-	55	%	
Rise and Fall Time	$T_{Rv} T_F$	@ 10% - 90% Levels, Tested load condition noted for typical values.		-	8	10	ns	
CB3		1.5 MHz to 20 MHz	$C_L=50pF$	-	5	8		
		20.1 MHz to 80 MHz	$C_L=50pF$	-	2.5	5		
		80.1 MHz to 160 MHz	$C_L=15pF$	-	6	8		
CB3LV		1.5 MHz to 20 MHz	$C_L=15pF$	-	3	5		
		20.1 MHz to 80 MHz	$C_L=15pF$	-	1.5	3		
	80.1 MHz to 160 MHz	$C_L=15pF$	-	-	-			
Start Up Time	$T_S$	Application of $V_{CC}$	-	-	10	ms		
Enable Function	$V_{IH}$	Pin 1 Logic '1', Output Enabled	2.0	-	-	V		
Enable Input Voltage		Pin 1 Logic '0', Output Disabled	-	-	0.8			
Disable Input Voltage	$V_{IL}$	Pin 1 Logic '1'	-	-	10	ms		
Standby Current	$I_{ST}$	Pin 1 Logic '0', Output Disabled	-	-	10	µA		
Period Jitter, Pk-Pk	-	-	-	-	50	ps		
Period Jitter, RMS	-	-	-	-	5	ps		
Phase Jitter, RMS	-	Bandwidth 12 kHz - 20 MHz	-	-	1	ps		

Notes:

1. Inclusive of calibration @ 25°C, operating temperature range, supply voltage variation, load variation, and first year aging.

**CMOS/TTL OUTPUT WAVEFORM**

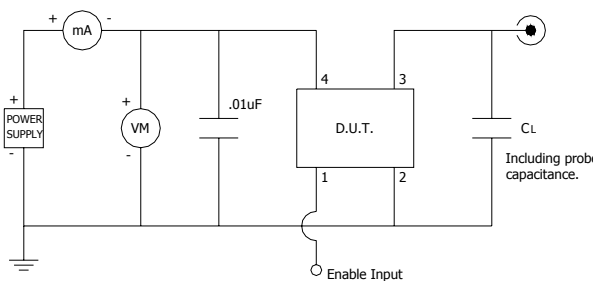


DUTY CYCLE =  $t/T \times 100$  (%)

**ENABLE TRUTH TABLE**

PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

**TEST CIRCUIT, CMOS LOAD**

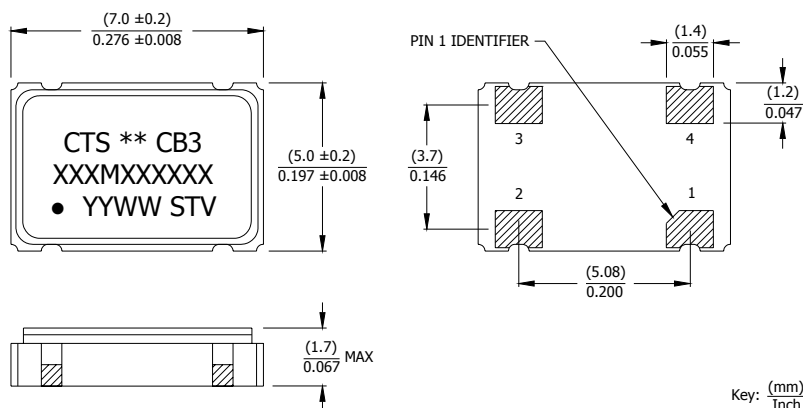


**D.U.T. PIN ASSIGNMENTS**

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V <sub>CC</sub>	Supply Voltage

**MECHANICAL SPECIFICATIONS**

**PACKAGE DRAWING**



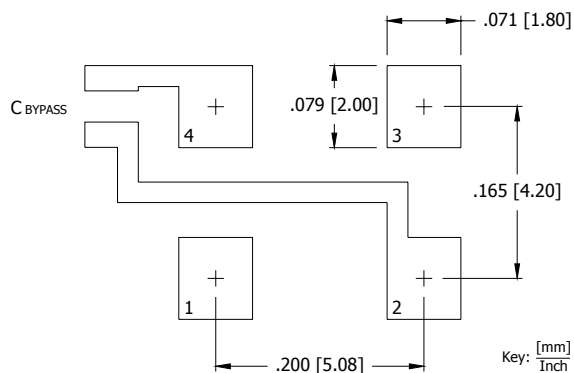
**MARKING INFORMATION**

- \*\* – Manufacturing Site Code.  
[Note a dash may follow the site code and is acceptable.]
- XXXXMXXXXXX – Frequency is marked with only leading significant digits before the 'M' and 4 - 6 digits after the 'M' (including zeros).  
Ex. XMXXXXXX (3M579545)  
XXMXXXXXX (14M31818)  
XXXMXXXX (125M0000)
- YYWW – Date code, YY – year, WW – week.
- ST – Frequency stability/temperature code. (Refer to Ordering Information.)
- V – Voltage code. 3 = 3.3V, 5 = 5.0V.

**NOTES**

- Termination pads (e4). Barrier-plating is nickel (Ni) with gold (Au) flash plate.
- Reflow conditions per JEDEC J-STD-020.

**SUGGESTED SOLDER PAD GEOMETRY**



C<sub>BYPASS</sub> should be ≥ 0.01 uF.

