

Model CB3 & CB3LV

HCMOS/TTL CLOCK OSCILLATOR



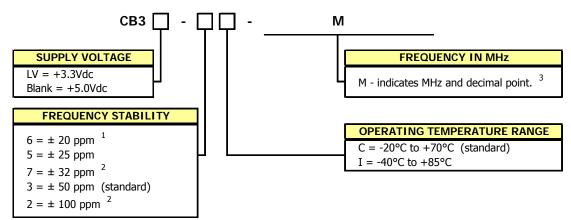
FEATURES

- Standard 7.0x5.0mm Surface Mount Footprint
- HCMOS/TTL Compatible
- Fundamental and 3RD Overtone Crystals
- Frequency Range 1.5 160 MHz
- Frequency Stability, ±50 ppm Standard (±25 ppm and ±20 ppm available)
- +3.3Vdc or +5.0Vdc Operation
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging
- RoHS/Green Compliant (6/6)

DESCRIPTION

The CB3/CB3LV is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.

ORDERING INFORMATION



1] 6I Stability/Temperature combination is not available.

2] These stabilities are not recommended for new designs.

3] Frequency is recorded with only leading significant digits before the 'M' and 4 - 6 significant digits after the 'M' (including zeros). [Ex. XMXXXXXX (3M579545), XXMXXXXX (14M31818), XXXMXXXX (125M0000)]

4] CTS Distributors may add a -T or -1 at the end of the part number to indicate Tape and Reel packaging.

Not all performance combinations and frequencies may be available. Contact your local CTS Representative or CTS Customer Service for availability.

Example Part Number: CB3LV-3C-32M7680 or CB3-3I-32M7680

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 • • • CTS Electronic Components, Inc. • 171 Covington Drive • Bloomingdale, IL 60108 • • •
 • • • www.ctscorp.com • • •



ELECTRICAL CHARACTERISTICS

Baseline Waximum Supply Voltage V _{CC} - - - 7.0 V Storage Temperature T _{STG} - - - 1.5 - 125 °C Frequency Range f ₀ . 1.5 - 107 MHz CB3 Afr First year - 3 5 # ppm Operating Temperature T _A - - - 3 5 # ppm Operating Temperature T _A - - - 3 5 # ppm Operating Temperature T _A - - - 3 5 # ppm Commercial T _A - - - 3 3.6 V CB3 Voc *10 % 4.5 5.0 5.5 V CB3 1.5 MHz to 20 MHz C_=50pF - 10 25 - 20.1 MHz to 80 MHz - - 50 60 - -		PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Frequency Range 0.0 . 1.5 . 107 MHz GBJLV 6 - 1.5 - 107 160 MHz GBJLV Δff Frequency Stability Δff First year - 3 5 ± ppm Operating Temperature Commercial TA - - 20 25 70 °C CB3LV Crammercial TA - - - 3 5 ± ppm Operating Temperature TA - - - - 0 25 70 °C CB3 Vcc ± 10 % 4.5 5.0 5.5 V 25 70 °C 6 3.3 3.6 V 25 70 °C 6 3.0 3.3 3.6 V 25 70 °C 6 3.0 3.3 3.6 V 10 25 20.1 Mtz to 20 MHz C= 50 10 10		Maximum Supply Voltage	V _{CC}	-	-0.5	-	7.0	V	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	S	Storage Temperature	T _{STG}	-	-55	-	125	°C	
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$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	cim		f _o	-				MHz	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	١a	CB3LV		-	1.5	-			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	tel	Frequency Stability	∆f/f _o	See Note 1 and Ordering Information	-	-		± ppm	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	lut	Aging	٨f	First vear	-	3		± nnm	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	psq							_ ppm	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	A			-	-20	25	70	°C	
CB3 CB3 VCC 4.5 5.0 5.5 V Supply Current Frequency Range, rester road condition noted for typical values. 3.0 3.3 3.6 3.6 CB3 Log Log Supply Current 1.5 MHz to 20 MHz C_=50pF - 10 25 CB3 Log NHz to 20 MHz C_=50pF - 40 80 CB3LV Log 80.1 MHz to 107 MHz C_=15pF - 7 12 mA CB3LV Log NHz to 20 MHz C_=15pF - 7 12 mA CB3LV Log Thz to 80 MHz C_=15pF - 7 12 mA Output Load Logic '1' Level Vort S0.1 MHz to 80 MHz - - 15 MA Output Voltage Levels Vort CMOS TTL - - 0.1*Vcc - - - 15 Output Voltage Levels Logic '1' Level Vort GMOS TTL -					-40	ZJ	85		
CB3LV requency karge, rester had condition noted for typical values. 3.0 3.3 3.6 Supply Current I.S MHZ to 20 MHZ C ₄ =50pF - 10 25 CB3 Lcc Supply Current - 10 25 CB3 Lcc MHZ to 20 MHZ C ₄ =15pF - 7 12 CB3 Logic MHZ to 80 MHZ C ₄ =15pF - 7 12 mA Output Load C 1.5 MHZ to 160 MHZ - - 50 mA Logic T' Level VoH CMOS Load 10 0.9*Vcc - - - - Logic T' Level Logi VoH S0.1 MHZ to 160 MHZ - - - - - - - - - -			N/	± 10 %					
Supply Current Prequency karage, rescent out control on noced - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -			V _{CC}					V	
CB3 I.S. MHz to 20 MHz C = 50pF - 10 25 CB3 J.Cc S0.1 MHz to 20 MHz C = 50pF - 30 50 CB3LV I.S. MHz to 20 MHz C = 15pF - 40 80 CB3LV I.S. MHz to 20 MHz C = 15pF - 7 12 Output Load I.S. MHz to 30 MHz C = 15pF - 20 40 Output Load I.S. MHz to 30 MHz C = 15pF - 20 40 Output Voltage Levels I.S. MHz to 80 MHz - - - 50 Logic '0' Level VoH CMOS Load 10 0.9*VcC - - - 0.4 Output Current Logic '0' Level VoH CMOS Load 10 0.9*VcC - - +16/-8 mA Logic '0' Level Iot VoL Load 10 0.9*VcC - - +16/-8 mA Logic '0' Level Iot VoL Load 10 NoL				Frequency Range, Tested load condition noted	5.0	5.5	3.0		
CB3LV 20.1 MHz to 80 MHz C _L =50pF - 30 50 40 80 CB3LV 1.5 MHz to 20 MHz C _L =15pF - 7 12 40 80 Output Load 1.5 MHz to 80 MHz C _L =15pF - 7 12 40 80 Output Load 1.5 MHz to 80 MHz C _L =15pF - 7 12 40 Output Load 1.5 MHz to 50 MHz - - 50 9 Output Voltage Levels 50.1 MHz to 160 MHz - - 15 9 Logic '1' Level V _{OH} CMOS Load 10 0.9*V _{CC} - - Logic '0' Level V _{OH} CMOS Load TTL - - 0.1*V _{CC} - Logic '0' Level V _{OH} CMOS Load TUL - - - - - - - - - - - - - - - - - - - - -		Supply Current		for typical values.					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		CB3		1.5 MHz to 20 MHz $C_L=50pF$	-	10	25		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $				20.1 MHz to 80 MHz $C_L=50pF$	-				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			L _{CC}	80.1 MHz to 107 MHz C _L =15pF	-	40	80	m۸	
Bol 1 MHz to 160 MHz C _L =15pr - 30 60 Output Load 1.5 MHz to 50 MHz - - 50 pF Output Voltage Levels 50.1 MHz to 60 MHz - - 30 pF Logic '1' Level V _{OH} CMOS Load 10 0.9*V _{CC} - - - V Output Voltage Levels Logic '1' Level V _{OH} CMOS Load 10 0.9*V _{CC} - - - - 0.1*V _{CC} V Output Current Logic '1' Level IOH V _{OL} = 0.4V V _{CC} = 4.5V/3.0V - - - - - 0.4 Output Current Logic '1' Level IOH V _{OL} = 0.4V V _{CC} = 4.5V/3.0V - - +16/-8 mA Output Duty Cycle SYM 0.50% Level 0.1 MHz to 20 MHz C _L =50pF - 8 10 CB3 T _{Rv} T _F 20.1 MHz to 80 MHz C _L =50pF - 5 8 1.5 Ms to 20 MHz C _L =15pF <td></td> <td>CB3LV</td> <td></td> <td>1.5 MHz to 20 MHz $C_L=15pF$</td> <td>-</td> <td>7</td> <td>12</td> <td>ШA</td>		CB3LV		1.5 MHz to 20 MHz $C_L=15pF$	-	7	12	ШA	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$				20.1 MHz to 80 MHz $C_L=15pF$	-				
Start Up Time Ts Application of Vcc - - - 30 pF Start Up Time Ts VoH CMOS Load 10 0.9 ⁴ Vcc - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -<				80.1 MHz to 160 MHz C _L =15pF	-	30	60		
See 80.1 MHz to 160 MHz - - 15 Output Voltage Levels Logic '1' Level VoH CMOS Load 10 0.9*Vcc Vcc*0.6V - - V Logic '1' Level VoL CMOS TTL - 0.1*Vcc Vcc*0.6V - - V Logic '1' Level Logic '1' Level Logic '1' Level Logic '1' Level - - 0.1*Vcc 0.4 - - 0.4 Output Current Logic '0' Level IoH VoH = 3.9V/2.2V Vcc = 4.5V/3.0V - - - - 16/-8 mA Output Duty Cycle SYM @ 50% Level 45 - 55 % Output Duty Cycle SYM @ 50% Level 45 - 55 % Rise and Fall Time Dot MHz C 0 MHz C = 50 pF - 8 10 - - - 1.5 MA CB3 T _{R'} T _F So 1 MHz to 160 MHz C = 150 F - 2.5 5 ns ns Start Up Time		Output Load			-	-			
Output Voltage Levels Logic '1' Level V_{OH} CMOS Load TTL LOAD 10 $0.9*V_{CC}$ $V_{CC}^{-0.6V}$ - - - V Logic '0' Level V_{OL} CMOS TTL - - 0.1*V _{CC} V Output Current Logic '0' Level I_{OH} V_{OL} V_{OL} - - - 0.4 Output Current Logic '0' Level I_{OH} V_{OL} V_{OL} - - - - - 0.4 Output Duty Cycle SYM 0.5 Level 45 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - <td< td=""><td></td><td></td><td>CL</td><td></td><td>-</td><td>-</td><td></td><td>pF</td></td<>			CL		-	-		pF	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	ŝrs			80.1 MHz to 160 MHz	-	-	15		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	iete			CMOS Load 10	0 0*1/				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	am		V _{OH}			-	-		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Par				V _{CC} 0.0V		0.1*\/	V	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	E	Logic '0' Level	V _{OL}		-	-			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	for	Output Current		2000			0.1		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	ave		I _{OH}	$V_{OH} = 3.9V/2.2V$ $V_{CC} = 4.5V/3.0V$	-	-	-16/-8		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Ň	Logic '0' Level			-	-	+16/+8	MA	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	pu			@ 50% Level	45	-		%	
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$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	ect	CB3			-				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Ĕ		T_{P}, T_{F}		_				
$ \begin{array}{ c c c c c c c } \hline & 20.1 \text{ MHz to } 80 \text{ MHz} & C_L = 15 \text{pF} & - & 3 & 5 \\ \hline & 80.1 \text{ MHz to } 160 \text{ MHz} & C_L = 15 \text{pF} & - & 1.5 & 3 \\ \hline & 1.5 & 3 & \\ \hline & 1.5 & 1.5 & 1.5 & \\ \hline & 1.5 & 1.5 & 1.5 & \\ \hline & 1.5 & 1.5 & 1.5 & \\ \hline & 1.5 & 1.5 & 1.5 & \\ \hline & 1.5 & 1.5 & 1.5 & \\ \hline & 1.5$		CB3LV					-	ns	
$ \begin{array}{ c c c c c c c c } \hline & & & & & & & & & & & & & & & & & & $		CB3LV			-				
Start Up TimeTsApplication of V _{CC} 10msEnable Function </td <td></td> <td></td> <td></td> <td></td> <td>_</td> <td></td> <td></td> <td></td>					_				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		Chart Lin Time -	т	E 1			-		
$ \begin{array}{ c c c c c c } \hline Enable Input Voltage & V_{IH} & Pin 1 Logic '1', Output Enabled & 2.0 & - & - & V \\ \hline Disable Input Voltage & V_{IL} & Pin 1 Logic '0', Output Disabled & - & 0.8 \\ \hline Enable Time & T_{PLZ} & Pin 1 Logic '1' & - & 10 & ms \\ \hline Standby Current & I_{ST} & Pin 1 Logic '0', Output Disabled & - & - & 10 & \muA \\ \hline Period Jitter, Pk-Pk & - & - & - & 50 \\ \hline Period Jitter, RMS & - & - & - & 5 & ps \\ \hline \end{array} $			IS		-	-	10	ms	
Disable Input Voltage V _{IL} Pin 1 Logic '0', Output Disabled - - 0.8 Enable Time T _{PLZ} Pin 1 Logic '1' - - 10 ms Standby Current I _{ST} Pin 1 Logic '0', Output Disabled - - 10 μA Period Jitter, Pk-Pk - - - 50 ps Period Jitter, RMS - - - 50 ps			V	Pin 1 Logic '1' Output Enabled	20	_	_	V	
Enable Time T _{PLZ} Pin 1 Logic '1' - - 10 ms Standby Current I _{ST} Pin 1 Logic '0', Output Disabled - - 10 μA Period Jitter, Pk-Pk - - - 50 ps Period Jitter, RMS - - - 5 ps					2.0		0.8	v	
Standby Current I Pin 1 Logic '0', Output Disabled - 10 μA Period Jitter, Pk-Pk - - 50 - 50 ps Period Jitter, RMS - - - 50 ps		· · ·						me	
Period Jitter, Pk-Pk - - 50 Period Jitter, RMS - - 5 ps				-		_			
Period Jitter, RMS 5 ps			1	-	_	_		μΑ	
				<u>-</u>	-	-		ps	
		Phase Jitter, RMS	-	Bandwidth 12 kHz - 20 MHz	-	-	1		

Notes:

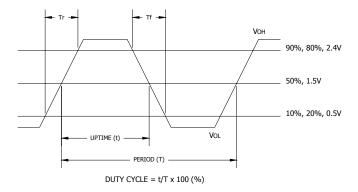
1. Inclusive of calibration @ 25°C, operating temperature range, supply voltage variation, load variation, and first year aging.

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Model CB3 & CB3LV 7.0x5.0mm Low Cost **HCMOS/TTL Clock Oscillator**

CMOS/TTL OUTPUT WAVEFORM

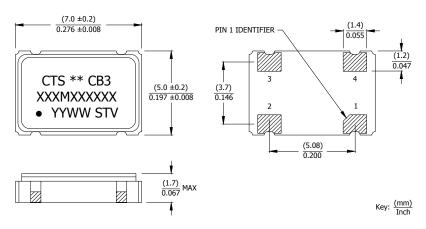


ENABLE TRUTH TABLE

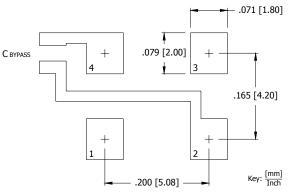
PIN 1	PIN 3		
Logic `1'	Output		
Open	Output		
Logic '0'	High Imp.		

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



SUGGESTED SOLDER PAD GEOMETRY

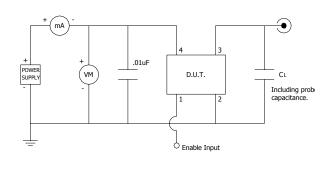


 C_{BYPASS} should be ≥ 0.01 uF.

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 171 Covington Drive
 Bloomingdale, IL 60108
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TEST CIRCUIT, CMOS LOAD



D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION	
1	EOH	Enable Input	
2	GND	Circuit & Package Ground	
3	Output	RF Output	
4 V _{CC}		Supply Voltage	

MARKING INFORMATION

- 1. ** Manufacturing Site Code.
- [Note a dash may follow the site code and is acceptable.] 2. XXXMXXXXX – Frequency is marked with
- only leading significant digits before the 'M' and 4 - 6 digits after the 'M' (including zeros). Ex. XMXXXXXX (3M579545) XXMXXXXX (14M31818) XXXMXXXX (125M0000)
- 3. YYWW Date code, YY year, WW week.
- 4. ST Frequency stability/temperature code. (Refer to Ordering Information.)
- 5. V - Voltage code. 3 = 3.3V, 5 = 5.0V.

NOTES

- 1. Termination pads (e4). Barrier-plating is
- nickel (Ni) with gold (Au) flash plate.
- 2. Reflow conditions per JEDEC J-STD-020.

Rev. F

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TAPE AND REEL INFORMATION

DIMENSIONS IN MILLIMETERS 17.5 - 2.0 Ø13 Ø1.50 1.75 4.0 8.0 2.40 2.10 120° 0 ÷ 0 0 Ć œ Φ C (Th 16.0 8.40 + . Ø60 Ø180 5.70 Ø23 DIRECTION OF FEED

Standard packaging is tape and reel for this product family. Device quantity is 1,000 pieces per 180mm reel.

ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from -55° C to $+125^{\circ}$ C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.		
Mechanical Shock:	1,500g's, 0.5mS duration, $\frac{1}{2}$ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).		
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).		
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.		
Fine Leak:	Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent.		
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.		
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.		
Frequency Aging:	1,000 hours at +85°C, full bias, less than ± 5 ppm shift.		
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.		

Document No. 008-0256-0

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