LOW COST 27 MHZ 3.3 VOLT VCXO

ICS722

Description

The ICS722 is a low cost, low-jitter, high-performance 3.3 volt VCXO designed to replace expensive discrete VCXOs modules. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by over ±100 ppm. Using IDT's patented VCXO techniques, the device uses an inexpensive external pullable crystal in the range of 16.2 to 28 MHz to produce a VCXO output clock at that same frequency.

The frequency of the on-chip VCXO is adjusted by an external control voltage input into pin VIN. Because VIN is a high-impedance input, it can be driven directly from an PWM RC integrator circuit. Frequency output increases with VIN voltage input. The usable range of VIN is 0 to 3.3 V.

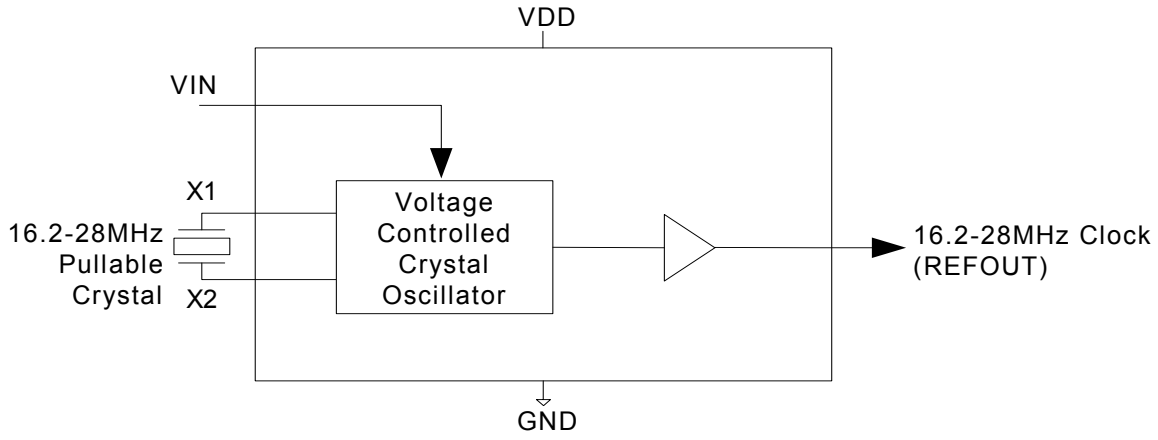
IDT manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult IDT to eliminate VCXOs, crystals, and oscillators from your board.

Features

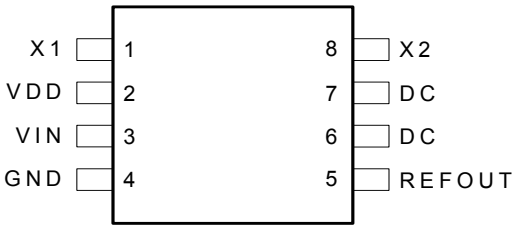
- Packaged in 8-pin SOIC
- Operational frequency range of 16.2 MHz to 28 MHz
- Uses an inexpensive external crystal
- On-chip patented VCXO with pull range of 230 ppm (minimum)
- VCXO tuning voltage of 0 to 3.3 V
- Operating voltage of 3.3 V
- 12 mA output drive capability at TTL levels
- Advanced, low-power, sub-micron CMOS process

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



ICS722

8-Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI	Input	Crystal connection. Connect to the external pullable crystal.
2	VDD	Power	Connect to +3.3 V (0.01µf decoupling capacitor recommended).
3	VIN	Input	Voltage input to VCXO. Zero to 3.3 V signal which controls the VCXO frequency.
4	GND	Power	Connect to ground.
5	REFOUT	Output	VCXO CMOS level clock output matches the nominal frequency of the crystal.
6	DC	—	Do not connect anything to this pin.
7	DC	—	Do not connect anything to this pin.
8	X2	Input	Crystal connection. Connect to a external pullable crystal.

External Component Selection

The ICS722 requires a minimum number of external components for proper operation.

Decoupling Capacitors

A decoupling capacitor of 0.01µF should be connected between VDD and GND on pins 2 and 4 as close to the ICS722 as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Quartz Crystal

The ICS722 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The oscillation frequency of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The ICS722 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the ICS722 is designed to have zero frequency error when the total of on-chip + stray capacitance is
14 pF.

Recommended Crystal Parameters:

Initial Accuracy at 25° C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
Load Capacitance	14 pf
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	250 Max
Equivalent Series Resistance	35 Ω Max

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS722. There should be no via’s between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal. See application note MAN05.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

The procedure for determining the value of these capacitors can be found in application note MAN05.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS722. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+70	° C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.145		3.465	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load		6		mA
Short Circuit Current	I_{OS}			±50		mA
VIN, VCXO Control Voltage	V_{IA}		0		3.3	V

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

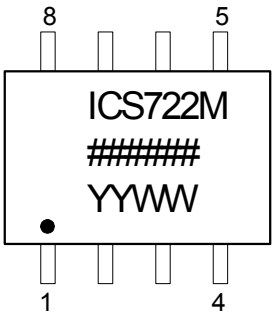
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	F_O		16.2		28	MHz
Crystal Pullability	F_P	0V≤ VIN ≤ 3.3 V, Note 1	± 115			ppm
VCXO Gain		VIN = VDD/2 ± 1 V, Note 1		120		ppm/V
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF			1.5	ns
Output Clock Duty Cycle	t_D	Measured at 1.4 V, C_L=15 pF	40	50	60	%
Maximum Output Jitter, short term	t_J	C_L=15 pF		110		ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

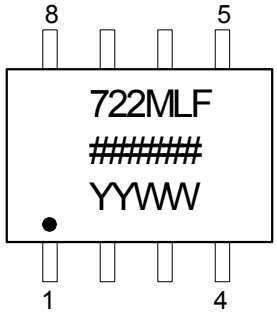
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram (ICS722M)



Marking Diagram (ICS722MLF)

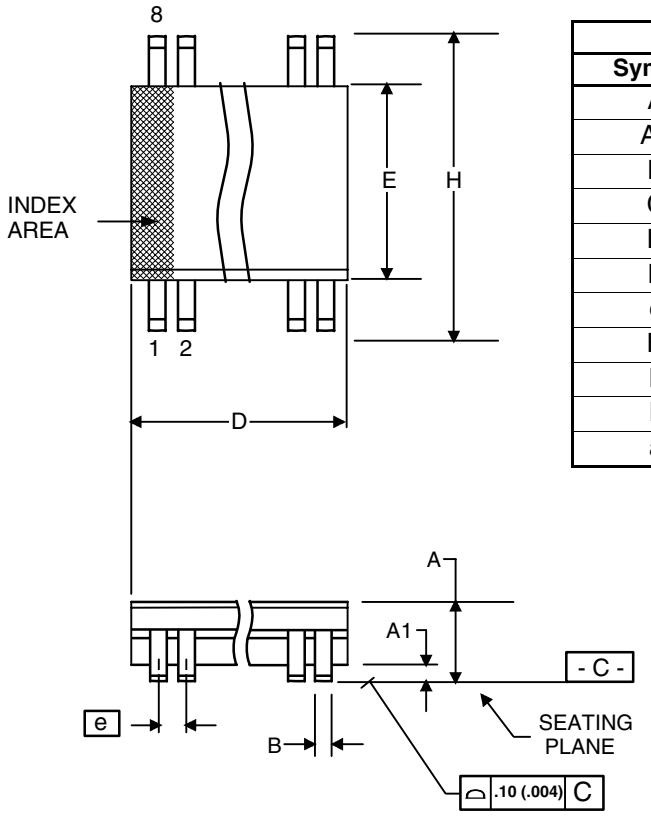


Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “LF” denotes Pb (lead) free package.
4. Bottom marking: (origin)
   Origin = country of origin if not USA.

Package Outline and Package Dimensions (8-pin SOIC)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	1.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	0.1497	0.1574
e	1.27 Basic		0.050 Basic	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
a	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
722M*	see page 5	Tubes	8-pin SOIC	0 to +70° C
722MT*		Tape and Reel	8-pin SOIC	0 to +70° C
722MLF		Tubes	8-pin SOIC	0 to +70° C
722MLFT		Tape and Reel	8-pin SOIC	0 to +70° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

"LF" denotes Pb (lead) free package.

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