
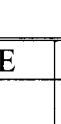
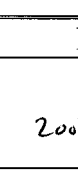


DOCUMENT NUMBER AND REVISION  
**VL-PS-TLM-T700MPZA-01 REV. A**  
**(TLM-T700MPZA-01)**

DOCUMENT TITLE:  
**PRELIMINARY SPECIFICATION**  
**OF**  
**LCD MODULE TYPE**  
**MODEL NUMBER: TLM-T700MPZA-01**

DEPARTMENT	NAME	SIGNATURE	DATE
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**VARITRONIX LIMITED**

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**Preliminary Specification  
 of  
 LCD Module Type  
 Model No.: TLM-T700MPZA-01**

**1. General Description**

- 7.0"(diagonal), wide VGA, 800xRGBx480 dots, 262K colors, positive, transmissive, amorphous silicon TFT LCD module.
- Pixel in stripe configuration.
- Viewing angle: 6 o'clock.
- Logic voltage: +3.3V.
- Normally white.
- White LED02 backlight.
- FPC connection.

**2. Mechanical Specifications**

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		165.1(W) x 104.24(H) x 6.85(D) (excluded connector and cables of backlight and FPC)	mm
Color TFT 800xRGBx480	Active area	152.40(W) x 91.44(H)	mm
	Display format	800 x RGB x 480	dots
	Color configuration	RGB stripes	-
	Dot pitch	0.1905(RGB)(W) x 0.1905(H)	mm
Weight		TBD	grams

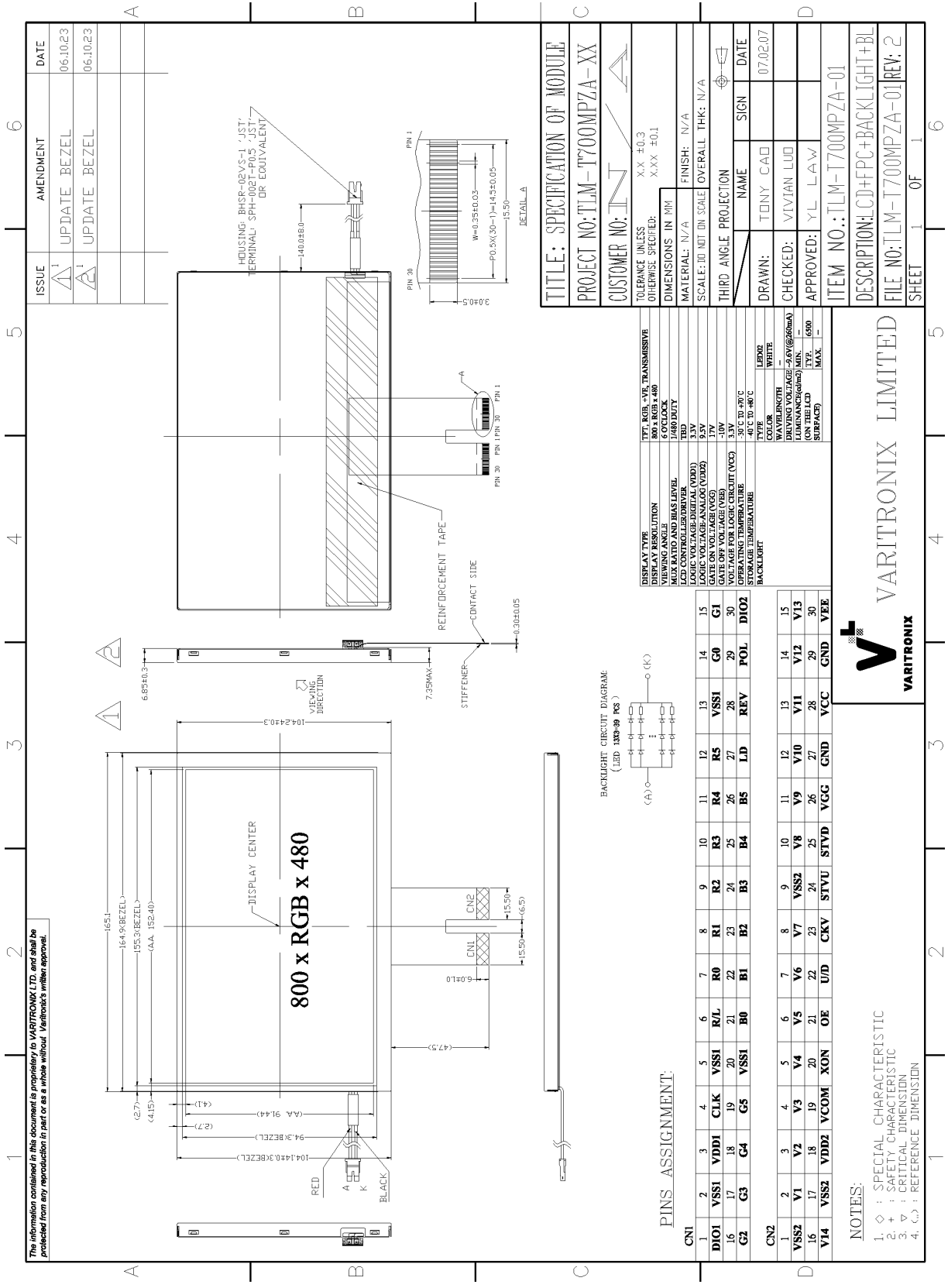
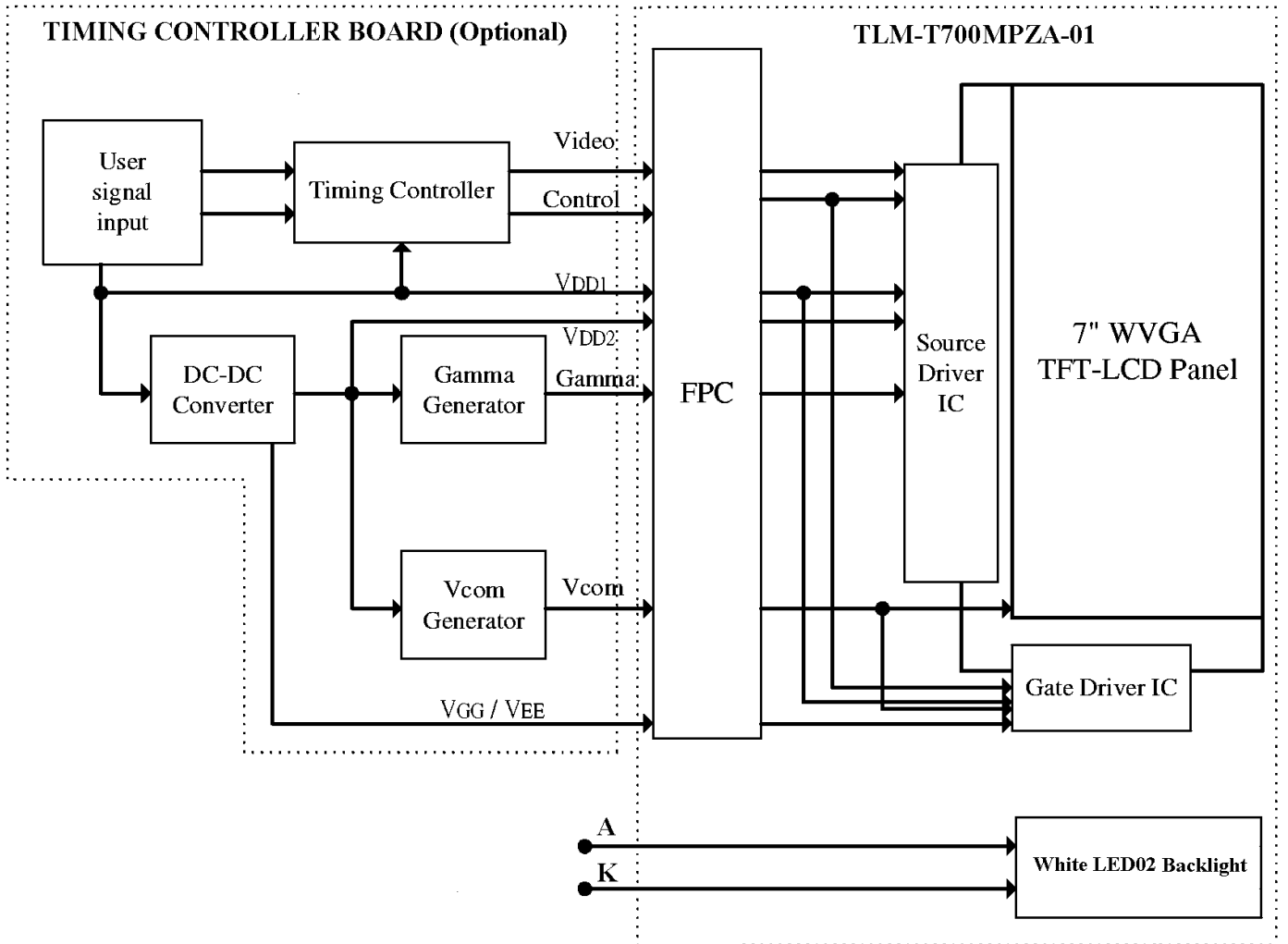


Figure 1: Outline Drawing



Remark:

TIMING CONTROLLER BOARD P/N: PCA-T700MPZA-01.

Figure 2: Block Diagram

### 3. Interface signals

#### 3.1 TFT-LCD Panel Driving

Table 2(a): Pin Assignment of CN1

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output	Note 1
2	VSS1	I	Ground	
3	VDD1	I	Power Supply	
4	CLK	I	Horizontal Shift Clock	
5	VSS1	I	Ground	
6	R/L	I	Right / Left selection	Note 1
7	R0	I	Red Data (LSB)	
8	R1	I	Red Data	
9	R2	I	Red Data	
10	R3	I	Red Data	
11	R4	I	Red Data	
12	R5	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0	I	Green Data (LSB)	
15	G1	I	Green Data	
16	G2	I	Green Data	
17	G3	I	Green Data	
18	G4	I	Green Data	
19	G5	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0	I	Blue Data (LSB)	
22	B1	I	Blue Data	
23	B2	I	Blue Data	
24	B3	I	Blue Data	
25	B4	I	Blue Data	
26	B5	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note 2
28	REV	I	Data invert control	Note 3
29	POL	I	Polarity selection	Note 4
30	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note 1

Table 2(b): Pin Assignment of CN2

Pin No.	Symbol	I/O	Function	Remark
1	VSS2	I	Ground	
2	V1	I	Gamma Voltage 1	Note 10
3	V2	I	Gamma Voltage 2	Note 10
4	V3	I	Gamma Voltage 3	Note 10
5	V4	I	Gamma Voltage 4	Note 10
6	V5	I	Gamma Voltage 5	Note 10
7	V6	I	Gamma Voltage 6	Note 10
8	V7	I	Gamma Voltage 7	Note 10
9	VSS2	I	Ground	
10	V8	I	Gamma Voltage 8	Note 10
11	V9	I	Gamma Voltage 9	Note 10
12	V10	I	Gamma Voltage 10	Note 10
13	V11	I	Gamma Voltage 11	Note 10
14	V12	I	Gamma Voltage 12	Note 10
15	V13	I	Gamma Voltage 13	Note 10
16	V14	I	Gamma Voltage 14	Note 10
17	VSS2	I	Ground	
18	VDD2	I	Voltage for analog circuit	Note 10
19	VCOM	I	Common Voltage	
20	XON	I	NC	
21	OE	I	Output Enable	Note 5
22	U/D	I	Up / Down Selection	Note 6
23	CKV	I	Vertical Shift Clock	Note 7
24	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 6
25	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note 6
26	VGG	I	Gate On Voltage	Note 8
27	GND	I	Ground	
28	VCC	I	Voltage for logic circuit	
29	GND	I	Ground	
30	VEE	I	Gate Off Voltage	Note 9

Note 1: Gate off voltage,  $V_{EE(TYP.)} = -10.0V$ .

Note 2: Gate on voltage,  $V_{GG(TYP.)} = +17V$ .

Note 3: Select up or down shift.

Table 3

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down



Note 4: Gate driver shift clock.

Note 5: When OE is connected to high “1”, the driver outputs are disabled (Gate output =  $V_{EE}$ ). Under this condition, the operation of registers will not be affected.

Note 6: Select left or right shift

Table 4

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to right
0	Hi-Z	Input	Right to left

Note 7: Latch the polarity of outputs and switch the new data to outputs. At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

Note 8: Control whether the Data R0~G5 are inverted or not. (Connecting to GND is suggested.)  
 When “REV=1”, these data will be inverted.

EX: “00”→ “3F”, “07”→ “38”, “15”→ “2A”

Note 9: Polarity selector for dot-inversion control. Available at the rising edge of LD.

When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;

When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.



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Note 10: Typical Application Circuit (When  $V_{DD2(TYP.)} = +9.5V$ )

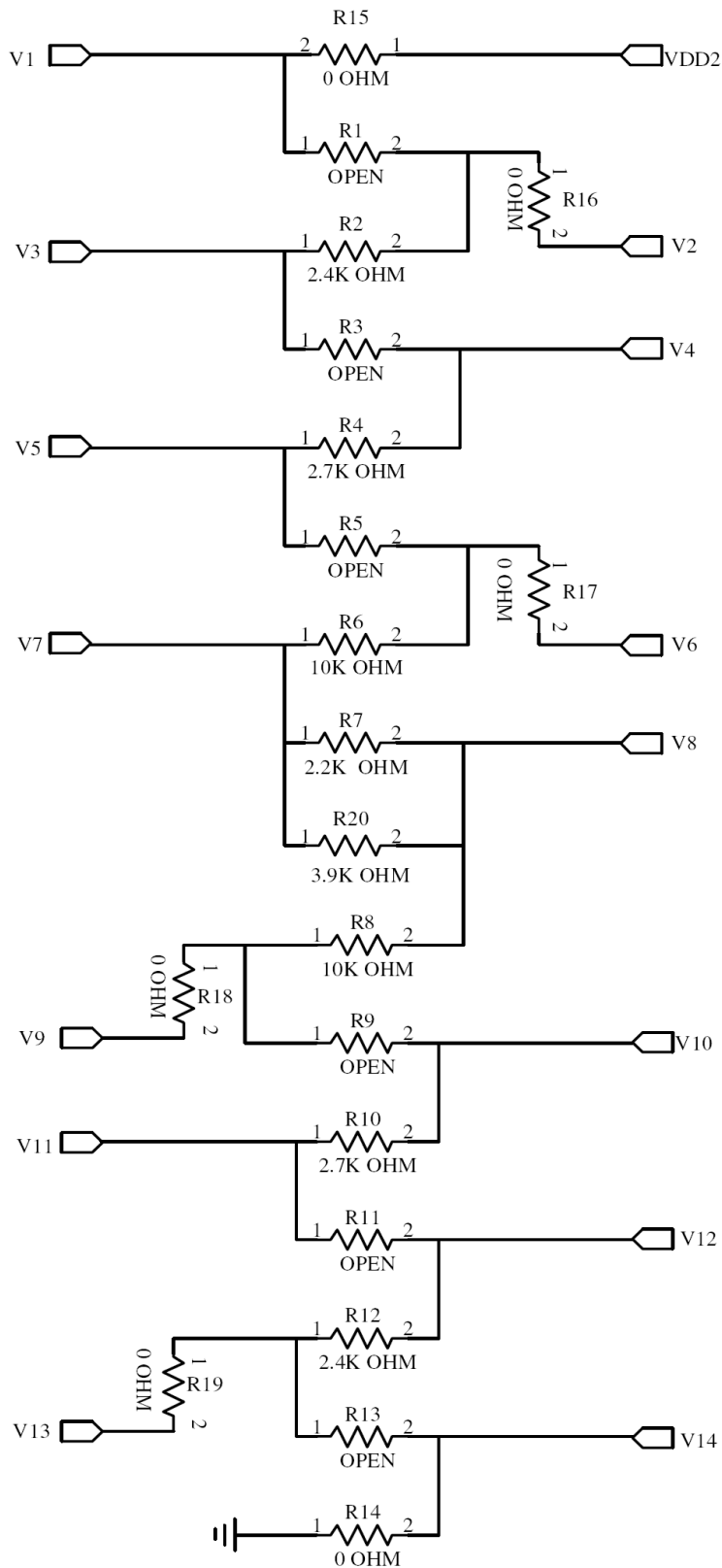


Figure 3

### 3.2 Backlight Driving

Table 5

Symbol	Description	Remark
A	Anode of LED backlight	Wire Color: Red
K	Cathode of LED backlight	Wire Color: Black

## 4. Absolute Maximum Ratings

### 4.1 Electrical Maximum Ratings – For IC Only

Table 6 ( $V_{SS1}=V_{SS2}=GND=0V$ ,  $T_a=25^{\circ}C$ )

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	$V_{DD1}$	-0.3	+5.0	V	
	$V_{CC}$			V	
	$V_{DD2}$	-0.5	+12.0	V	
	$V_{GG}$	-0.3	+40.0	V	
	$V_{GG}-V_{EE}$	-	+40	V	
	$V_{EE}$	-20	+0.3	V	

Note: 1. The modules may be destroyed if they are used beyond the absolute maximum ratings.

### 4.2 Environmental Condition

Table 7

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-30°C	+70°C	-40°C	+80°C	Dry

Note 1: Product cannot sustain at extreme storage conditions for long time.

## 5. Electrical Specifications

### 5.1 Typical Electrical Characteristics

At  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD1}=V_{CC}=3.3\text{V}\pm 0.3\text{V}$ ,  $V_{SS1}=V_{SS2}=\text{GND}=0\text{V}$ .

Table 8

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	$V_{DD1}$	+3.0	+3.3	+3.6	V	
	$V_{DD2}$	+9	+9.5	+10	V	
Supply Voltage for Gate Driver	$V_{GG}$	-	+17	-	V	
	$V_{EE}$	-	-8	-	V	
	$V_{CC}$	+3.0	+3.3	+3.6	V	
Digital Input Voltage	$V_{IH}$	$0.8V_{DD1}$	-	$V_{DD1}$	V	
	$V_{IL}$	0	-	$0.2V_{DD1}$	V	
Vcom Voltage	Vcom	-	+3.1	-	V	

### 5.2 Recommended Driving Condition for LED Backlight

Table 9

( $T_a=25\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage of white LED02 backlight	VLED02	Forward current =260mA	-	~9.6	-	V
Luminance of backlight (on the backlight surface)		Number of LED dies =13x3=39 pcs	-	6500	-	cd/m <sup>2</sup>

### 5.3 Power Consumption

Table 10

(GND=0V, Ta=25°C)

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	I <sub>GG</sub>	V <sub>GG</sub> =+17V	0.32	0.41	mA	
Supply Current for Gate Driver (Low level)	I <sub>EE</sub>	V <sub>EE</sub> =-8.0V	3.35	4.19	mA	
Supply Current for Source Driver (Digital)	I <sub>DD1</sub>	V <sub>DD1</sub> =+3.3V	6	10	mA	
Supply Current for Source Driver (Analog)	I <sub>DD2</sub>	V <sub>DD2</sub> =+9.5V	20	27.5	mA	
Supply Current for Gate Driver (Digital)	I <sub>CC</sub>	V <sub>CC</sub> =+3.3V	0.01	0.013	mA	
LCD Panel Power Consumption (W/O B/L)	-	-	251.97	347.26	mW	

### 5.4 Timing Specifications

#### 5.4.1 Timing Parameters

At Ta=25°C, V<sub>CC</sub>=V<sub>DD1</sub>=3.3V, V<sub>DD2</sub>=9.5V, GND=V<sub>SS1</sub>=V<sub>SS2</sub>=0V

Table 11

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	F <sub>clk</sub>	-	32	40	MHz
CLK Pulse Width	T <sub>cw</sub>	25	-	-	ns
Data Set-up Time	T <sub>su</sub>	4	-	-	ns
Data Hold Time	T <sub>hd</sub>	2	-	-	ns
Propagation Delay of DIO2/1	T <sub>phl</sub>	6	10	15	ns
Time That The Last Data to LD	T <sub>ld</sub>	1	-	-	T <sub>cw</sub>
Pulse width of LD	T <sub>wld</sub>	2	-	-	T <sub>cw</sub>
Time That LD to DIO1/2	T <sub>lds</sub>	5	-	-	T <sub>cw</sub>
POL Set-up Time	T <sub>psu</sub>	6	-	-	ns
POL Hold Time	T <sub>phd</sub>	6	-	-	ns
OE Pulse Width	T <sub>OEV</sub>	1	-	-	μs
CKV Pulse Width	T <sub>CKV</sub>	500	-	-	ns
STV Set-up Time	T <sub>SUV</sub>	400	-	-	ns
STV Hold Time	T <sub>HdV</sub>	400	-	-	ns
Horizontal Display Period	T <sub>HDP</sub>	-	800	-	T <sub>cw</sub>
Horizontal Period Timing Range	T <sub>HP</sub>	-	1056	-	T <sub>cw</sub>
Horizontal Lines Per Field	T <sub>V</sub>	484	508	620	THP
Vertical Display Timing Range	T <sub>DV</sub>	-	480	-	THP



### 5.4.2 Timing Diagram

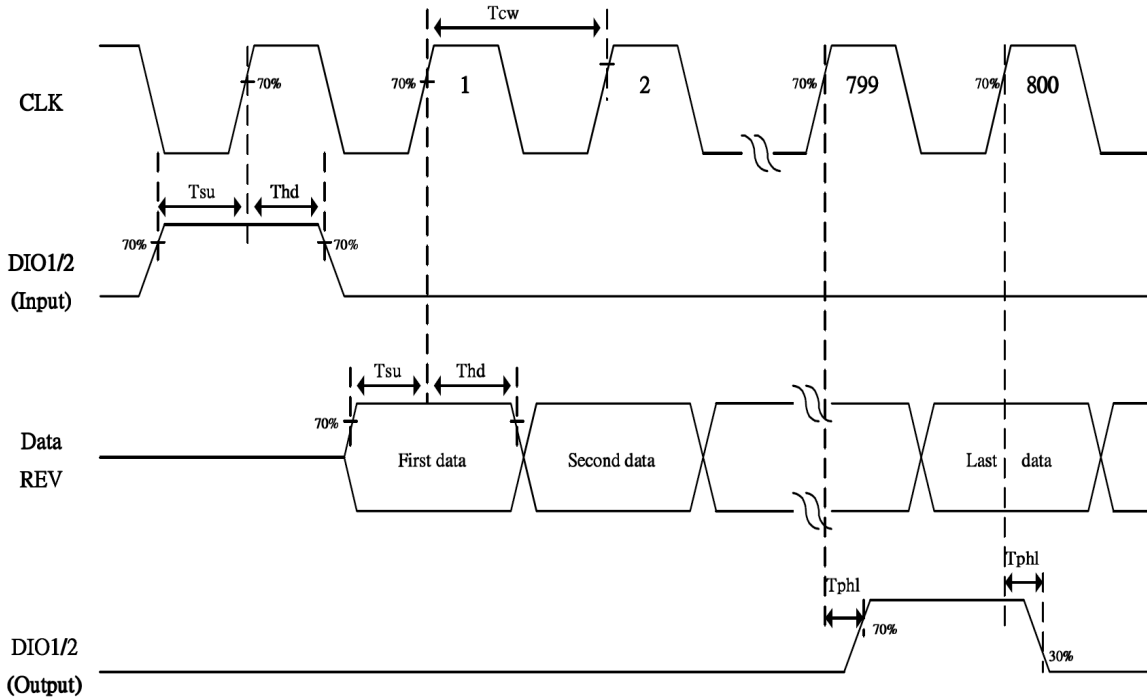


Figure 4: Horizontal timing (1)

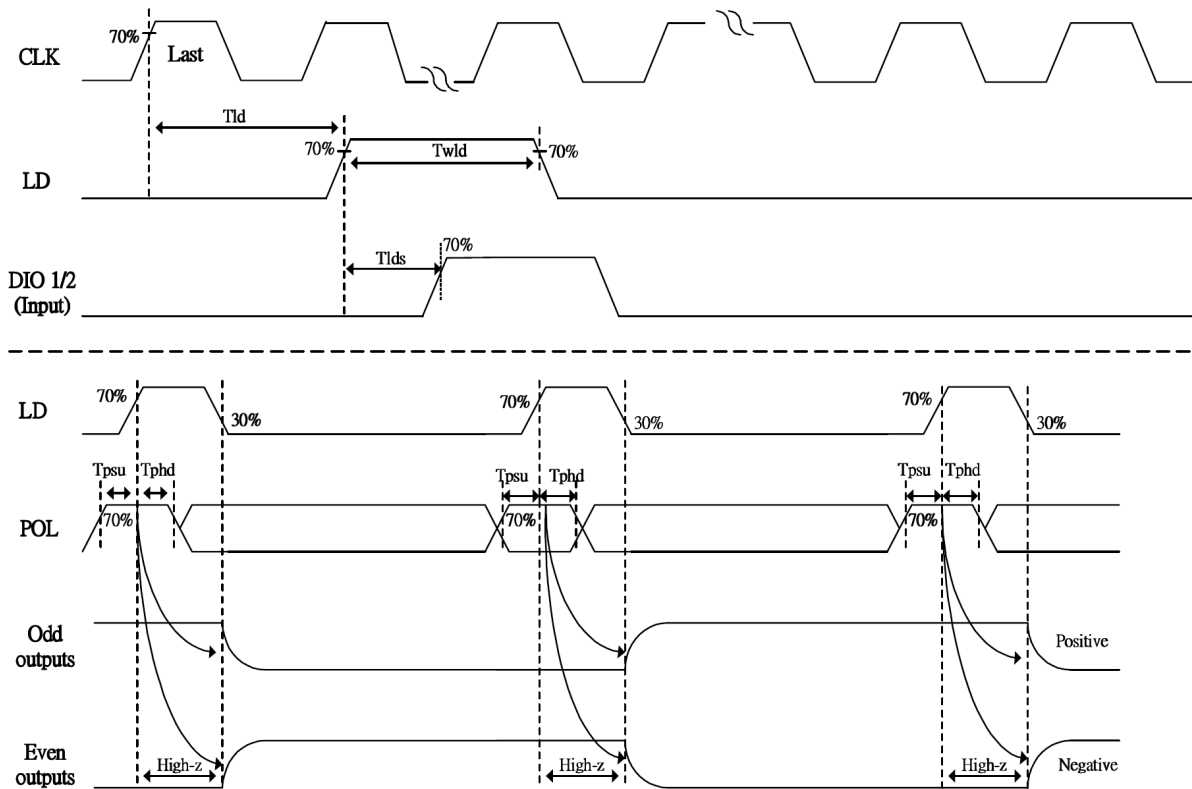


Figure 5: Horizontal timing (2)

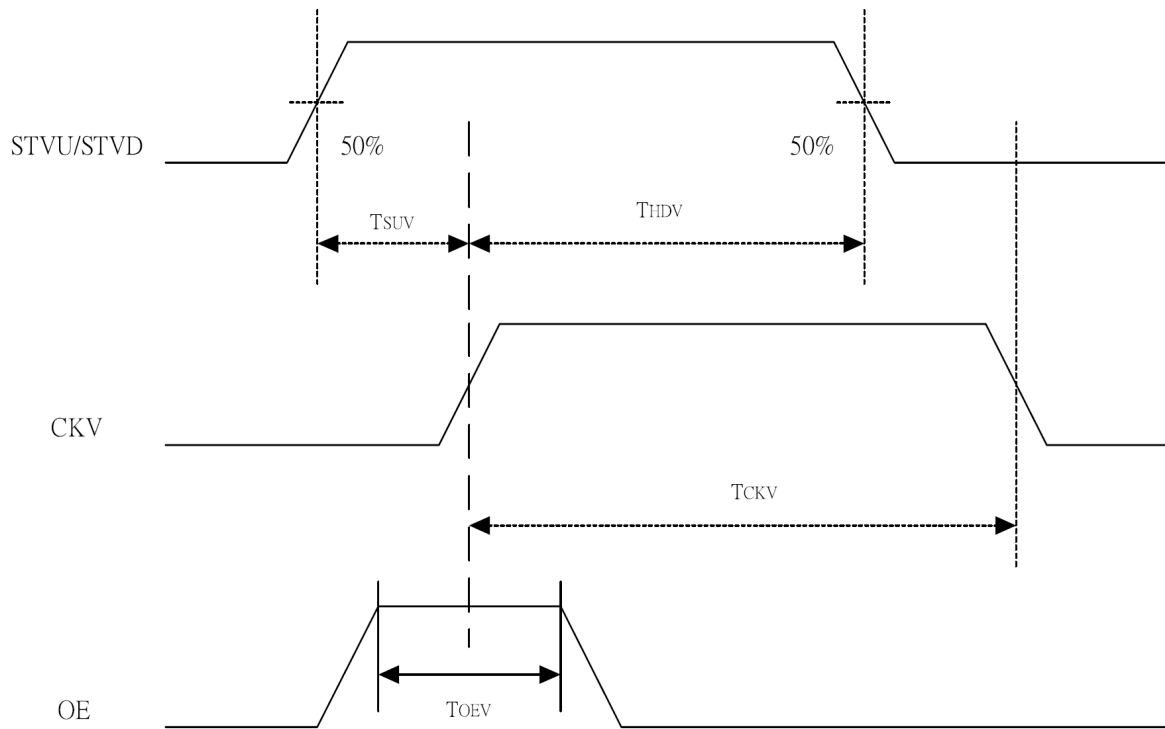


Figure 6: Vertical shift clock timing

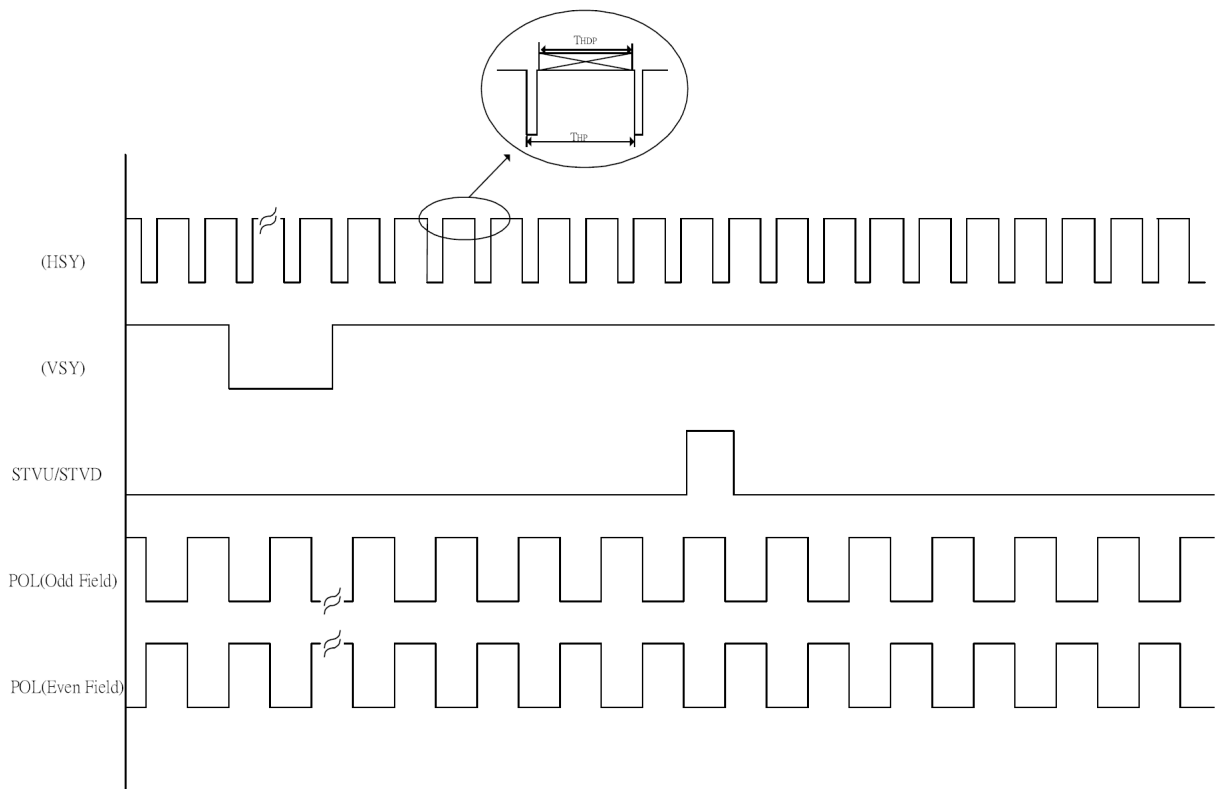
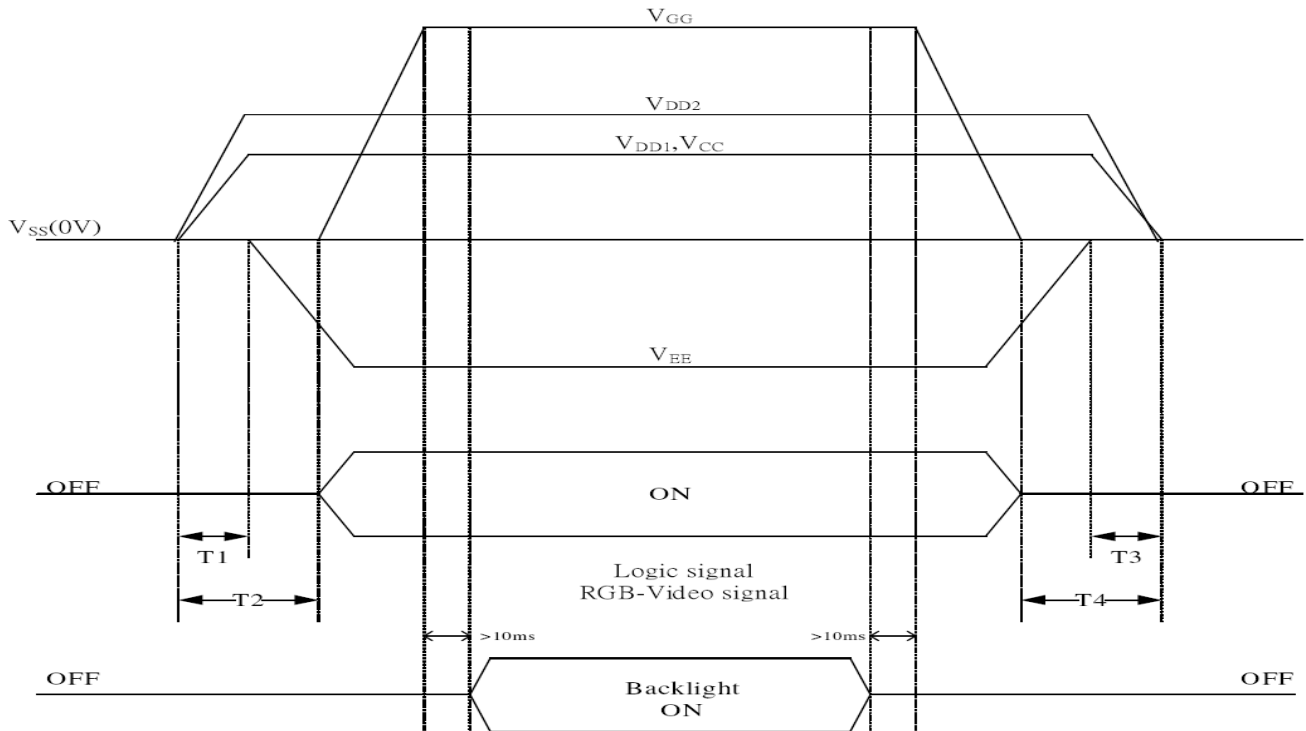


Figure 7: Vertical timing

### 6. Power On Sequence

The Power on sequence only effect by VCC,VDD1,VDD2,VEE and VGG, the others do not care.



$$1. 10\text{ms} \leq T1 < T2$$

$$2. 0\text{ms} < T3 \leq T4 \leq 10\text{ms}$$

Figure 8

### 7. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

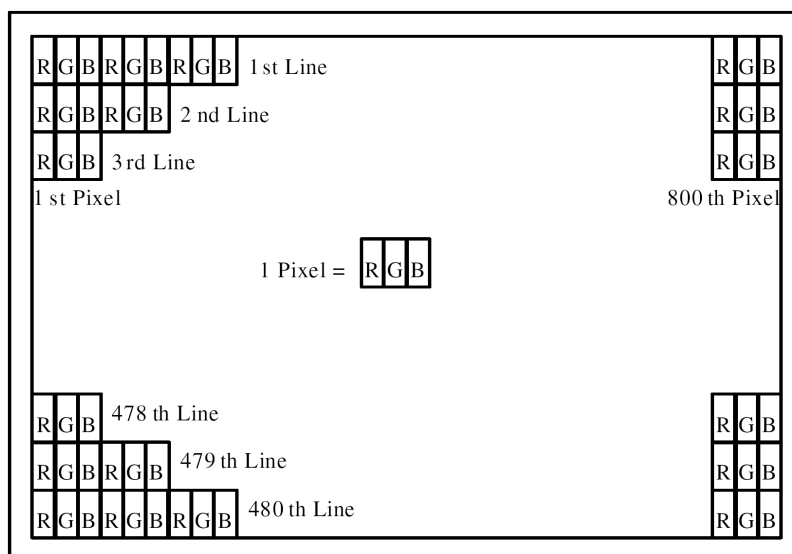


Figure 9





**8. Display Color and Gray Scale Reference**

Table 12

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

### 9. Optical Characteristics

Following data was test with WV+AG polarizer and B/L.(B/L=5900nits)

Table 13: Optical characteristics (Ta=25°C)

Parameter	Symbol	Condition	Values			Units	Remarks	
			Min	Typ	Max			
Viewing Angle	Horizontal	$\phi 1$ (3 o'clock), $\phi 2$ (9 o'clock)	CR>10	$\pm 55$	$\pm 60$	-	deg	Note 1
	Vertical	$\theta 2$ (12 o'clock)		35	40	-	deg	
		$\theta 1$ (6 o'clock)		50	55	-	deg	
Contrast Ratio	CR	-	250	400	-	-	Note 2	
Response time	Rise	Tr	$\theta=0^\circ$	-	15	30	ms	Note 3
	Fall	Tf		-	25	50		
Cross Talk	-	$\theta=0^\circ$	-	-	3.5	%	Note 4	
Transmission	T	$\theta=0^\circ$	6.0	6.5	-	%	Note 3	
Brightness	-	-	340	400	-	cd/m <sup>2</sup>		

All the optical measurement shall be executed 30 minutes after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.

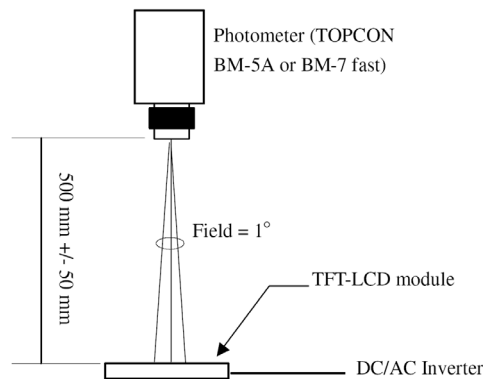


Figure 10

Note 1: The definition of viewing angle are as follow

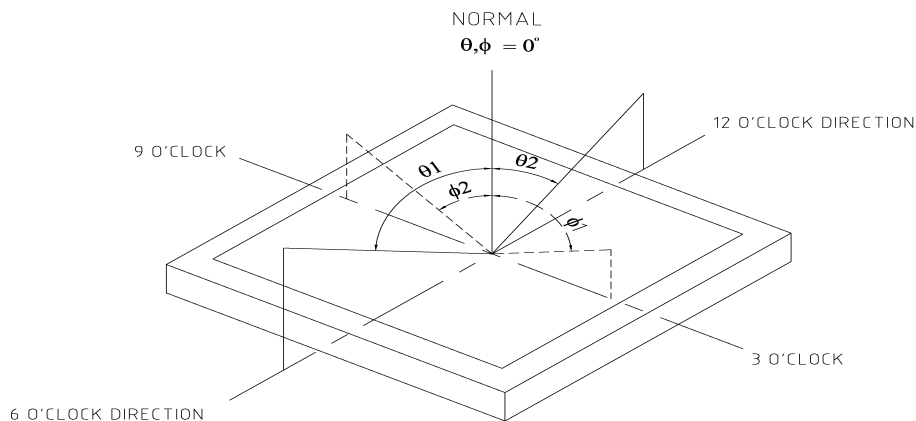


Figure 11

Note 2: The definition of contrast ratio  $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 3: Definition of Response Time  $T_r$  and  $T_f$ :

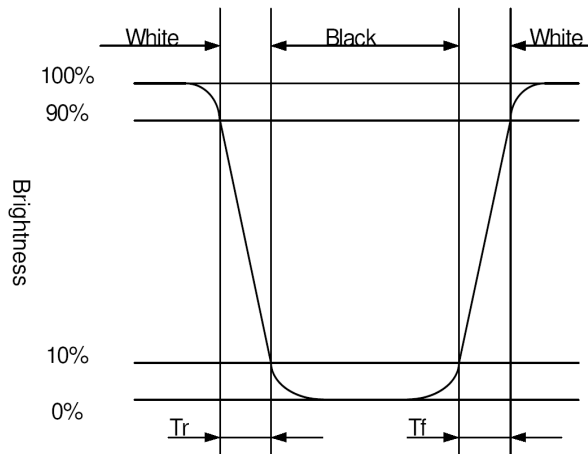


Figure 12

Note 4: Cross Talk (CTK)  $= (|Y_A - Y_B| / Y_A) \times 100\%$

$Y_A$ : Brightness of Pattern A

$Y_B$ : Brightness of Pattern B

Luminance meter: BM 5A or BM-7 fast (TOPCON)

Measurement distance: 500 mm +/- 50 mm

Ambient illumination: < 1 Lux

Measuring direction: Perpendicular to the surface of module.

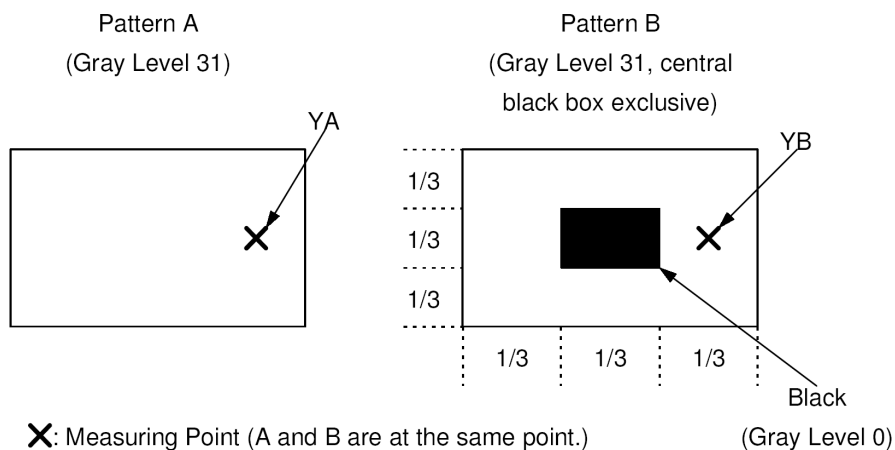


Figure 13

**10. Reliability for LCD Panel Only**

Table 14

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +85°C, 240hrs	
2	Low Temperature Storage Test	Ta = -40°C, 240hrs	
3	High Temperature Operation Test	Ta = +80°C, 240 hrs	
4	Low Temperature Operation Test	Ta = -30°C, 240hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-30°C → +80°C, 200 Cycles 30min 30min	
7	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal	

Ta: ambient temperature

Note: The protective film must be removed before temperature test.

[Criteria]

1. Main LCD should normally work under the normally condition no defect of function, screen quality and appearance (including: mura, line defect, no image).
2. After the temperature and humidity test, the luminance and CR (Contrast ratio), should not be lower than minimum of specification.

## **11. Handling Cautions**

### **11.1 Mounting of module**

- Please power off the module when you connect the input/output connector.
- Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
  - 1.The noise from the backlight unit will increase.
  - 2.The output from inverter circuit will be unstable.
  - 3.In some cases a part of module will heat.

### **11.2 Precautions in mounting**

- When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

### **11.3 Adjusting module**

- Adjusting volumes on the rear face of the module have been set optimally before shipment.
- Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

### **11.4 Others**

- Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- Store the module at a room temperature place.
- The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.



- Observe all other precautionary requirements in handling general electronic components.
- Please adjust the voltage of common electrode as material of attachment by 1 module.

"Varitronix Limited reserves the right to change this specification."

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- END -