Three-Channel, Closed-Loop, Switch Mode LED Driver IC

Features

- Switch mode controller for single-switch converters
- Closed loop control of output current
  - Buck
  - Boost
  - SEPIC
- High PWM dimming ratio
- Internal 40V linear regulator
- Constant frequency operation
- Programmable slope compensation
- Linear and PWM dimming
- +0.2A/-0.4A gate drives for the switching FETs
- Output short circuit protection
- Output over voltage protection
- Hiccup mode protection
- Analog control of PWM dimming

Applications

- RGB backlight applications
- Multiple string white LED driver applications

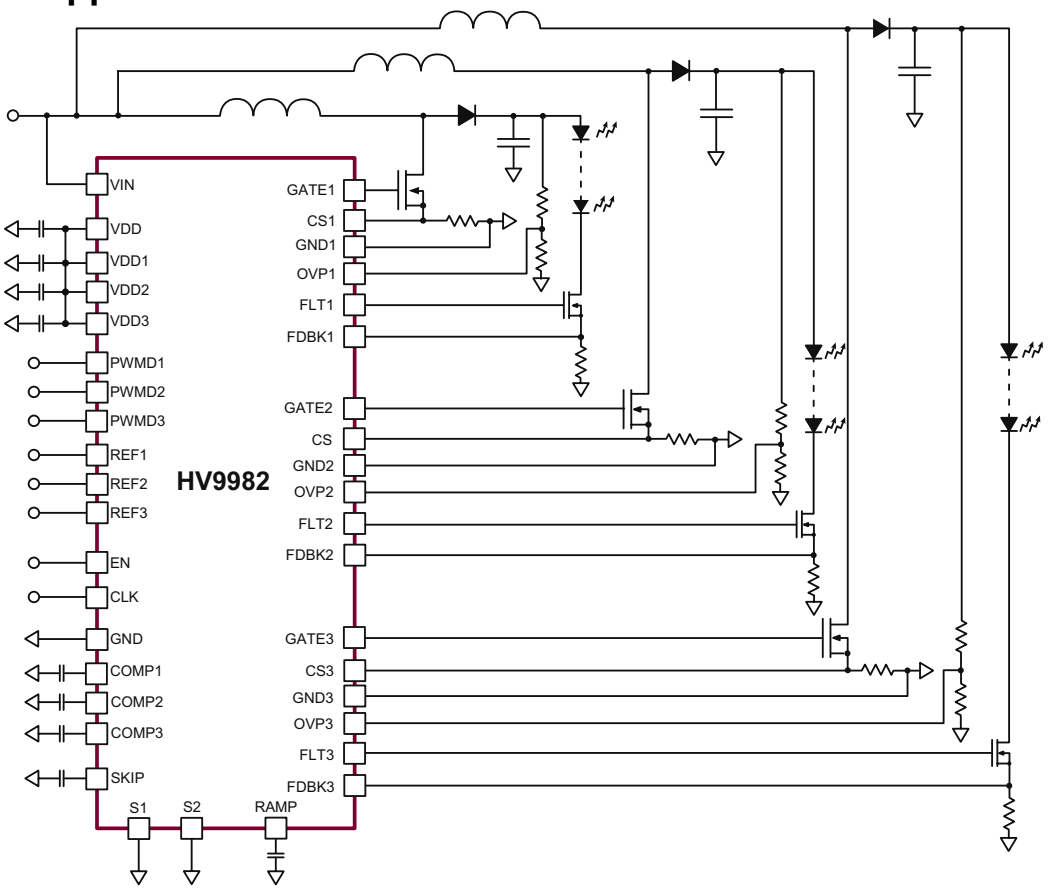
General Description

The HV9982 is a three-channel, closed loop, peak current mode PWM controller for driving a constant output current. It can be used for driving either RGB LEDs or multiple channels of white LEDs.

The HV9982 includes a 40V linear regulator which provides an 8.0V supply to power the IC. The switching frequencies of the three converters are controlled by an external clock signal. The channels operate at a switching frequency of 1/12th of the external clock frequency to minimize the input current ripple. Each converter is driven by a peak current mode controller with output current feedback.

The three output currents can be individually dimmed using either linear or PWM dimming. The IC also includes three disconnect FET drivers which enable high PWM dimming ratios and also help to disconnect the input in case of an output short circuit condition. HV9982 includes a hiccup mode protection for both open LED and short circuit condition with automatic recovery when the fault clears.

Typical Boost Application Circuit

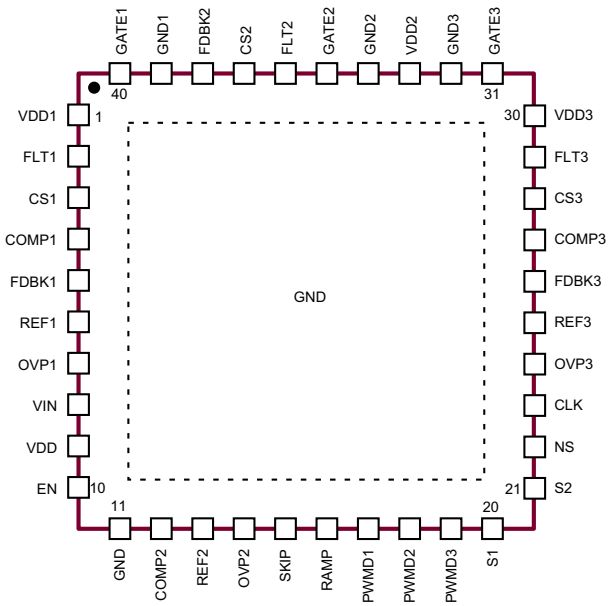


Ordering Information

Device	40-Lead QFN *6.00x6.00mm body* *1.00mm height (max)* *0.50mm pitch*
HV9982	HV9982K6-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



40-Lead QFN (K6)
(top view)

Absolute Maximum Ratings

Parameter	Value
VIN to GND	-0.5V to +45V
VDD to GND, VDD 1-3 to GND	-0.3V to +10V
All other pins to GND	-0.3V to (V_{DD} + 0.3V)
Junction temperature	+125°C
Storage ambient temperature range	-65°C to +150°C
Continuous Power dissipation (T_A = +25°C)	5000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
= "Green" Packaging

Package may or may not include the following marks: Si or

40-Lead QFN (K6)

Thermal Resistance

Package	θ_{ja}
40-Lead QFN	18.1°C/W

Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range of 0°C < T_A < +85°C, otherwise the specifications are at T_A = 25°C. V_{DD} = 8.0V unless otherwise noted)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage	*	10	-	40	V	DC input voltage
I_{INSD}	Shut-down mode supply current	*	-	-	500	µA	EN ≤ 0.8V
I_{IN}	Supply current	-	-	-	4.5	mA	EN ≥ 2.0V; PWMD1 = PWMD2 = PWMD3 = GND
R_{EN}	Pull-down resistor	-	75	130	160	kΩ	V_{EN} = 5.0V
Internal Regulator							
V_{DD}	Internally regulated voltage	*	7.25	7.75	8.25	V	V_{IN} = 12-40V; EN = HIGH; PWMD1-3 = V_{DD}; GATE1-3 = 1nF; CLK = 6MHz
UVLO	V_{DD} under voltage lockout threshold	-	6.0	-	6.5	V	V_{DD} falling
$UVLO_{HYST}$	V_{DD} under voltage hysteresis	-	-	500	-	mV	V_{DD} rising

 # Denotes specifications guaranteed by design
** The specifications which apply over the full operating temperature range at 0°C < T_A < +85°C are guaranteed by design and characterization.*

Electrical Characteristics *(cont.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
PWM Dimming (PWMD1, PWMD2 and PWMD3)							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull down resistor	-	75	130	160	kΩ	V_{PWMD} = 5V
Gate (GATE1, GATE2 and GATE3)							
I_{SOURCE}	Gate short circuit current, sourcing	#	0.2	-	-	A	V_{GATE} = 0V
I_{SINK}	Gate sinking current	#	0.4	-	-	A	V_{GATE} = V_{DD}
T_{RISE}	Gate output rise time	-	-	-	85	ns	C_{GATE} = 1.0nF
T_{FALL}	Gate output fall time	-	-	-	45	ns	C_{GATE} = 1.0nF
D_{MAX}	Maximum duty cycle	#	-	91.7	-	%	---
Over Voltage Protection (OVP1, OVP2 and OVP3)							
$V_{OVP,rising}$	Over voltage rising trip point	*	4.5	5.0	5.5	V	OVP rising
$V_{OVP,HYST}$	Over voltage hysteresis	-	-	0.5	-	V	OVP falling
Current Sense (CS1, CS2 and CS3)							
T_{BLANK}	Leading edge blanking	*	100	-	250	ns	---
T_{DELAY}	Delay to output of gate	*	-	-	200	ns	100mV overdrive to the current sense
R_{DIS}	Discharge resistance for slope compensation	*	-	-	650	Ω	Gate = Low
Internal Transconductance Opamp (Gm1, Gm2 and Gm3)							
GB	Gain bandwidth product	#	-	1.0	-	MHz	75pF capacitance at COMP pin
A_V	Open loop DC gain	-	65	-	-	dB	Output open
V_{CM}	Input common-mode range	#	-0.3	-	3.0	V	---
V_O	Output voltage range	#	0.7	-	V_{DD}	V	---
G_m	Transconductance	-	500	600	700	µA/V	---
V_{OFFSET}	Input offset voltage	-	-5.0	-	5.0	mV	---
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
Oscillator (CLOCK)							
f_{OSC1}	Oscillator frequency	-	-	500	-	kHz	F_{CLOCK} = 6.0MHz
K_{SW}	Oscillator divider ratio	#	-	6.0	-	-	---
T_{OFF}	CLOCK low time	#	50	-	-	ns	---
T_{ON}	CLOCK high time	#	50	-	-	ns	---
$V_{CLOCK,HI}$	CLOCK input high	*	2.0	-	-	V	---
$V_{CLOCK,LO}$	CLOCK input low	*	-	-	0.8	V	---

 # Denotes specifications guaranteed by design.

** The specifications which apply over the full operating temperature range at $0^oC < T_A < +85^oC$ are guaranteed by design and characterization.*

Electrical Characteristics *(cont.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Disconnect Driver (FAULT1, FAULT2 and FAULT3)							
$T_{RISE,FAULT}$	Fault output rise time	-	-	-	450	ns	330pF capacitor at $\overline{FAULT}$ pin
$T_{FALL,FAULT}$	Fault output fall time	-	-	-	200	ns	330pF capacitor at $\overline{FAULT}$ pin
Short Circuit Protection (all three channels)							
$T_{BLANK,SC}$	Blanking time	*	400	-	700	ns	---
G_{SC}	Gain for short circuit comparator	-	1.85	2.0	2.15	-	---
V_{omin}	Minimum current limit threshold	#	0.15	-	0.25	V	REF = GND
T_{OFF}	Propagation time for short circuit detection	-	-	-	250	ns	FDBK = 2 • REF + 0.1V
HICCUP timer							
$I_{HC,SOURCE}$	Current source at SKIP pin used for hiccup mode protection	-	-	10	-	µA	---
$V_{TH(H)}$	High threshold at SKIP pin	#	-	5.0	-	V	---
$V_{TH(L)}$	Low threshold at SKIP pin	#	-	0.1	-	V	---
C_{RAMP} for Analog Control of PWM Dimming							
$F_{RAMP,min}$	Minimum frequency	-	-	110	-	Hz	C_{RAMP} = 10nF
$F_{RAMP,max}$	Maximum frequency	-	-	1250	-	Hz	C_{RAMP} = 1.0nF
V_{RAMP}	Voltage of ramp	-	0.2	-	1.85	V	---

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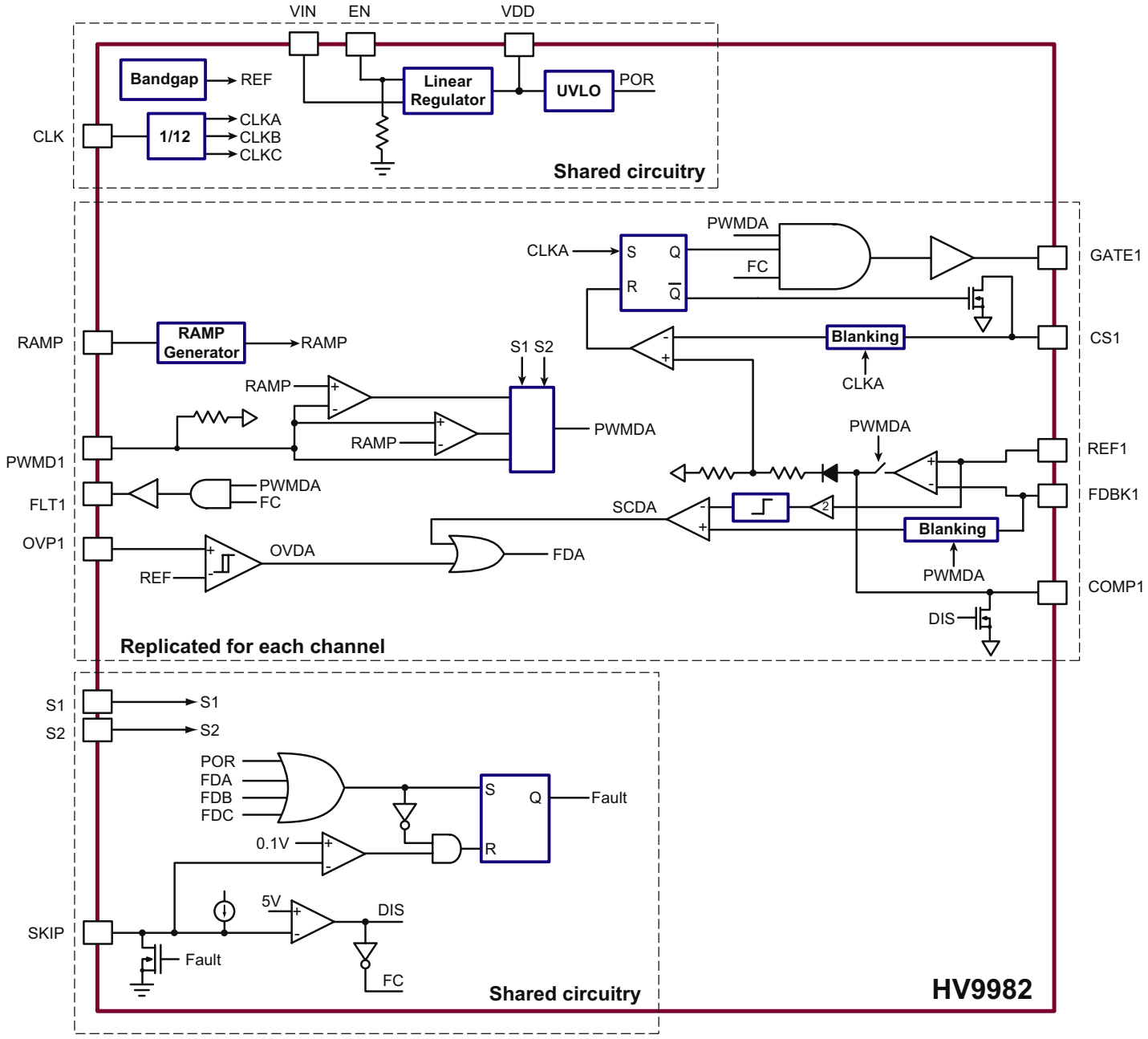
Internal Block Diagram



Functional Description

Power Topology

The HV9982 is a three-channel, switch-mode converter LED driver designed to control a continuous conduction mode buck, boost or SEPIC converter in a constant frequency mode. The IC includes an internal linear regulator, which operates from input voltages 10 to 40V. The IC can also be powered directly using the VDD pins and bypassing the internal linear regulator. The IC includes features typically required in LED drivers like open LED protection, output short circuit protection, linear and PWM dimming, programmable input current limiting and accurate control of the LED current. A high current gate drive output enables the controller to be used in high power converters. The IC is ideally suited for backlight application using either RGB or multi-channel white LED configurations.

Power Supply to the IC (VIN, VDD, VDD1-3)

The HV9982 can be powered directly from its VIN pin that withstands a voltage up to 40V. When a voltage is applied at the VIN pin, the HV9982 tries to maintain a constant 7.75V (typ) at the VDD pin. The regulator also has a built in under-voltage lockout which shuts off the IC if the voltage at the VDD pin falls below the UVLO threshold. By connecting this VDD pin to the VDD1-3 pins of the three channels, the internal regulator can be used to power all three channels in the IC.

In case the internal regulator is not utilized, an external power supply (7.0 - 9.0V) can be used to power the IC. In this case, the power supply is directly connected to the VDD1-3 pins and the VIN pin is left unconnected.

All four VDD pins must by bypassed by a low ESR capacitor (≥0.1µF) to provide a low impedance path for the high frequency current of the output gate driver. These capacitors must be referenced to the individual grounds for proper noise rejection (see Layout Guidelines section for more information). Also, in all cases, the four VDD pins *must* be connected together externally.

The input current drawn from the external power supply (or VIN pin) is a sum of the 4.5mA (max) current drawn by all the internal circuitry and the current drawn by the gate drivers (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 4.5mA + (Q_{g1} + Q_{g2} + Q_{g3}) \bullet f_S$$

In the above equation, f_S is the switching frequency of the converters and Q_{g1-3} are the gate charges of the external FETs (which can be obtained from the FET datasheets).

The EN pin is a TTL compatible input used to disable the IC. Pulling the EN pin to GND will shut down the IC and reduce the quiescent current drawn by the IC to be less than 500µA. If the enable function is not required, the EN pin can be connected to VDD.

Clock Input (CLK)

The switching frequency of the converters is set by using a TTL compatible square wave input at the CLK pin. The switching frequencies of the three converters will be 1/12TH the frequency of the external clock.

Current Sense (CS1-3)

The current sense input is used to sense the source current of the switching FET. Each CS input of the HV9982 includes a built in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 13. This voltage is used as the reference for the current sense comparators. Since the maximum voltage of the COMP pin is (V_{DD} - 1.0V), this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current.

The current sense resistor R_{CS} should be chosen so that the input inductor current is limited to below the saturation current level of the input inductor. For discontinuous conduction mode of operation, no slope compensation is necessary. In this case, the current sense resistor is chosen as:

$$R_{CS} = \frac{V_{DD} - 1.0V}{13 \bullet I_{IN,pk}}$$

where $I_{IN,pk}$ is the maximum desired peak input current.

For continuous conduction mode converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 0.5. This factor must also be accounted for when determining R_{CS} (see Slope Compensation section).

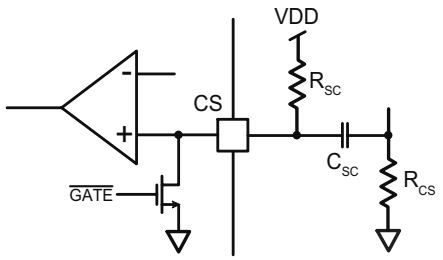
Slope Compensation

Choosing a slope compensation which is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation in the HV9982 can be programmed by two external components (see Fig. 1). A resistor for VDD sets a current (which is almost constant since the V_{DD} voltage is much larger than the voltage at the CS pin). This current flows into the capacitor and produces a ramp voltage across the capacitor. The voltage at the CS pin is then the sum of the voltage across the capacitor and the voltage across the current sense resistor, with the voltage across the capacitor providing the required slope compensation. When the GATE

turns off, an internal pull down FET discharges the capacitor. The 650Ω resistance of the internal FET will prevent the voltage at the CS pin from going all the way to zero.

Fig.1 Slope Compensation



The minimum value of the voltage will instead be:

$$V_{CS,MIN} = \frac{V_{DD}}{R_{SC}} \bullet 650\Omega$$

The slope compensation capacitor is chosen so that it can be completely discharged by the internal 650Ω FET at the CS pin during the time the FET is off. Assuming the worst case switch duty cycle of 92%,

$$C_{SC} = \frac{0.08}{3 \bullet 650\Omega \bullet f_S}$$

Assuming a down slope of DS (A/ms) for the inductor current, the current sense resistor and the slope compensation resistor can be computed as:

$$R_{CS} = \frac{V_{DD} - 1}{13} \bullet \frac{1}{\left(\frac{DS \bullet 10^6 \bullet 0.92}{2 \bullet f_S}\right) + I_{IN,pk}}$$

$$R_{SC} = \frac{2 \bullet V_{DD}}{DS \bullet 10^6 \bullet C_{SC} \bullet R_{CS}}$$

Control of the LED Current

The LED currents in the HV9982 are controlled in a closed-loop manner. The current references which set the three LED currents are provided at the REF pins (REF1-3). This reference voltage is compared to the voltage at the FDBK1-3 pins which sense the LED currents in the three channels using current sense resistors. HV9982 includes three 1MHz transconductance amplifiers with tri-state output, which are used to close the feedback loops and provide accurate current control. The compensation networks are connected at the COMP pins (COMP1-3).

The output of the op-amps are buffered and connected to the current sense comparators using a 12R:1R resistor divider.

The outputs of the op-amps are controlled by the signal applied to the PWMD pins (PWMD1-3). When PWMD is high, the output of the opamp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor will force the converter into steady state almost instantaneously.

Linear Dimming

Linear Dimming can be accomplished in the HV9982 by varying the voltages at the REF pins. Note that since the HV9982 is a peak current mode controller, it has a minimum on-time for the GATE outputs. This minimum on-time will prevent the converters from completely turning off even when the REF pins are pulled to GND. Thus, linear dimming cannot accomplish true zero LED current. To get zero LED current PWM dimming has to be used. Note that different signals can be connected to the three REF pins if desired and they need not be connected together.

Due to the offset voltage of the short circuit comparator as well as the non-linearity of the X2 gain stage, pulling the REF pin very close to GND would cause the internal short circuit comparator to trigger and shut down the IC. To overcome this, the output of the gain stage is limited to 125mV (minimum), allowing the REF pin to be pulled all the way to 0V without triggering the short circuit comparator.

PWM Dimming

PWM dimming in the HV9982 can be accomplished in one of two ways - true PWM dimming using TTL compatible square wave sources at the PWMD pins (PWMD1-3) or an analog control of PWM dimming by applying a 0 - 2.0V linear signal to the PWMD pins. The analog control of PWM dimming helps the HV9982 to be backward compatible with CCFL controllers. All three channels can be individually PWM dimmed as desired.

The mode of PWM dimming is set using control pins S1 and S2. The truth table for S1 and S2 control is given in Table 1. It is recommended that the pins be connected to either VDD or GND and not left unconnected.

Table 1: S1 and S2 control logic

S1	S2	PWMD output
0	0	The output will follow PWMD input signal
0	1	
1	0	Input DC zero volt corresponds to 100% duty cycle output
1	1	Input DC two volt corresponds to 100% duty cycle output

When S1 is high and the HV9982 is operating in the analog control of PWM dimming mode, the PWM dimming frequency is set by a capacitor connected at the RAMP pin. The

RAMP frequency range is 100Hz - 1.0kHz and the capacitor can be selected as:

$$f(Hz) = \frac{1.0\mu S}{C_{RAMP}}$$

Note: *In the following description of the PWM dimming performance the PWMD signals refer to the internal PWM dimming signal and not to the signal applied at the PWMD pins.*

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance opamp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching and the FLT pin goes low, turning off the disconnect switch.

The output capacitor of the converter determines the PWM dimming response of the converter, since it has to get charged and discharged whenever the PWMD signal goes high or low. In the case of a buck converter, since the inductor current is continuous, a very small capacitor is used across the LEDs. This minimizes the effect of the capacitor on the PWM dimming response of the converter. However, in the case of a boost converter, the output current is discontinuous and a very large output capacitor is required to reduce the ripple in the LED current. Thus, this capacitor will have a significant impact on the PWM dimming response. By turning off the disconnect switch when PWMD goes low, the output capacitor is prevented from being discharged and thus the PWM dimming response of the boost converter Improves dramatically.

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The filter capacitor should be chosen large enough so that it can absorb the inductor energy without significant change to the voltage across it.

Fault Conditions

The HV9982 is a robust controller which can protect the LEDs and the LED driver in case of fault conditions. The HV9982 includes both open LED protection and output short circuit protection. In both cases, the HV9982 shuts down and attempts a restart. The hiccup time can be programmed by a single external capacitor at the SKIP pin.

During start-up or when a fault condition is detected, both GATE and FLT outputs are disabled, the COMP pins and SKIP pins are pulled to GND. Once the voltage at the SKIP pin falls below 0.1V and the fault condition(s) have disappeared, the capacitor at the SKIP pin is released and is charged slowly by a 10µA current source. Once the capacitor is charged to 5.0V, the COMP pins are released and GATE and FLT pins are allowed to turn on. If the hiccup time is long enough, it will ensure that the compensation networks are all completely discharged and that the converters start at minimum duty cycle.

The hiccup timing capacitor can be programmed as:

$$C_{RAMP} = \frac{10\mu A \bullet t_{HICCUP}}{4.9V}$$

Short Circuit Protection

When a short circuit condition is detected (output current becomes higher than twice the steady state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the short circuit condition disappears. At this time, the hiccup timer is started (Fig. 3). Once the timing is complete, the converter attempts to restart. If the fault condition still persists, the converter shuts down and goes through the cycle again. If the fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This allows the LED driver to recover from accidental shorts without having to reset the IC.

During short circuit conditions, there are two conditions that determine the hiccup time.

The first is the time required to discharge the compensation capacitors. Assuming a pole-zero R-C network at the COMP pin (series combination of R_Z and C_Z in parallel with C_C),

$$t_{COMP,n} = 3 \bullet R_{Zn} \bullet C_{Zn}$$

where n refers to the channel number.

In case the compensation networks are only type 1 (single capacitor), then:

$$t_{COMP,n} = 3 \bullet 650\Omega \bullet C_{Zn}$$

Thus, the maximum COMP discharge time required can be computed as:

$$t_{COMP,max} = max\ (t_{COMP1}, t_{COMP2}, t_{COMP3})$$

The second is the time required for the inductors to completely discharge following a short circuit. This time can be computed as:

$$t_{IND,N} = \frac{\pi}{4}\sqrt{L_N \bullet C_{ON}}$$

where L and C_O are the input inductor and output capacitor of each power stage.

Thus, the maximum time required to discharge the inductors can be computed as:

$$t_{ind,max} = max\ (t_{ind1},\ t_{ind2},\ t_{ind3})$$

The hiccup time is then chosen as:

$$t_{hiccup} > max\ (t_{COMP,max},\ t_{ind,max})$$

False Triggering of the Short Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string causes a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short circuit comparator, it will cause the IC to falsely detect an over current condition and shut down.

In the HV9982, to prevent these false triggerings, there is a built in 500ns blanking network for the short circuit comparator. This blanking network is activated when the PWMD input goes high. Thus, the short circuit comparator will not see the spike in the LED current during the PWM Dimming turn-on transition. Once the blanking timer is completed, the short circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short circuit will depend on the condition of the PWMD input.

If the output short circuit exists before the PWM dimming signal goes high, the total detection time will be:

$$t_{detect1} = t_{BLANK} + t_{DELAY} \approx 950ns(max)$$

If the short circuit occurs when the PWM dimming signal is already high, the time to detect will be:

$$t_{detect1} = t_{DELAY} \approx 250ns(max)$$

Over Voltage Protection

The HV9982 provides hysteretic over voltage protection allowing the IC to recover in case the LED load is momentarily disconnected.

When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, the HV9982 detects an over voltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the falling OVP threshold (which is 10% lower than the rising threshold). This time is mostly dictated by the R-C time constant of the output capacitor C_O and the resistor network used to sense over voltage (R_{OVP1}+ R_{OVP2}). In case of a persistent open circuit condition, this cycle keeps repeating maintaining the output voltage within a 10% band.

In most designs, the lower threshold voltage of the over voltage protection (V_{OVP} – 10%) at which point the HV9982 attempts to restart will be more than the LED string voltage. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage will cause a spike in the output current. This causes a short circuit to be detected and the HV9982 will trigger short circuit protection. This behavior continues till the output voltage becomes lower than the LED string voltage at which point, no fault will be detected and normal operation of the circuit will commence.

Layout Considerations

For multi-channel peak current mode controller IC to work properly with minimum interference between the channels, it is important to have a good PCB layout which minimizes noise. Following the layout rules stated below will help to ensure proper performance of all three channels.

1. **GND connection**
   The IC has four separate ground connections – one for each of the three channels and one analog ground for the common circuitry. It is recommended that four separate ground planes be used in the PCB and all the GND planes be connected together at the return terminal of the input power lines.

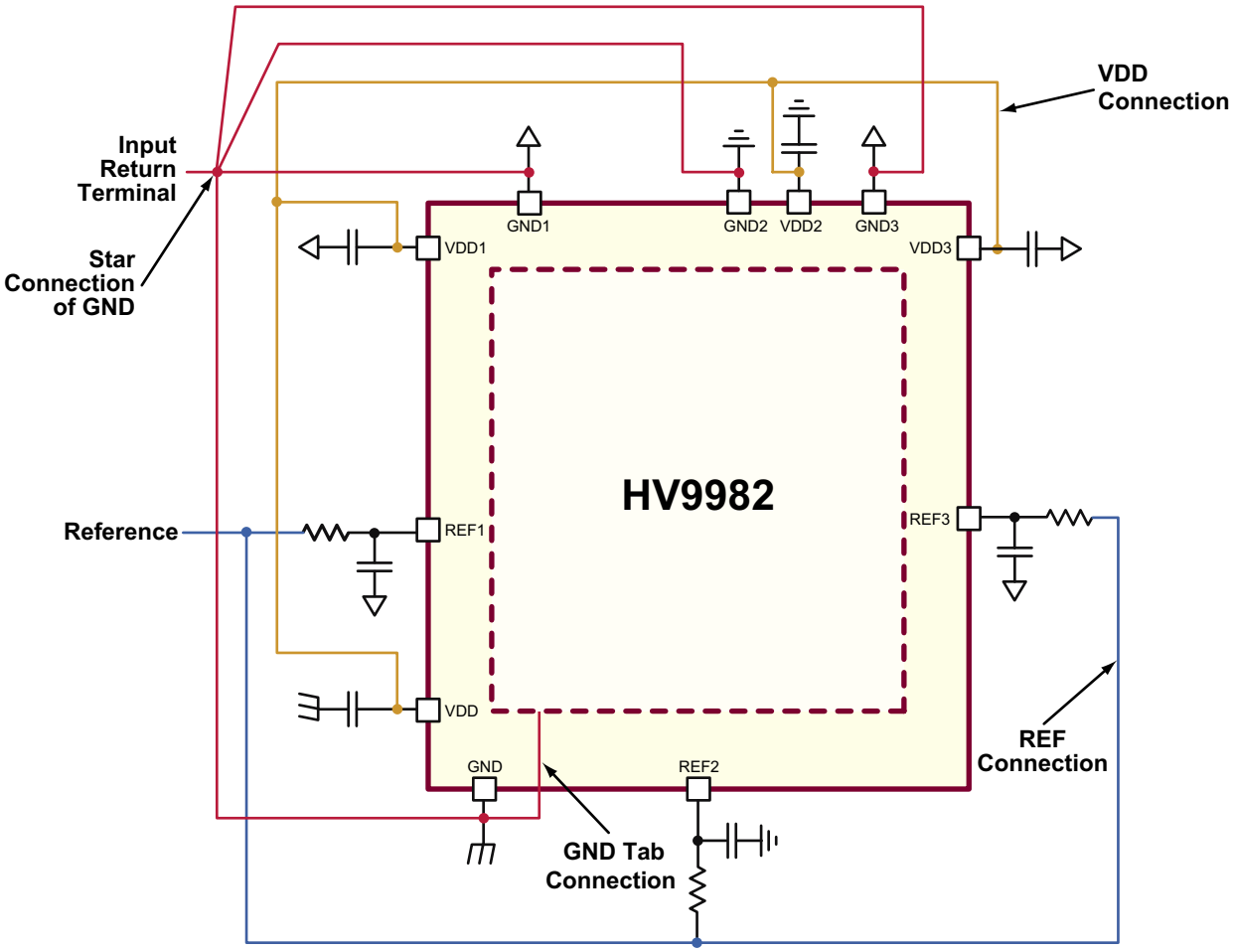
2. **VDD Connection**
   Each VDD pin should be by passed with a low ESR capacitor to its OWN ground (i.e. VDD1 is bypassed to GND1 and so on). The common VDD pin can be bypassed to the common GND.

3. **REF Connection**
   In case all the references are going to be driven from a single voltage source, it is recommended to have a small R-C low pass filter (1.0k, 1.0nF) at each REF pin with the filter being referenced to the appropriate channel's ground (as in the case of the VDD pins). If the REF pins are driven with three individual voltage sources, then just a small capacitor (1.0nF) at each pin would suffice.

4. **GATE and CS connection**
   The connection from GATE output to the gate of the external FET as well as the connection from the CS pin to the external sense resistor made as short as possible to avoid false triggering.

5. **OVP protection**
   Typically, the OVP resistor dividers would be located away from the IC. To prevent false triggering of the IC due to noise at the OVP pin, a small bypass capacitor (1.0nF) right at the OVP pin is recommended.

Layout Guidelines



Pin Description

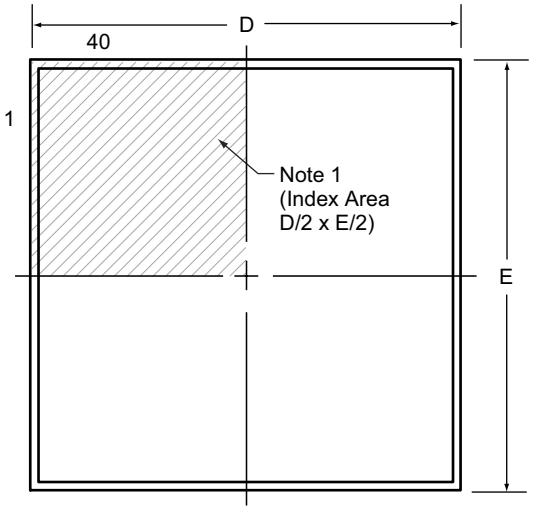
Pin #	Name	Description
1	VDD1	Power supply pin for channel 1. It can either be connected to the VDD pin or supplied with an external power supply. It must be bypassed with a low ESR capacitor to GND1 (at least 0.1µF). All VDD pins (VDD, VDD1-3) must be connected together externally. An external supply (7.0 – 9.0V) can be connected to these pins to power the IC if the internal regulator is not used.
2	FLT1	Used to drive an external disconnect switch. The disconnect switch is used to protect the LEDs in case of fault conditions and also help to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
3	CS1	Used to sense the source current of the external power FET used with channel 1. It includes a built-in 100ns (min) blanking timer. An R-C network at this pin programs the slope compensation. Refer to the Slope Compensation section for additional information.
4	COMP1	Stable closed loop control for channel 1 can be accomplished by connecting a compensation network between each COMP1 pin and GND1.
5	FDBK1	Output current feedback input for channel 1. It receives a voltage signal from an external sense resistor.
6	REF1	The voltage at this pin sets the output current level for channel 1. Recommended voltage range for this pin is 0 – 1.25V.
7	OVP1	Provides the over voltage protection for the channel 1. When the voltage at this pin exceeds 5.0V, the HV9982 is turned off and the fault timer starts. Upon completion of the fault timer the IC attempts to restart.
8	VIN	Input of the internal 40V linear regulator.
9	VDD	Output of the linear regulator. It maintains a regulated 7.75V as long as the voltage of the VIN pin is between 10 and 40V. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF). Can be used as a power supply for the three channels.
10	EN	When pin is pulled below 0.8V, the IC goes into a standby mode and draws minimal current.
11	GND	Ground connection for the common circuitry in the HV9982.
12	COMP2	Stable closed loop control for channel 2 can be accomplished by connecting a compensation network between each COMP2 pin and GND2.
13	REF2	The voltage at this pin sets the output current level for channel 2. Recommended voltage range for this pin is 0 – 1.25V.
14	OVP2	Provides the over voltage protection for the channel 2. When the voltage at this pin exceeds 5.0V, the HV9982 is turned off and the fault timer starts. Upon completion of the fault timer the IC attempts to restart.
15	SKIP	Programs the hiccup timer for fault conditions. A capacitor to GND programs the hiccup time.
16	RAMP	Provides a ramp signal which is used while dimming the channels with pulse-width modulation with an analog input. A capacitor to GND programs the PWM dimming frequency.
17	PWMD1	PWM dimming of the three channels is accomplished by using the PWMD pins. If S1 is LOW, then the three pins directly control the PWM dimming of the three channels and a square wave input should be applied at these pins. If S1 is high, then a 0 – 2.0V analog signal should be applied at these pins. The PWM dimming is then done by comparing the analog voltage to the voltage at the RAMP pin.
18	PWMD2	
19	PWMD3	
20	S1	Digital input pins which select the operating mode of the PWMD inputs. Refer to the PWM dimming section for additional information.
21	S2	

Pin Description *(cont.)*

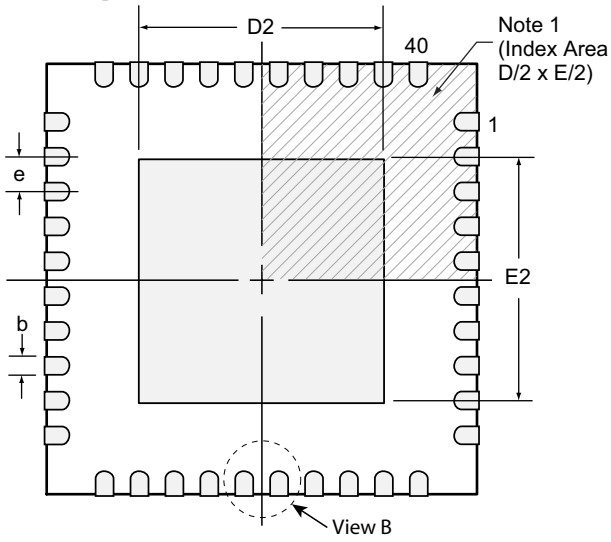
Pin #	Name	Description
22	NC	No connect.
23	CLK	Clock input for the HV9982. The input to the CLK pin should be a TTL compatible square wave signal. The three channels will switch at 1/12th the switching frequency of the signal applied at the CLK pin.
24	OVP3	Provides the over voltage protection for the channel 3. When the voltage at this pin exceeds 5.0V, the HV9982 is turned off and the fault timer starts. Upon completion of the fault timer the IC attempts to restart.
25	REF3	The voltage at this pin sets the output current level for channel 3. Recommended voltage range for this pin is 0 – 1.25V.
26	FDBK3	Output current feedback input for channel 3. It receives a voltage signal from an external sense resistor.
27	COMP3	Stable closed loop control for channel 3 can be accomplished by connecting a compensation network between each COMP3 pin and GND3.
28	CS3	Used to sense the source current of the external power FET used with channel 3. It includes a built-in 100ns (min) blanking timer. An R-C network at this pin programs the slope compensation. Refer to the Slope Compensation section for additional information.
29	FLT3	Used to drive an external disconnect switch. The disconnect switch is used to protect the LEDs in case of fault conditions and also help to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
30	VDD3	Power supply pin for channel 3. It can either be connected to the VDD pin or supplied with an external power supply. It must be bypassed with a low ESR capacitor to GND3 (at least 0.1µF). All VDD pins (VDD, VDD1-3) must be connected together externally. An external supply (7.0 – 9.0V) can be connected to these pins to power the IC if the internal regulator is not used.
31	GATE3	Output gate drive for an external N-channel power MOSFET.
32	GND3	Ground return for channel 3. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
33	VDD2	Power supply pin for channel 2. It can either be connected to the VDD pin or supplied with an external power supply. It must be bypassed with a low ESR capacitor to GND2 (at least 0.1µF). All VDD pins (VDD, VDD1-3) must be connected together externally. An external supply (7.0 – 9.0V) can be connected to these pins to power the IC if the internal regulator is not used.
34	GND2	Ground return for channel 2. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
35	GATE2	Output gate drive for an external N-channel power MOSFET.
36	FLT2	Used to drive an external disconnect switch. The disconnect switch is used to protect the LEDs in case of fault conditions and also help to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
37	CS2	Used to sense the source current of the external power FET used with channel 2. It includes a built-in 100ns (min) blanking timer. An R-C network at this pin programs the slope compensation. Refer to the Slope Compensation section for additional information.
38	FDBK2	Output current feedback input for channel 2. It receives a voltage signal from an external sense resistor.
39	GND1	Ground return for channel 1. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
40	GATE1	Output gate drive for an external N-channel power MOSFET.

40-Lead QFN Package Outline (K6)

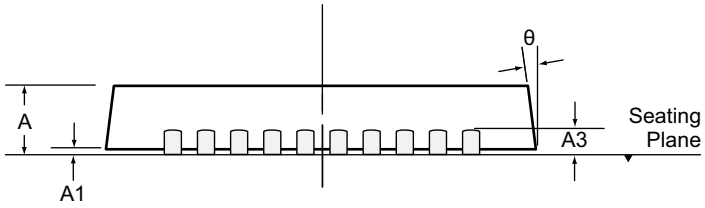
6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



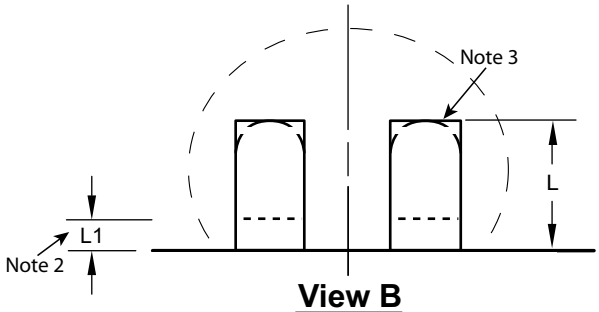
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85*	1.05	5.85*	1.05	0.50 BSC	0.30†	0.00	0
	NOM	0.90	0.02		0.25	6.00	-	6.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	6.15*	4.45	6.15*	4.45		0.50†	0.15	14

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-40QFNK66X6P050, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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