40-Channel Symmetric Row Driver

Features

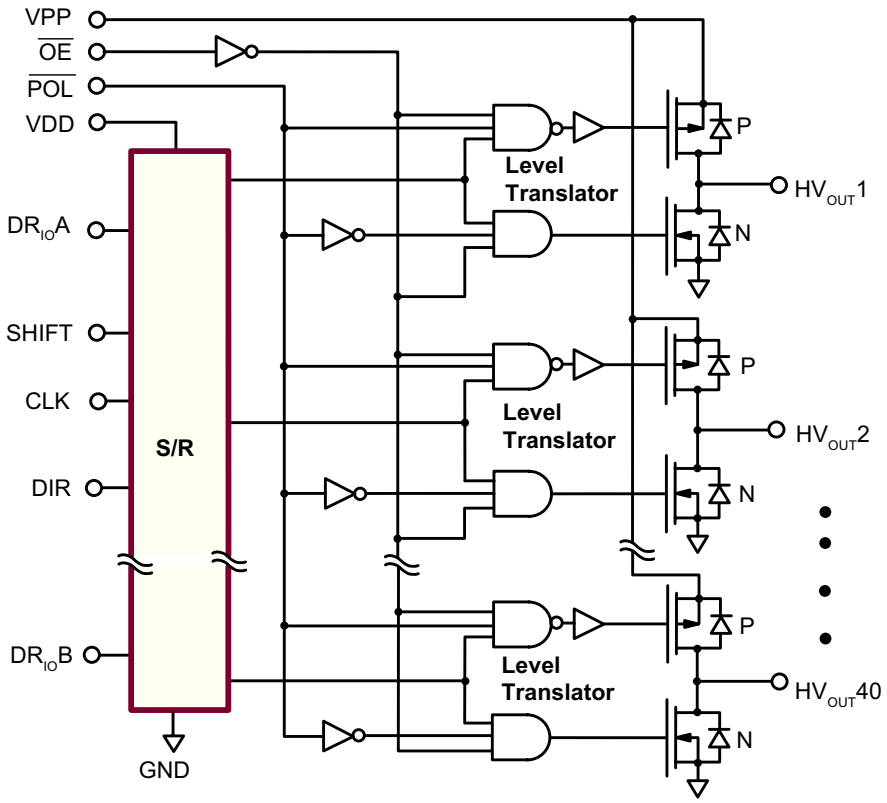
- HVCMOS® technology
- Symmetric row drive (reduces latent imaging in ACTFEL displays)
- Output voltage up to +240V
- Low power level shifting
- Source/sink current minimum 70mA
- Shift register speed 3.0MHz
- Pin-programmable shift direction (DIR, SHIFT)

General Description

The HV7224 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. It is especially suitable for use as a symmetric row driver in AC thin-film electroluminescent (ACTFEL) displays.

When the data reset pin ($DR_{IO}A/DR_{IO}B$) is at logic high, it will reset all the outputs of the internal shift register to zero. At the same time, the output of the shift register will start shifting a logic high from the least significant bit to the most significant bit. The $DR_{IO}A/DR_{IO}B$ can be triggered at any time. The DIR and SHIFT pins control the direction of data shift through the device. When DIR is at logic high, $DR_{IO}A$ is the input and $DR_{IO}B$ is the output. When DIR is grounded, $DR_{IO}B$ is the input and the $DR_{IO}A$ is the output. See the Output Sequence Operation Table for output sequence. The $\overline{POL}$ and $\overline{OE}$ pins perform the polarity select and output enable function respectively. Data is loaded on the low to high transition of the clock. A logic high will cause the output to swing to VPP if $\overline{POL}$ is high, or to GND if $\overline{POL}$ is low. All outputs will be in High-Z state if $\overline{OE}$ is at logic high. Data output buffers are provided for cascading devices.

Functional Block Diagram



Ordering Information

Device	Package Option
	64-Lead PQFP (3-sided) *20.00x14.00mm body* *3.40mm height (max)* *0.80mm pitch* *3.90mm footprint*
HV7224	HV7224PG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

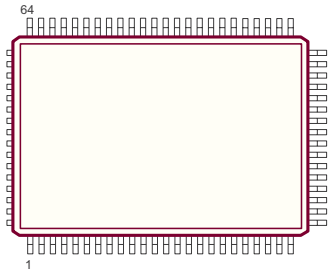
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +7.0V
Supply voltage , V_{PP}	-0.5V to +260V
Logic input levels	-0.5V to V_{DD} + 0.5V
Continuous total power dissipation[1]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm from case for 10 seconds	260°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note:

1. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.*

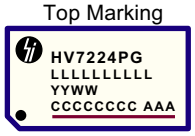
Pin Configuration



64-Lead PQFP (3-sided) (PG)
(top view)

Product Marking

Top Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

64-Lead PQFP (3-sided) (PG)

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	High voltage supply[1]	0	240	V
V_{IH}	High-level input voltage	0.7 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage	0	0.2V_{DD}	V
f_{CLK}	Clock frequency	-	3.0	MHz
T_A	Operating free-air temperature	-40	+85	°C
I_O	High voltage output current	-	±70	mA
I_{OD}	Allowable pulsed current through output diode	-	±300	mA

Note:

1. *Output will not switch at V_{PP} = 0V.*

Power-up sequence should be the following:

1. *Connect ground.*
2. *Apply V_{DD}.*
3. *Set all inputs (Data, CLK, Enable, etc.) to a known state.*
4. *Apply V_{PP}.*

The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics

(over recommended operating conditions of V_{DD} = 5.0V, V_{PP} = 240V, and T_A = 25°C unless noted)

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	10	mA	f_{CLK} = 3.0MHz, V_{DD} = 5.5V
I_{PP}	V_{PP} supply current		-	2.0	mA	All outputs low or High-Z
			-	4.0	mA	One output high[1]
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All V_{IN} = GND or V_{DD}
V_{OH}	High-level output	HV_{OUT}	190	-	V	I_O = -70mA
		DATA OUT	4.5	-	V	I_O = -100µA
V_{OL}	Low-level output	HV_{OUT}	-	50	V	I_O = +70mA
		DATA OUT	-	0.5	V	I_O = +100µA
I_{IH}	High-level logic input current		-	1.0	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current		-	-1.0	µA	V_{IL} = 0V
I_{SAT}	HV_{OUT} saturation current	P-channel	-80	-	mA	---
		N-channel	75	-	mA	---

Note:

1. *Only one output can be turned on at a time.*

AC Electrical Characteristics

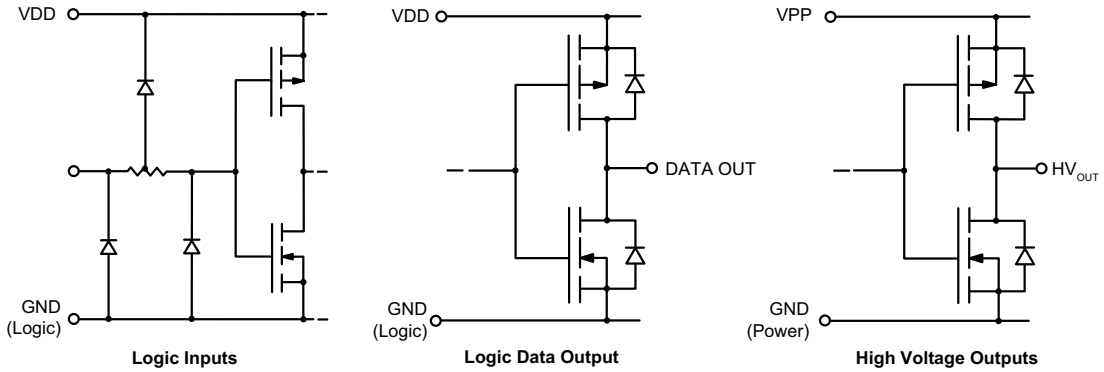
(V_{DD} = 5.0V and T_A = 25°C)

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	3.0	MHz	Per register, C_L = 15pF
t_{WH}, t_{WL}	Clock width high or low	150	-	ns	---
t_{SUD}	Data set-up time before clock rises	50	-	ns	---
t_{HD}	Data hold time after clock rises	50	-	ns	---
t_{SUC}	HV_{OUT} delay from clock rises (Hi-Z to H or L)	-	1.0	µs	C_L = 330pF // R_L = 10kΩ
t_{SUE}	HV_{OUT} delay from $\overline{\text{Output Enable}}$ falls	-	600	ns	C_L = 330pF // R_L = 10kΩ
t_{HC}	HV_{OUT} delay from clock rises (H or L to Hi-Z)	-	2.0	µs	C_L = 330pF // R_L = 10kΩ
t_{HE}	HV_{OUT} delay from $\overline{\text{Output Enable}}$ rises	-	600	ns	C_L = 330pF // R_L = 10kΩ
t_{DHL}	Delay time clock to data output falls*	-	250	ns	C_L = 15pF
t_{DLH}	Delay time clock to data output rises*	-	250	ns	C_L = 15pF
t_{ONF}	HV_{OUT} fall time	-	2.0	µs	C_L = 330pF // R_L = 10kΩ
t_{ONR}	HV_{OUT} rise time	-	2.0	µs	C_L = 330pF // R_L = 10kΩ
t_{POW}	$\overline{\text{POL}}$ pulse width	3.0	-	µs	---
t_{OEW}	$\overline{\text{Output Enable}}$ pulse width	3.0	-	µs	---
SR	Slew rate, V_{PP}	-	45	V/µs	One active output driving 4.7nF load

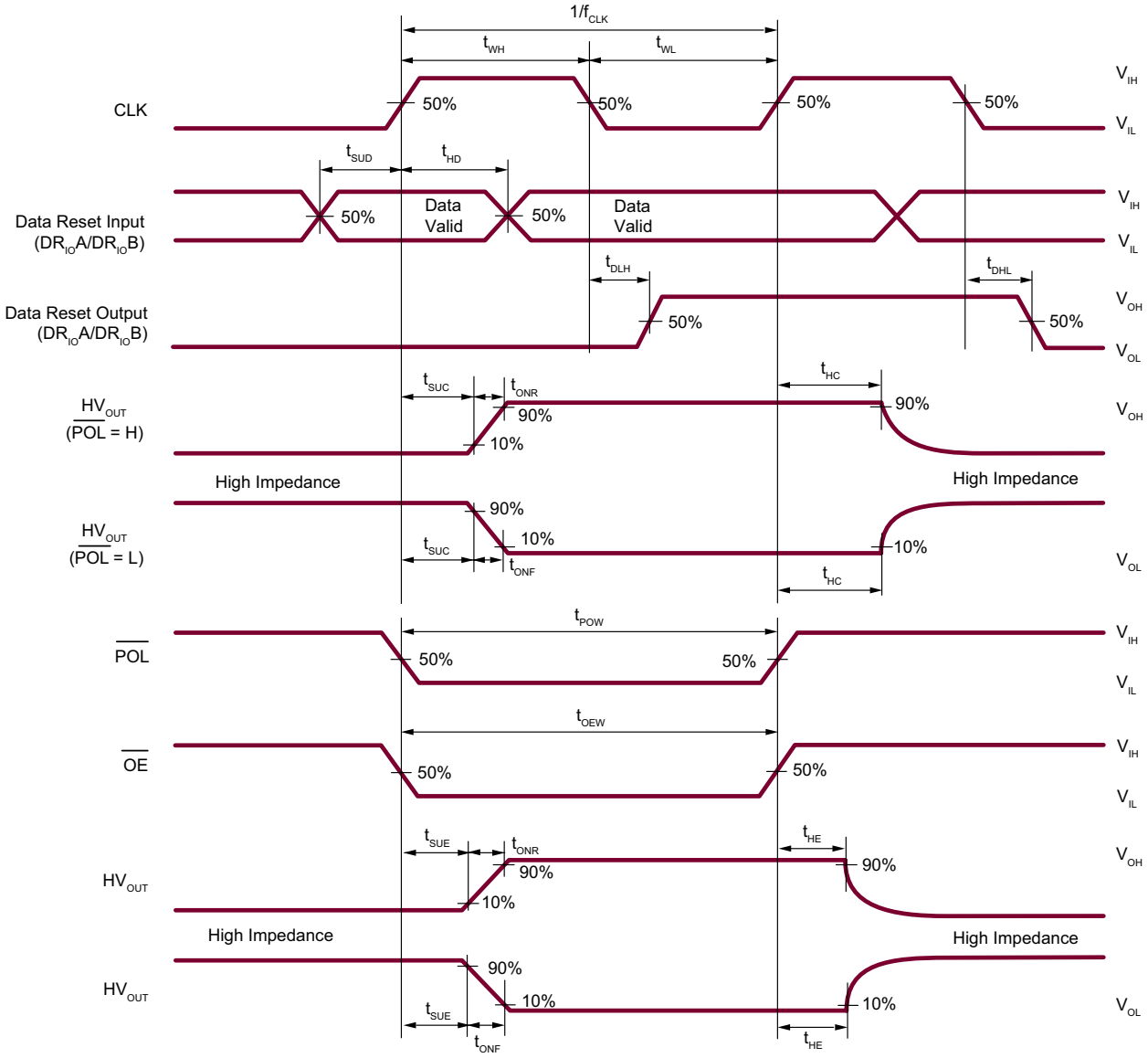
Note:

** The delay is measured from the trailing edge of the clock but the data is triggered by the rising edge of the clock. There is an internal delay for the data output which is equal to t_{WH}.*

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

I/O Relations	Inputs					HV Outputs
	CLK	DIR	S/R DATA	$\overline{POL}$	$\overline{OE}$	
O/P HIGH	X	X	H	H	L	H
O/P OFF	X	X	L	X	L	HIGH-Z
O/P LOW	X	X	H	L	L	L
O/P OFF	X	X	X	X	H	All O/P HIGH-Z

Notes:

H = logic high level, L = logic low level, X = irrelevant

Data input (DR_{IO}) loaded on the low-to-high transition of the clock.

Only one active output can be set at a time.

Output Sequence Operation Table

DIR	SHIFT	Data Reset In	Data Reset Out	HV_{OUT} # Sequence	Direction*
L	L	$DR_{IO}B$	$DR_{IO}A^{1}$	40 → 1	
H	L	$DR_{IO}A$	$DR_{IO}B^{2}$	1 → 40	
L	H	$DR_{IO}B$	$DR_{IO}A^{1}$	20 → 1 → 40 → 21	
H	H	$DR_{IO}A$	$DR_{IO}B^{2}$	21 → 40 → 1 → 20	

Notes:

* *Reference to package outline or chip layout drawing.*

1. *$DR_{IO}A$ is $DR_{IO}B$ delayed by 40 clock pulses.*
2. *$DR_{IO}B$ is $DR_{IO}A$ delayed by 40 clock pulses.*

Pin Descriptions - 64-Lead PQFP (3-sided) (PG) Option A

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HV_{OUT}1/40	17	HV_{OUT}17/24	33	N/C	49	HV_{OUT}25/16
2	HV_{OUT}2/39	18	HV_{OUT}18/23	34	DR_{IO}B	50	HV_{OUT}26/15
3	HV_{OUT}3/38	19	HV_{OUT}19/22	35	$\overline{OE}$	51	HV_{OUT}27/14
4	HV_{OUT}4/37	20	HV_{OUT}20/21	36	N/C	52	HV_{OUT}28/13
5	HV_{OUT}5/36	21	VPP	37	$\overline{POL}$	53	HV_{OUT}29/12
6	HV_{OUT}6/35	22	N/C	38	N/C	54	HV_{OUT}30/11
7	HV_{OUT}7/34	23	GND (Power)	39	VDD	55	HV_{OUT}31/10
8	HV_{OUT}8/33	24	GND (Logic)	40	N/C	56	HV_{OUT}32/9
9	HV_{OUT}9/32	25	DIR	41	GND (Logic)	57	HV_{OUT}33/8
10	HV_{OUT}10/31	26	VDD	42	GND (Power)	58	HV_{OUT}34/7
11	HV_{OUT}11/30	27	CLK	43	N/C	59	HV_{OUT}35/6
12	HV_{OUT}12/29	28	N/C	44	VPP	60	HV_{OUT}36/5
13	HV_{OUT}13/28	29	SHIFT	45	HV_{OUT}21/20	61	HV_{OUT}37/4
14	HV_{OUT}14/27	30	N/C	46	HV_{OUT}22/19	62	HV_{OUT}38/3
15	HV_{OUT}15/26	31	DR_{IO}A	47	HV_{OUT}23/18	63	HV_{OUT}39/2
16	HV_{OUT}16/25	32	N/C	48	HV_{OUT}24/17	64	HV_{OUT}40/1

Note:

Pin designation for DIR H/L, Shift = L

Example: For DIR = H, pin 1 is HV_{OUT}1

For DIR = L, pin 1 is HV_{OUT}40

Pin Descriptions - 64-Lead PQFP (3-sided) (PG) Option B

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HV_{OUT}20/21	17	HV_{OUT}4/37	33	N/C	49	HV_{OUT}36/5
2	HV_{OUT}19/22	18	HV_{OUT}3/38	34	DR_{IO}B	50	HV_{OUT}35/6
3	HV_{OUT}18/23	19	HV_{OUT}2/39	35	$\overline{OE}$	51	HV_{OUT}34/7
4	HV_{OUT}17/24	20	HV_{OUT}1/40	36	N/C	52	HV_{OUT}33/8
5	HV_{OUT}16/25	21	VPP	37	$\overline{POL}$	53	HV_{OUT}32/9
6	HV_{OUT}15/26	22	N/C	38	N/C	54	HV_{OUT}31/10
7	HV_{OUT}14/27	23	GND (Power)	39	VDD	55	HV_{OUT}30/11
8	HV_{OUT}13/28	24	GND (Logic)	40	N/C	56	HV_{OUT}29/12
9	HV_{OUT}12/29	25	DIR	41	GND (Logic)	57	HV_{OUT}28/13
10	HV_{OUT}11/30	26	VDD	42	GND (Power)	58	HV_{OUT}27/14
11	HV_{OUT}10/31	27	CLK	43	N/C	59	HV_{OUT}26/15
12	HV_{OUT}9/32	28	N/C	44	VPP	60	HV_{OUT}25/16
13	HV_{OUT}8/33	29	SHIFT	45	HV_{OUT}40/1	61	HV_{OUT}24/17
14	HV_{OUT}7/34	30	N/C	46	HV_{OUT}39/2	62	HV_{OUT}23/18
15	HV_{OUT}6/35	31	DR_{IO}A	47	HV_{OUT}38/3	63	HV_{OUT}22/19
16	HV_{OUT}5/36	32	N/C	48	HV_{OUT}37/4	64	HV_{OUT}21/20

Note:

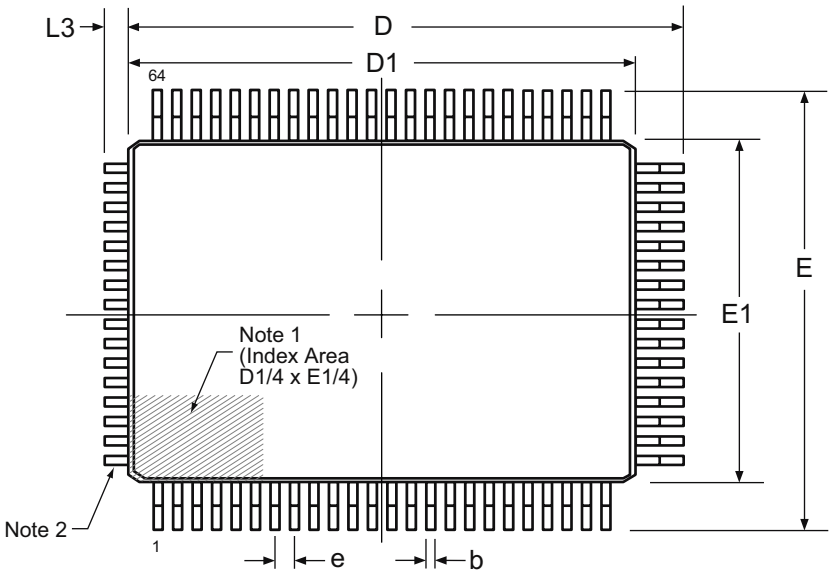
Pin designation for DIR H/L, Shift = H

Example: For DIR = H, pin 1 is HV_{OUT}20

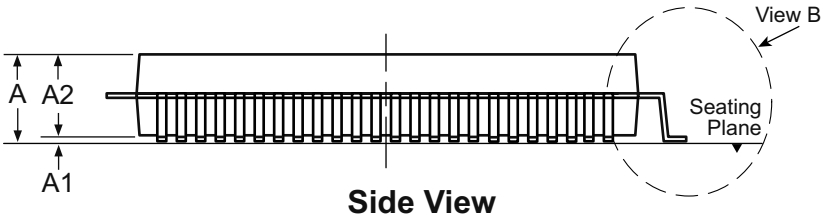
For DIR = L, pin 1 is HV_{OUT}21

64-Lead PQFP (3-sided) Package Outline (PG)

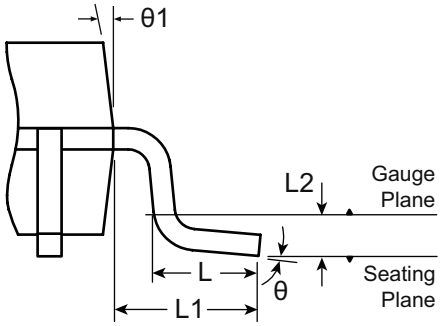
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *The leads on this side are trimmed.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	L3	θ	θ1
Dimension (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0.55 REF	0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		0.88				3.5°	-
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7°	16°

Drawings not to scale.
Supertex Doc. #: *DSPD-64PQFPPG, Version NR090608.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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