Tri-EL Lamp Driver IC

Features

- Tri-EL lamp driver with common terminal
- Independent brightness control for all 3 lamps
- 1.73 - 6.5V operating supply voltage
- Output voltage regulation
- Two-pin serial data communication for control
- Linear brightness control with seven steps at constant efficiency
- 128kHz fixed switching frequency
- Split supply capability
- Patented high efficiency EL lamp driver
- Single miniature inductor drives all 3 lamps
- Only 4 external components
- Burst mode power converter for best efficiency
- CMOS compatible serial interface with noise rejection
- 500nA max. leakage current when disabled
- Power-on reset causes all outputs to be off when first powered up

Applications

- Mulit-segment, variable displays
- Cell phone keypads and displays
- MP3 players

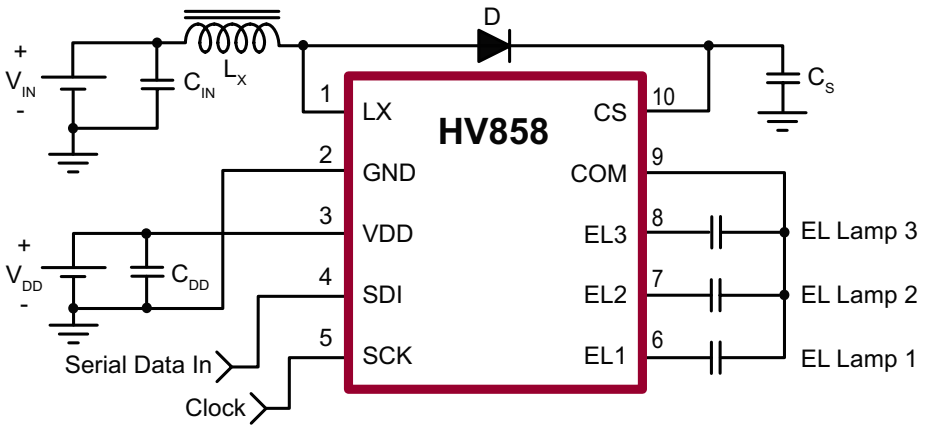
General Description

The Supertex HV858 is a high voltage triple EL lamp driver designed for driving combined EL lamps of up to 3.0in^2 (1.0in^2 each). The input supply voltage range is from 1.73 - 6.5V. The device is designed such that the input voltage to the inductor can be different from the input voltage to the device (split supply). The device uses a single inductor and a minimum number of passive components. The nominal regulated output voltage that is applied to the EL lamp is ±95V. The HV858 has two internal oscillators, one for the internal switching MOSFET, and the other for the high voltage EL lamp driver. The EL lamp frequency is fixed internally at 500Hz. The power converter oscillator runs 256 times faster than the EL lamp driver at 128kHz.

An external inductor is connected between the LX and VDD pins (or between the LX pin and a separate voltage source in the case of a split supply application). A 0.001 - 0.01µF, 100V capacitor is connected between the CS pin and ground. The switching MOSFET charges the external inductor and discharges it into the capacitor at the CS pin. The voltage at the CS pin will start to increase. Once the voltage at the CS pin reaches a nominal value of 95V, the switching MOSFET is turned OFF to conserve power.

One side of the 3 EL lamps is connected to the COM pin of the HV858, the other side to the EL1, EL2, and EL3 pins. Each EL lamp output may be independently controlled to have one of the 7 brightness levels or can be completely turned OFF by a 10-bit serial data input register. The 10-bit control code has 3 bits to control the brightness level of each EL Lamp and one bit to optionally control the power converter. The 3-bit binary brightness control code controls the number of 500Hz cycles (from 0 to 7) in a group of 7 cycles.

Typical Application Circuit

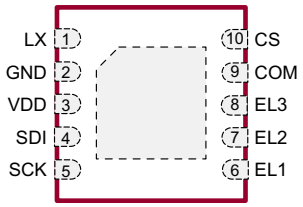


Ordering Information

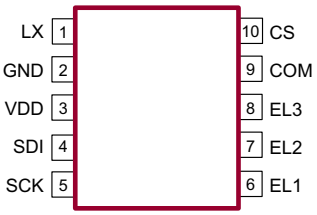
Device	Package Options	
	10-Lead DFN *3.00x3.00mm body* *0.80mm height (max)* *0.50mm pitch*	10-Lead MSOP *3.00x3.00mm body* *1.10mm height (max)* *0.50mm pitch*
HV858	HV858K7-G	HV858MG-G

-G indicates package is RoHS compliant ('Green')

Pin Configurations



10-Lead DFN (K7)
(top view)



10-Lead MSOP (MG)
(top view)

Note:

1. *Bottom side heat slug is at ground potential*
2. *Pads are at the bottom of the package*

Absolute Maximum Ratings

Parameter	Value
V_{DD}, supply voltage	-0.5V to +7.0V
SDI, SCK	-0.5V to +7.0V
V_{CS}, output voltage	0.5V to +115V
I_{SW}	0.7A peak
Power dissipation: 10-Lead DFN 10-Lead MSOP	 1.6W 250mW
Storage temperature	-65°C to +150°C
Operating temperature	-40°C to +85°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
___ = "Green" Packaging

Package may or may not include the following marks: Si or

10-Lead DFN (K7)

Top Marking

Bottom Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
___= "Green" Packaging

Package may or may not include the following marks: Si or

10-Lead MSOP (MG)

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Unit	Conditions
V_{DD}	Supply voltage	1.73	-	6.5	V	---
f_{EL}	EL Lamp frequency	-	-	1.0	kHz	---
$I_{SW(PK)}$	Peak switch current	-	-	0.4	A	---
T_A	Operating temperature	-40	-	85	°C	---

Electrical Characteristics *(unless otherwise specified V_{DD} = 2.6 - 5.5V, T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Unit	Conditions
$R_{DS(ON)}$	On-resistance of switching transistor	-	4.0	6.0	Ω	V_{DD} = 1.73 - 6.5V, I = 100mA
V_{CS}	Output regulation voltage	85	95	105	V	S1...S9 = 0, V_{DD} = 1.73 - 6.5V, no load
V_{LAMP}	Differential lamp voltage	170	190	210	V	V_{COM} to any EL, no load, code[1] = 111
I_{DD}	V_{DD} supply current	-	-	0.25	mA	V_{DD} = 1.73 - 3.30V, V_{CS} = 20V, no load, PWR_ON = 1
		-	-	0.70		V_{DD} = 3.40 - 6.50V, V_{CS} = 20V, no load, PWR_ON = 1
I_{CS}	V_{CS} supply current	10	50	100	µA	V_{CS} = 75V, no load
I_{DDQ}	Quiescent V_{DD} current when disabled	-	-	500	nA	V_{DD} = 1.73 - 3.30V, S1...S9 = 0, SCK and SDI can be tied to V_{DD} or GND
		-	-	2000		V_{DD} = 3.40 - 6.50V, S1...S9 = 0, SCK and SDI can be tied to V_{DD} or GND
f_{SW}	Inductor switching frequency	108.8	128	147.2	kHz	See Fig. 1
f_{EL}	EL Lamp frequency	425	500	575	Hz	For all codes except code[1] = 000
V_{LOW}	Logic pin input low level	-0.5	0	$0.2V_{DD}$	V	---
V_{HIGH}	Logic pin input high level	$0.8V_{DD}$	V_{DD}	V_{DD} +0.5	V	---
I_{LOGIC}	Logic pin input current	-0.1	0	0.1	µA	0 < V_{DD} < 7.0V
I_{IN}	Inductor current	-	56	70	mA	See Fig 1. V_{DD} = V_{IN} = 3V, total lamp size = 3.0in² (1.0in² each) 10-bit SDI serial code = 1111111111
V_{CS}	Output regulation voltage	-	82.5	-	V	
f_{EL}	Lamp frequency	-	500	-	Hz	
D_{MAX}	Maximum PWM switch duty cycle	80	88	94	%	V_{CS} = 20V, R_{LOAD} = 20Ω
f_{CLK}	SCK speed	-	-	1.0	MHz	---
t_{SU}	SDI setup time before SCK rises	30	-	-	ns	---
t_H	SDI hold time before SCK rises	30	-	-	ns	---

Note:

1. Code refers to the 3-bit Brightness Control Code for the respective EL Lamp.

Logic Input Conditions

The serial data input consists of a 10-bit string, 3-bit of brightness control for each lamp and one bit(10th bit) to optionally control the power converter. The power converter runs if any of the EL lamps has a non-zero brightness value or if the PWR_ON bit is high while the other 9 bits are low.

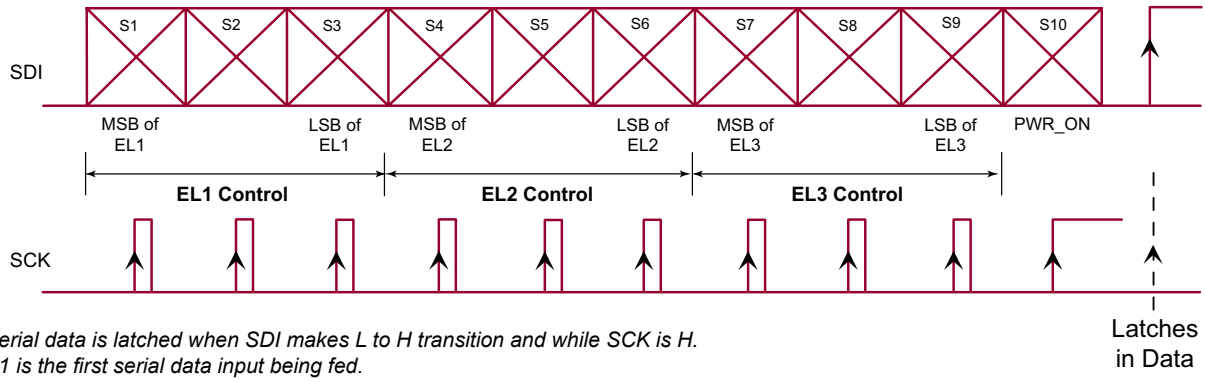
1. SDI may be H or L if SCK is H.
2. SCK may be H or L if SDI is H.
3. While inputting serial data to the shift register, SDI can change value only when SCK is L.
4. The previous 10 bits of serial input will be latched when SDI makes L to H transition while SCK is H.

Logic Input Diagram

The EL Lamp brightness control is a 3-bit binary number stored in a latch, which is provided by a serial to parallel conversion shift register.

1. If all the 3 bits for a designated EL lamp are L, the differential voltage across that lamp will be zero.
2. If any of the 3 bits for a designated EL lamp is H:
   a. The 3-bit value sets the average number of cycles for which the EL lamp voltage is non-zero.
   b. The EL lamp brightness is linearly proportional to the binary lamp control code.

EL lamp Brightness Control



Notes:

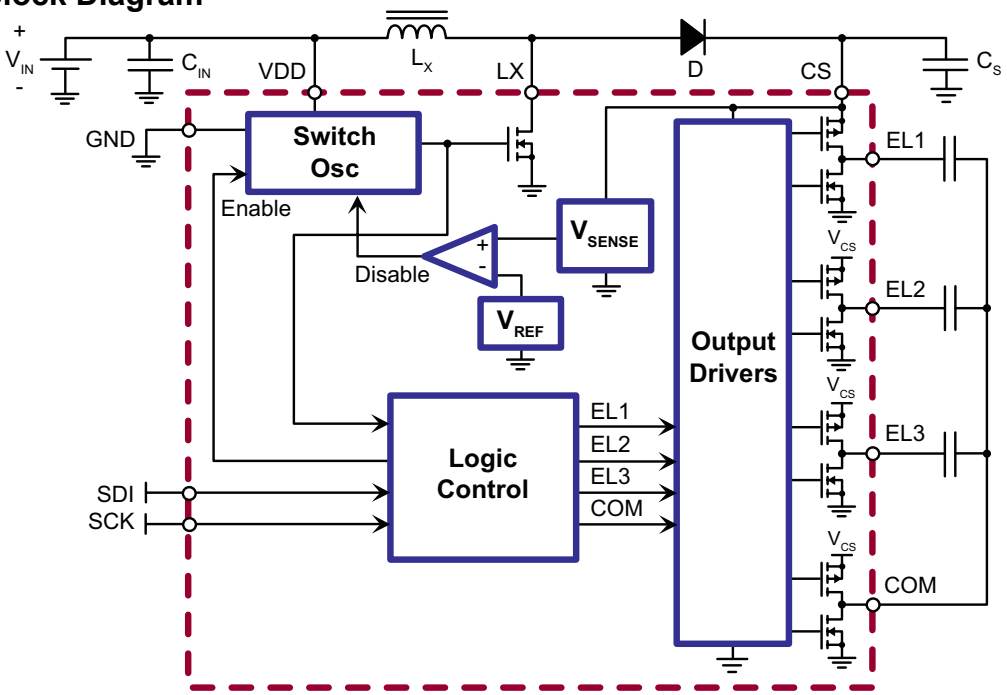
1. *Serial data is latched when SDI makes L to H transition and while SCK is H.*
2. *S1 is the first serial data input being fed.*

Logic Truth Table

	Brightness Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
Device Disabled	All Lamps Off	L	L	L	L	L	L	L	L	L	L
Device Enabled		L	L	L	L	L	L	L	L	L	H
EL1	7/7	H	H	H	NA	NA	NA	NA	NA	NA	NA
	6/7	H	H	L	NA	NA	NA	NA	NA	NA	NA
	5/7	H	L	H	NA	NA	NA	NA	NA	NA	NA
	4/7	H	L	L	NA	NA	NA	NA	NA	NA	NA
	3/7	L	H	H	NA	NA	NA	NA	NA	NA	NA
	2/7	L	H	L	NA	NA	NA	NA	NA	NA	NA
	1/7	L	L	H	NA	NA	NA	NA	NA	NA	NA
	OFF	L	L	L	NA	NA	NA	NA	NA	NA	NA
EL2	7/7	NA	NA	NA	H	H	H	NA	NA	NA	NA
	6/7	NA	NA	NA	H	H	L	NA	NA	NA	NA
	5/7	NA	NA	NA	H	L	H	NA	NA	NA	NA
	4/7	NA	NA	NA	H	L	L	NA	NA	NA	NA
	3/7	NA	NA	NA	L	H	H	NA	NA	NA	NA
	2/7	NA	NA	NA	L	H	L	NA	NA	NA	NA
	1/7	NA	NA	NA	L	L	H	NA	NA	NA	NA
	OFF	NA	NA	NA	L	L	L	NA	NA	NA	NA
EL3	7/7	NA	NA	NA	NA	NA	NA	H	H	H	NA
	6/7	NA	NA	NA	NA	NA	NA	H	H	L	NA
	5/7	NA	NA	NA	NA	NA	NA	H	L	H	NA
	4/7	NA	NA	NA	NA	NA	NA	H	L	L	NA
	3/7	NA	NA	NA	NA	NA	NA	L	H	H	NA
	2/7	NA	NA	NA	NA	NA	NA	L	H	L	NA
	1/7	NA	NA	NA	NA	NA	NA	L	L	H	NA
	OFF	NA	NA	NA	NA	NA	NA	L	L	L	NA

L = Low (L = 0 to L< 20% of V_{DD}), H = High (80% of V_{DD} < H = V_{DD}), NA = Does not control brightness of the designated EL Lamp

Functional Block Diagram



Note:
This drawing is a generalized representation. Actual internal circuitry may differ.

Differential Output Waveform

The following is the differential output waveform across the lamp for each 3-bit input code for each lamp.

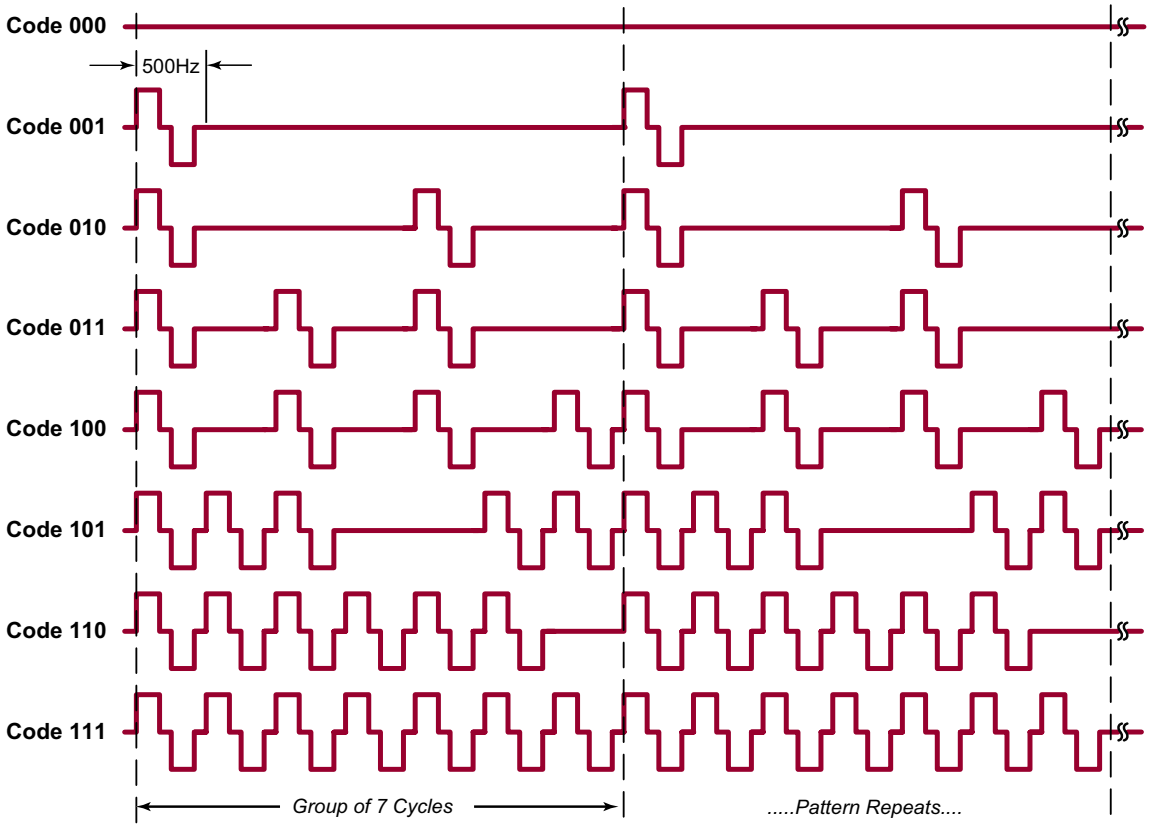
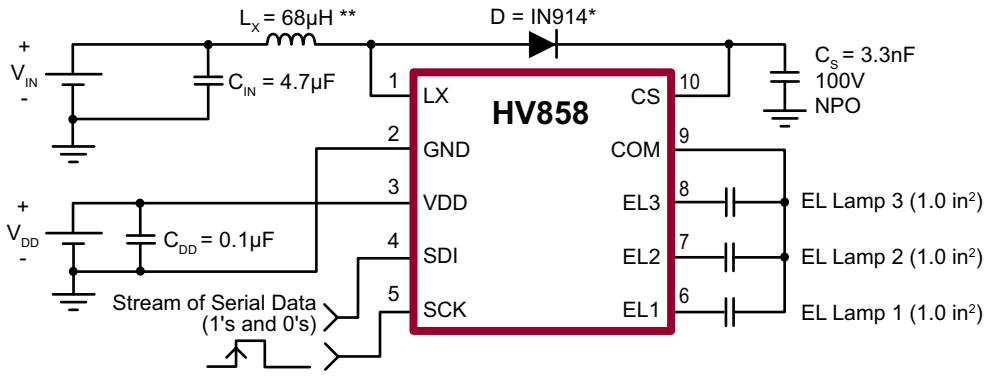


Fig. 1: Test Circuit



* *Any 100V fast reverse recovery diode can be used*
** *68µH Murata LQH32CN680*

Note:
The maximum lamp size for each segment is 1.0in². To drive larger size lamps, any combination of EL1, EL2 and EL3 can be paralleled. However, the 3-bit serial data input code (for each output) should be such that the paralleled outputs have the same code.

Typical Performance (V_{DD} = V_{IN} = 3.0V)

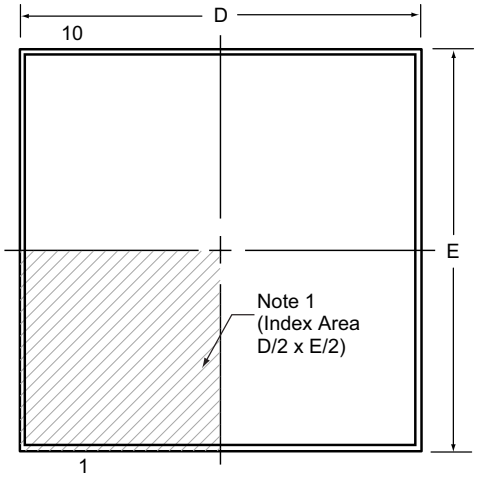
1ST 9-bit SDI Code	EL1 Brightness			I_{IN} (mA)	V_{CS} (V)
	Level	ft-lm	Cd/m²		
000111111	0/7	0	0	42.6	85.7
001111111	1/7	1.60	5.46	44.7	85.3
010111111	2/7	3.24	11.08	46.9	84.9
011111111	3/7	4.95	16.94	48.9	84.5
100100100	4/7	6.68	22.85	51.2	84.0
101111111	5/7	8.44	28.85	53.3	83.5
110111111	6/7	10.21	34.93	55.0	82.9
111111111	7/7	12.05	41.20	56.2	82.5

Pin Description

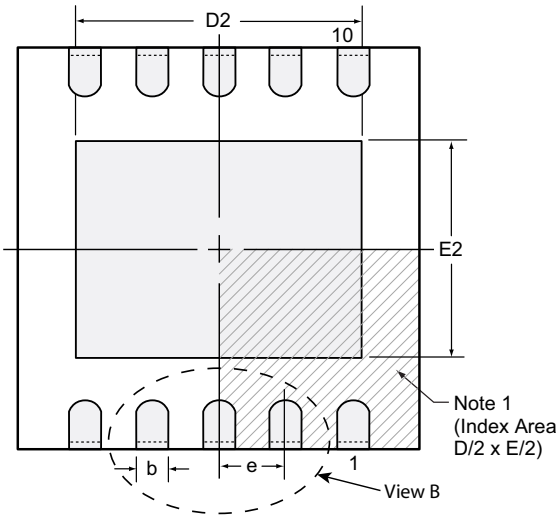
Pin	Name	Description
1	LX	Inductor pin.
2	GND	Ground pin.
3	VDD	Input voltage supply pin. It is a common practice to use a bypass capacitor as close as possible to the device on this pin.
4	SDI	Serial data input pin.
5	SCK	Serial clock input pin.
6	EL1	EL Lamp 1 pin.
7	EL2	EL Lamp 2 pin.
8	EL3	EL Lamp 3 pin.
9	COM	Common pin for one side of all 3 EL Lamps.
10	CS	High voltage capacitor pin.

10-Lead DFN Package Outline (K7)

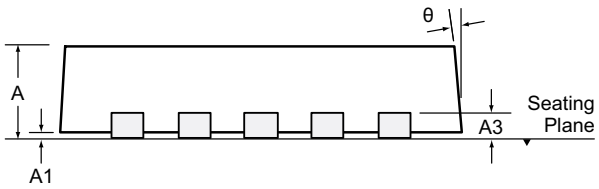
3.00x3.00mm body, 0.80mm height (max), 0.50mm pitch



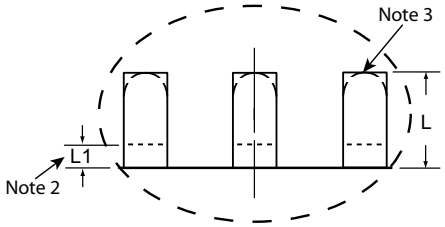
Top View



Bottom View



Side View



View B

Notes:

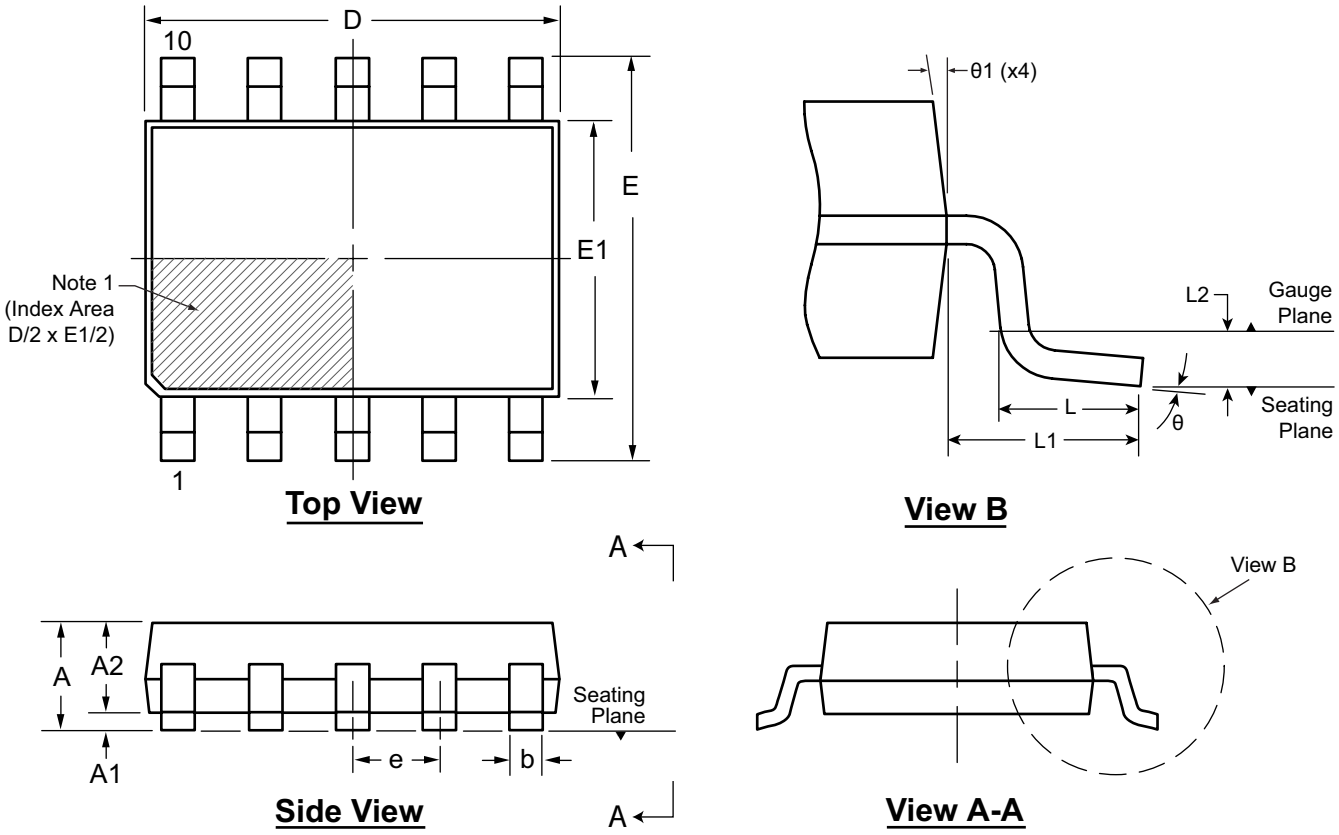
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	2.85*	2.20	2.85*	1.40	0.50 BSC	0.30	0.00*	0°
	NOM	0.75	0.02		0.25	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.30	3.15*	2.70	3.15*	1.75		0.50	0.15	14°

JEDEC Registration MO-229, Variation WEED-5, Issue C, Aug. 2003.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
Supertex Doc.#: *DSPD-10DFNK73X3P050, Version D041309.*

10-Lead MSOP Package Outline (MG)

3.00x3.00mm body, 1.10mm height (max), 0.50mm pitch



Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.75*	0.00	0.75	0.17	2.80*	4.65*	2.80*	0.50 BSC	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00		0.60			-	-
	MAX	1.10	0.15	0.95	0.33	3.20*	5.15*	3.20*		0.80			8°	15°

JEDEC Registration MO-187, Variation BA, Issue E, Dec. 2004.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-10MSOPMG, Version F041309*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com