CMD-5xx

Development Board for the Motorola MPC5xx Series Microcontrollers

Versions CMD-555, CMD560 - 566

Users Manual

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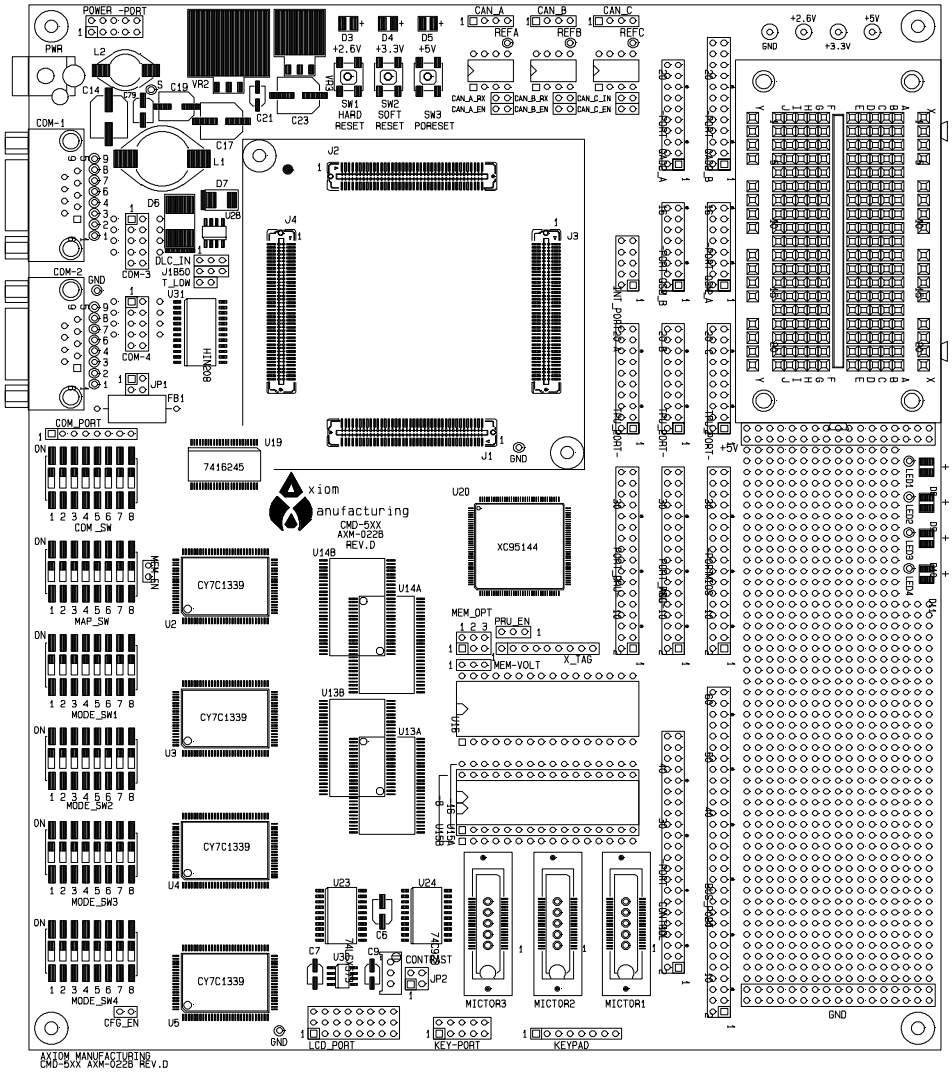
Features

The CMD-5xx along with a PM-5xx Personality Module is a modular development system for the Motorola series of MPC5xx PowerPC microcontrollers. The system is Plug and Play with the supplied with the Axiom Monitor in the on-board EPROM, 2MByte (512K x 32) Synchronous SRAM, 4MByte (1M x 32) Burstable Flash EPROM, Communication Interfaces, Port Replacement Unit, Keypad and LCD Module support, Serial Cable, Wall Plug power source, printed hardware manual and the UTL5xx CD with programming utilities, support software and technical manuals. Applications developed on the CMD-5xx are directly portable to the PMP-xxx peripheral support boards for in-system industrial control solutions.



Specifications

Clock	50 MHz Maximum
Operating temperature	0°C to +70°C
Power requirement	6 - 20V DC @ 400 ma Typical
Power output	5.8V @ 2.5A output with 5V, 3.3V, and 2.6V regulated supplies
Board Size	8 x 9.5 inches

Standard Configurations

Board	*Processor*	*Board*	*Processor*	*Board*	*Processor*
CMD-555	MPC555	CMD-562	MPC562	CMD-565	MPC565
CMD-556	MPC556	CMD-563	MPC563	CMD-566	MPC566
CMD-561	MPC-561	CMD-564	MPC564	CMD-560	MGT560

Example part number: CMD-565 would be the CMD-5xx board with the PM-565 Personality Module that has a socketed processor, AMD flash, and the global power source.

CMD-5xx Features

- Standard fixed memory (buffered):
- 512K x 32 Sync. SRAM (100MHz)
- 1M x 32 Burstable Flash EPROM
- Two Configurable 32pin memory sockets for 32K to 2MByte EPROM with 8 or 16 bit wide data bus, Axiom Monitor installed standard.
- PRU - Port Replacement Unit provided for MPC5xx ports A, C, and D allow simulation of single chip port operation when expanded bus is operating.
- MAP Switch – provides easy assignment of chip selects to ram and flash memory banks.
- MODE Switches – 4 DIP switches to fully support Hard Reset Word Configuration options.
- COM Switch – provide easy method of applying or isolating serial connections to RS232 transceiver.
- COM1 - SCIA1 w/ RS232 type DB9-S Connection
- COM2 - SCIA2 w/ RS232 type DB9-S Connection
- COM3 – SCIB1 w/ RS232 type 10pin cable Connection
- COM4 – SCIB2 w/ RS232 type 10pin cable Connection
- CAN Ports – 3 CAN transceiver (PCA82C250) interfaced ports, 1 x 4 headers.
- LCD Port - LCD Module Interface Connector w/ Contrast Adjust, Buffered and Memory Mapped
- KEYPAD and KEY Port - 16 Key or 20 Key interface, Debounced, Buffered, and Memory Mapped
- BUS Port – provides 32 data and 24 address or MPC5xx ports A and D on 60 pin header.
- CONTROL Port - Bus Controls or MPC5xx ports on a 44 pin header.
- QSM Ports – 2 Serial I/O ports with 16 pin socket headers.
- MIOS Port - MDA, PWM, and MGP timer or I/O interface with 34 pin socket header.
- TPU Ports - 3 Timing Processor I/O ports with 20 pin socket headers.
- QADC Ports - 2 Analog I/O ports, one 20 pin and one 24 pin socket header.
- INT Port – Interrupt or MPC5xx SGP port I/O with 10 pin header.
- POWER Port – Primary and standby power supply access port.
- I/O Connectors in .1 grid, pin headers for bus and control provide easy ribbon cable connection for external connections. Socket headers provide easy wire connection to solderless prototype area or with provided pin headers installed, will allow ribbon cable or wire wrap connections.
- Large Prototyping Area (5 x 1.75 inch) with +5V and ground connection grids.
- Mictor Logic Probe connectors for the Address and Data bus
- Solderless Prototyping area (2.5 x 1.5 inch) for easy installation of test connections.
- Power Indicators – Supply voltage indications for 5, 3.3, and 2.6V supplies
- Reset Switches – POR, Hard, Soft reset buttons.
- User Indicators – 4 user indicators to provide user conceived visual response during testing.

Axiom development systems provide for low cost software testing with the use of the Monitor in the on-board EPROM. Operation allows the user to load code in the On-Board RAM, Execute application, and display or modify registers or memory. After code is operational the user may relocate the code and reprogram the MPC5xx Internal Flash EEPROM or the boards fixed flash for dedicated operation of new software. No additional hardware or software is required to operate. For high level debug, extensive tools are available for the PowerPC core and the Debug Port is available on the PM-5xx module to connect a background debugger.

Cautionary Notes

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EMC Information on CMD565

1. This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of EN5022 and EN 50082-1: 1998 as a **CLASS A** product.
2. This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.
3. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.
4. Anti-static precautions must be adhered to when using this product.
5. Attaching additional cables or wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

Getting Started

See the **README.TXT** file on the CD provided with this board for all the documentation and support files provided.

See also the PM-5xx Personality Module Reference for your platform specific information, including BDM and CMFI (on-chip flash) programming support.

This section assumes that you have just received your board from the manufacturer. If this is not the case then jumpers and switches may have been changed so that the board may not function as expected. In this case, see the "Option Switches and Jumpers " section of this manual and return everything to "default" positions before proceeding.

To get started quickly, perform the following test now to make sure the board is working correctly:

1. Connect one end of the supplied 9-pin serial cable to a free COM port on your PC. Connect the other end of the cable to the COM-1 port on the board.

2. Run a standard ANSI terminal communications program set to 9600 baud, N,8,1. Any terminal program will work, including the simple terminal that comes with MS Windows (HyperTerminal) or the one supplied on the support CD with this board.

3. Apply power to the board by plugging in the wall plug power transformer that came with the system.

4. After a few seconds delay, if everything is working properly, you should see the main utilities menu, similar to the following:

```
 ---------------------------------
 AXIOM CMD-5XX UTILITIES
 ---------------------------------

1. Debug Monitor
2. On-Chip CMFI Flash Programming
3. External Flash Programming
4. Test Hardware

Select:
```

Your board is now ready to use! If you do not see the monitor prompt, press then release the RESET button on the board. If still no go, or if the text is garbage, see the **TROUBLESHOOTING** section of this manual. The MEM bank should contain the “Axiom MON5xx” EPROM’s and this bank only should be assigned CS0 to boot the utilities.

Software Development

The example monitor / utility software initializes the clock to run this board at 20 MHz on power-up. The board has been tested and does run at speeds up to 40 MHz however, which you can set by changing the PLL Register in your software.

Software development on the CMD-5xx is best performed using a BDM tool connected to the BDM-PORT connector on the PM-5xx module. This provides real-time access to all hardware, peripherals and memory on the board. BDM software is also available for high-level source code debugging. Contact the manufacturer for more information.

If a BDM is not available, software development can be done using the included simple monitor program to upload your code to ram and execute it or program it into EEPROM.

In either case, software is usually uploaded to RAM and executed during development, then programmed into EEPROM to execute when power is applied.

Terminal Settings

The utility software provided uses the serial port connected to your PC running a terminal program as described under "Getting Started". While you can use almost any commercial or free serial communications terminal interface, it is important that you configure it to work properly with this board. The following settings are important:

1. BPS: 9600, Data Bits 8, Parity none, Stop Bits 1
2. Flow Control should be set to HARDWARE or None
3. Emulation should be ANSI
4. When uploading files to the board, be sure to send in Text mode.
5. When programming CMFI memory, you must use ONE of the following:
    a. 15 millisecond pace delay after each line
    b. wait for echo character following each line

A free terminal program that works well with this board called “AxIDE” is provided on the support CD. It is also available for download from the manufacturers web site at www.axman.com.

Tutorial

The following brief tutorial will help you become familiar with software development on this board quickly. For processor specific tutorials, such as BDM support and CMFI programming, see the PM-5xx Personality Module Reference that came with your board.

Using the Debug Monitor

This board ships with a simple monitor utility programmed into the U15 and U16 EPROM devices. See "Getting Started" for startup instructions. Choose menu item 1 to launch the monitor.

Using this program and any serial communications terminal program, you can display and modify memory and registers on the board from any PC. This is done by typing commands into the terminal program on the PC. Type help and hit <enter> for a complete list of available commands.

You can experiment with some of the commands like reading (MD) and modifying (MM) memory. Make sure you're modifying memory that is mapped to valid addresses or the monitor program will "hang" or throw an exception. You may then have to RESET the board to get the monitor back. Internal RAM starts at 0x3F9800. External RAM starts at 0x800000 as shipped with the default MAP_SW settings. The monitor program itself uses internal RAM from 0x3F9800 - 0x3F9FFF, so if you modify anything in this area while the monitor is running it may hang.

You can also load and execute a program from memory using this utility. A simple "hello world" program is provided for you on the CD as an example. Follow these steps to load and execute it from internal RAM using the monitor program:

1. At the monitor prompt > type **DL** and hit <enter>.
2. Select the send text file (or upload) command from your terminal program and locate the file named "**HELLO_R.S19**" included on the support CD. Send this file to the board.
3. When finished uploading, type **go 3FA004** at the prompt. You should see the phrase "Hello World!" echoed back to the screen, which is all that this simple test program does, each time you hit a key.
4. To exit from this test program, hit a RESET button on the board.

This example program was compiled with the Diab Data compiler. The source files and scripts used are included on the support CD as follows:

`HELLO.C`	Main source code file
`SERIAL.C`	Serial port I/O and ASCII text conversion routines
`HELLO_R.DLD`	Diab Linker script - specifies the programs memory organization
`HELLO_R.BAT`	DOS batch file used to build the program

Programming the Onboard Flash Memory

After testing your program running out of RAM you will probably want to program it into EEPROM so that it starts whenever power is applied to the board. To do this you must first change the starting address of your program to match that of the memory device being programmed. This is usually done in assembly language using the ORG statement, or by MAK or Project file arguments to the LINKER if using a compiler.

As an example, a version of the "hello world" program is included on the support CD that has been relocated to start at address 0x400000. This will be the starting address assigned to external onboard flash memory, once we move some jumpers and reset the board.

This version is called "**HELLO_F**". It uses the same HELLO.C and SERIAL.C source code as the RAM version, with the following unique files:

`INIT.S`	Example Boot initialization assembly source file
`HELLO_F.DLD`	Diab Linker script - specifies the programs memory organization
`HELLO_F.BAT`	DOS batch file used to build the program

The output files produced from this build are called `HELLO_F.S19` and `HELLO_F.ELF`.

Follow these steps to program the "hello world" example to start on power-up instead of the monitor program:

1. Make sure the MAP_SW positions 2 and 7 are only on. This will configure the board to match the default Memory Map.
2. Make sure the MEM_EN jumper is installed and press RESET to get the utilities menu (see Getting Started).
3. Select External Flash Programming from the menu.
4. Select **2** for External Flash (U13/U14) - CS2.
5. Select **1** to Erase the Flash Memory. This should take less than 20 seconds.
6. Select **2** to Program from a file -> Flash CS. This will prompt you to upload the file to be programmed.
7. Select the send text file (or upload) command from your terminal program and locate the file named "**HELLO_F.S19**" included on the support CD and send this file to the board. If you have problems uploading, try adding a pacing delay.
8. After all lines from the file have been programmed, the words programmed are displayed along with any errors, followed by the menu again. Now the "hello world" program is at address 0xC00000 (the current location of onboard flash), however it is linked to be run from 0x400000, since this is the address the program assigns to the CS0 base register at runtime.

   Explanation: Since the monitor EPROMS in U15/16 use the same Chip Select 0 that we wish to use for the "hello world" program (by the setting of the MEM_EN jumper), we must do an offset programming operation to a different chip select. Setting the MAP Switch position 7 on configures the onboard flash to Chip Select 2. The monitor program will offset the program to that chip select base address (0xC00000) temporarily during programming.
9. Power down the board and move the MODE_SW1 switch 5 to the OFF position. This will configure the board to 32-bit mode boot, which is required for the onboard flash memory to boot while in the 32 bit wide mode.
10. Remove the MEM_EN jumper and change the MAP Switch to position 7 OFF and position 5 ON.
11. Power up the board. You should see the "hello world" message on your terminal screen every time you press a key.
12. To return to the Utilities Menu, turn power off the board, move the MODE_SW1 switch 5 back to ON, install the MEM_EN jumper, and set the MAP switch position 5 OFF and position 7 ON. Power on the board and you should see the menu again.

Although this "Hello World" example is a simple program, you can use the same procedure for programming your own application into external flash memory using the CMD-5xx development board.

To develop more complex applications, with source level debugging, you will no doubt require a debugger tool. An excellent choice would be a Background Debug Module (BDM) which is supported using the BDM-PORT on this board. See the "Using a BDM" section of this manual for more information. Follow these steps to program the "hello world" example to start on power-up instead of the monitor program:

Memory Banks and Default Memory Map

The CMD-5xx board provides three memory banks and a Port Replacement Unit (PRU) that can be optionally selected by the MPC5xx microcontroller chip selects. The memory banks are the Synchronous SRAM (U2-U5), Burstable Flash EPROM (U13-U14), and MEM firmware sockets (U15-U16). Since the MPC5xx chip selects are fully programmable (with the exception of CS0 providing external Reset start-up) the memory banks can be located at any location in the MPC5xx memory space. As a reference example, Axiom has defined a default memory map where the chip selects are located at predefined locations. The provided software uses this memory configuration. If you modify this memory map make sure that all memory bank and chip select configuration settings are correct. See **Memory Device / Bank Selection and Configuration** for more information.

Following is the default memory map for this board as configured by the utility EPROMs installed the MEM sockets U15/U16. The internal map is detailed further in the MPC5xx Users Manual. Chip Selects 0-3 can be changed by your software to map the external memory in different locations but the chip select configuration for each memory type should be maintained.

Possible Chip Select usage:

Synchronous SRAM Memory Bank	CS0, CS1, CS2, or CS3	default CS1
Burstable Flash Memory Bank	CS0, CS1 or CS2	default CS2
Port Replacement Unit	CS2 or CS3	default CS3
MEM Sockets Bank	CS0	

CMD-5xx Default Memory Map

Internal Memory (See MPC5xx microcontroller documentation)

0000 0000	CMFI Internal Flash Memory Array if present
0007 0000	Reserved or CMFI Array 2
002F C000	On-chip Control and Status Registers
003F 9800	Internal SRAM

External Memory

0040 0000	40:0000 – 40:FFFF for 64K device 40:0000 – 47:FFFF for 512K device	**CS0** - External MEM EPROM 16 bit MEM devices U15A-U16 **or** 8 bit MEM device in U15B (shipped with monitor / utilities program here)
0080 0000	**CS1** – External Sync. SRAM – 32 bit port, devices U2-U5 2M bytes at 80:0000–9F:FFFF on this board	
00C0 0000	**CS2** – External Flash Memory 32 bit port , parallel devices U13-U14 with 4M bytes at C0:0000-FF:FFFF on this board **or** 16 bit port, U13 device with 2M bytes at C0:0000–DF:FFFF	
0100 0000	**CS3** – External Port Replacement Unit (PRU), LCD Port and Keypad (see the PRU Memory section below for details)	
0140 0000	Non Mapped Address Space	
FFFF FFFF		

Synchronous SRAM Memory

The synchronous SRAM Memory Bank is composed of four 256K x 32 memory devices. These memory devices are connected in linear order from U2 to U5 so that the low order address of the memory bank will access U2 and the high order addresses of the memory bank will access U5. This memory bank must be configured as a 32 bit wide port but is byte, half word, and word accessible for read or write operations. The synchronous SRAM memory on revision C and earlier boards (CY1339) requires 1 wait state no matter the bus clock frequency to operate in asynchronous mode and will provide 32-bit wide burstable output of 2/1/1 cycles type. Revision D boards provide 0 wait state SRAM memory (CY1338) and will operate a 1/1/1 burst cycle.

Burstable Flash Memory

The Burstable Flash Memory Banks U13 and U14 contain two Intel DT28F160F3 or AMD AM29BL162B type flash devices. The two flash devices are configured in parallel to provide either a 16 bit wide port operating U13 or a 32 bit wide port operating both U13 and U14. Both devices require wait states when accessed in asynchronous mode and the same wait state delay during the first cycle of a burst type access. Refer to the specific device data sheet and sample software provided for configuring the flash memory.

Port Replacement Unit (PRU) Memory

The Port Replacement Unit (PRU) provides for single chip operation of the MPC5xx I/O ports used for address, data, and interrupts during 32 bit bus operation. The PRU also provides memory mapping and control of the LCD and Keypad Ports. The PRU_EN jumper must be installed (see PRU_EN section) and chip select configuration for the PRU must be set to 32 bits wide and should provide external access termination (use TA* signal) for correct operation of all functions.

The I/O ports provided by the PRU do not duplicate signal levels or internal pull-up operation of the MPC5xx I/O ports. The PRU I/O port output voltage levels are limited to +3.3V high while the MPC5xx I/O ports typically will provide voltage level of +5V high (refer to MPC5xx technical data for host). PRU I/O port input voltage levels are tolerant of +5V signals. The PRU register operation and memory map closely follows the MPC5xx I/O port data and direction registers located at internal addresses 2FC024 – 2FC02F. Following is the memory map of the PRU.

PRU Offset Address	Register Name	Register Information	Port
0x0000	LCD CMD1	LCD Module address 0, Command register access. Bits D0 – 7 of 32	LCD_PORT [1]
0x0004	LCD DATA1	LCD Module address 1, Display Data register access. Bits D0 – 7 of 32.	LCD_PORT [1]
0x0008	LCD CMD2	LCD Module address 2, Command register access. Bits D0 – 7 of 32.	LCD_PORT [1]
0x000C	LCD DATA2	LCD Module address 3, Display Data register access. Bits D0 – 7 of 32.	LCD_PORT [1]
0x0010	KEY DATA	Keypad or Keyport data register	KEY_PORT or KEYPAD [2]
0x0014	Reserved	Not applied, access termination provided.	
0x0018	Reserved	Not applied, access termination provided.	
0x001C	Reserved	Not applied, access termination provided.	
0x0020	Reserved	Not applied, access termination provided.	
0x0024	PRU Port D	D0-31 I/O port replacement	SGPIODT1 [3]
0x0028	PRU Port A&C	C0-7, A8-31 I/O port replacement	SGPIODT2 [3]
0x002C	PRU Port Direction	Replacement Port Direction	SGPIOCR [3]

1. Refer to LCD Module data sheet for register information.
2. Key_Port or Keypad is read only and writes have no effect. Keypad data is provided in a binary number in bits D0 – D4 for current or last key pressed while bit D7 indicates if the key is currently active (pressed).
3. Refer to MPC5xx users manual for register operation.

MEM Sockets Memory

The primary function of the MEM sockets memory bank is for CMD-5xx firmware. This memory bank is the default program code source from Reset or Power on and can only be enabled to operate from chip select CS0. The two memory sockets U15A and U16 provide a 16 bit wide port (default) while memory socket U15B provides an optional 8 bit wide port. If the 8 bit wide port is used the U16 socket should be vacant of any memory device for proper operation. The MEM sockets are configured for standard 8 bit wide 27xxx series EPROM's from 32K bytes up to 1M byte per socket. These devices require wait states during access for proper operation.

Option Switches and Jumpers

Mode Switch 1-4 External Reset Configuration Options

Mode Switches 1, 2, 3 and **4** configure the external Hard Reset Configuration Word when enabled. These switches provide a logic 0 or low level when off and a logic 1 or high level when on. The configuration is only presented to the data bus during Hard Reset if External Configuration is enabled with the CFG_EN option jumper installed **and** the External Configuration switch enabled on the PM-5xx module. The Hard Reset Configuration Word options are all defaulted to logic 0 when the Mode Switches are in the OFF position. For more information on the MPC5xx Reset Configuration refer to the Reset Chapter in the respective MPC5xx technical manual. The following tables represent common configuration items and should be verified against the MPC5xx installed.

Mode Switch 1

	Control Register Bit	Reset Function	Default Position
1	EARB	Internal or External Arbitration	Off = Internal
2	MSR[IP]	Initial Interrupt Prefix	Off = 0
3	BDRV	Bus Pin Drive Strength	Off = Full Drive
4	BDIS	Memory Controller Disable	Off = Enabled
5, 6	BPS	Boot Port Size: Off/Off = 32Bit Port, Off/On = 8 Bit Port	On/Off = 16 Bit Port
7	Reserved	Future Use	Off
8	Reserved	Future Use	Off

Mode Switch 2

	Control Register Bit	Reset Function	Default Position
1	Reserved	Future Use	
2, 3	DBGC[0:1]	Debug Pins Configuration	Off = VFLS[0:1], BR, BG, BB, BI
4	DBPC	Debug Port Pins Configuration	Off = DSCK, DSDO, DSDI
5	ATWC	Address Type / Write Enable Pins Configuration	Off = WE/BE[0:3]
6, 7	EBDF	External Bus Division Factor	Off = Equal to CLKOUT
8	Reserved	Future Use	Off

Mode Switch 3

	Control Register Bit	Reset Function	Default Position
1	PRPM	Peripheral Mode Enable	Off = Not Peripheral
2,3	SC[0:1]	Single Chip Select, Off/On = 16 bit bus, On/Off = Single-chip w/ Show cycles, On/On = Single-Chip	Off/Off = 32 bit bus
4	ETRC	Exception Table Relocation	Off = Disabled
5	FLEN	Internal CMFI Flash enable	On = Enabled
6	EN_COMP	Enable Code Compression ** Must be supported by processor.	Off = No compression
7	EXC_COMP	Enable Exception Compression *** Must be supported by processor	Off = No compression
8	Reserved	Future Use	Off

Mode Switch 4

	Control Register Bit	Reset Function	Default Position
1, 2	OERC	Other Exception Relocation Control ** ERTC on for any effect	Off , Off = 0x00 offset
3	Reserved	Future Use	Off
4	Reserved	Future Use	Off
5, 6, 7	ISB	Internal Space Base Select	Off, Off, Off = 0x00000000
8	DME	Dual Mapping Enable	Off = No Dual Mapping

CFG_EN Jumper

Enables/Disables External Reset Configuration drivers on the CMD5xx board. When installed, this jumper will connect the EXCNF* signal from the PM-5xx module to the External Reset Configuration Word buffers and allow the Configuration word to be driven onto the data bus during SRESET Condition. Removing this jumper will disable the Reset Configuration Word from being driven on to the data bus. The jumper should be installed until the internal Hard Reset Configuration Word is programmed into the MPC5xx internal flash memory of the microcontroller operating the board. This can be done from the utilities supplied with the board in U15/U16.

Memory Device / Bank Selection and Configuration.

The CMD-5xx board has three external memory banks and a PRU that provide:

- 512K x 32bit (2MByte) Synchronous Static RAM (U2 – U5)
- 1M x 32bit (4MByte) Burstable Flash EEPROM (U13 - U14)
- MEM Option Sockets for 8 or 16bit wide EPROM memory (U15 – U16)
- Port Replacement Unit (PRU) with LCD and Keypad Ports

Each memory bank can be configured individually to operate from the MPC5xx chip selects. Caution should be used not to place more than one memory bank on the same chip select or properly configure the chip select to operate the Memory Devices in the memory bank correctly. **Failure to observe precautions may render the external memory bus inoperable and cause the user great anxiety and grief.**

The MAP Switch, MEM_EN option jumper, and PRU_EN option jumper connect MPC5xx chip selects to the different memory banks. If memory access problems occur, the settings of these options and the associated chip select configurations should be reviewed with some detail. Information to configure the chip selects and memory is detailed in the following sections.

Memory Bank Chip Select Configuration

Application software that executes on reset must configure each memory bank chip select properly for correct operation. Following is a reference table of Memory Bank chip select values:

Memory Bank	Reg.	Default Value	Notes
MEM Sockets - 16 bit port	BR0	0x00400803	Base address = 0x400000, Port width = 16 bit *Default
MEM Sockets - 8-bit port	BRO	0x00400403	Port width = 8 bit
MEM Sockets	OR0	0xFFC00020	Memory Range = 0x400000, wait state = 2, 40MHz / 70ns devices
RAM – 32 bit port only	BRx	0x00800003	Base Address = 0x800000, Port width = 32 bit FIXED *Default
RAM – asynchronous mode	ORx	0xFFC0000	Memory Range = 0x400000, wait state = 0 or 1, Note: asynchronous operation requires 1 wait state no matter clock frequency on rev. C (CY1339 devices).
RAM – burst mode	ORx	TBD	TBD
Flash – 32 bit port asynchronous	BRx	0x00C00003	Base address 0xC00000, Port width 32 bit, *Default MAP_SW-8 = off
Flash – 16 bit port asynchronous	BRx	0x00C00803	Base address 0xC00000, Port width = 16 bit , MAP_SW-8 = on
Flash – 32 bit port asynchronous	ORx	0xFFC00030	Memory range = 0x400000, wait state = 3, asynchronous operation 40Mhz clock, 95ns device
Flash – 32 bit port burst mode			
Flash – 16 bit port burst mode			
PRU – 32 bit asynchronous only	BRx	0x01000007	Base address = 0x1000000, Port width = 32 bit *Default
PRU – External terminate	ORx	0xFFFF80F0	Memory Range 0x8000, wait state = External Terminate (TA*) *Default

MAP_SW – Ram Bank and Flash Bank Options

The MAP Switch provides chip select to memory bank selection for the Synchronous RAM Memory Bank and the Burstable Flash Memory Bank. Positions 1-4 set the Chip Select for RAM, the rest are for Flash. Position 8 determines the Flash Bank Port Size so that either 16 or 32 bit burstable port can be selected. If switches 1 to 7 are all off the RAM and Flash Banks are disabled.
The Default positions shown below will set RAM to CS1 and FLASH to 32 bit mode on CS2.

MAP_SW Position	Chip Select	Default Position	Memory Bank Connection and Notes
1	CS0	Off	RAM – on for BDM use typically (with MEM_EN off)
2	CS1	**ON**	RAM – ***Default** monitor operation position
3	CS2	Off	RAM
4	CS3	Off	RAM
5	CS0	Off	Flash – on to Reset (BOOT) from Flash Bank (with MEM_EN off)
6	CS1	Off	Flash
7	CS2	**ON**	Flash - ***Default** monitor operation position
8	Flash Port Width	Off	Flash – Port Width Off = 32 bit wide port (parallel flash devices), On = 16 bit wide port (single flash device)

MEM_EN Jumper

The MEM_EN option jumper is located next to the MAP_SW. When installed it connects chip select CS0* to the MEM sockets U15/U16. The MEM sockets normally contain the Axiom Monitor / Utility firmware EPROM's that provide board operation from Reset. If the MEM_EN option jumper is removed the MEM sockets memory bank U15/U16 will be disabled and idle.

This jumper should be removed if CS0* is assigned to another memory bank.

MEM_OPT Jumper

The MEM_OPT option jumper provides options for 28 or 32 pin memory device and 8 or 16 bit addressing options for 32 pin devices installed in the 32 pin U15 and/or U16 MEM sockets memory bank. A 28 pin memory device must have MEM_OPT jumper 1 installed to supply necessary operating power or the device may load the data bus even if deselected with the MEM_EN option jumper.

Position 1 = Memory is one or two 28 pin devices. ***Default - 16 bit port**
Position 2 = Memory is two 32 pin devices, 16 bit port, U15A/U16 in use.
Position 3 = Memory is one 32 pin device, 8 bit port, U15B in use.

- A single 28 pin device can be used in U15B to provide an 8 bit port also.
- Standard EPROM devices are the 27xxxx series eproms. Both 5v and 3.3V versions can be used.

MEM_VOLT Jumper

The MEM_VOLT option jumper determines the MEM Sockets device operating voltage. This should be set to the voltage required for the device(s) installed in U15A/B and U16. The device must be compatible with the bus voltage level of the installed MPC5xx or damage to the MPC5xx can occur.

Position 1-2 = MEM (U15/U16) devices are +5V operation ***Default**
Position 2-3 = MEM (U15/U16) devices are +3.3V operation

PRU_EN Jumper

The PRU_EN option jumper provides chip select assignment for the Port Replacement Unit, Keypad, and LCD interfaces. Chip selects CS2 or CS3 (Default) can be assigned to the PRU. If the option jumper is idled (no 2 pins connected), the PRU is disabled and not present in the memory map. Any previous operations with the PRU will remain valid until the next system reset.

Position 3-2 = CS3 chip select assigned ***Default Position**

Position 2-1 = CS2 chip select assigned

Correct chip select configuration in software is critical for valid operation of the PRU. The PRU provides the TA* (Transfer Acknowledge) signal to terminate bus transactions and provide proper timing for replacement ports, Keypad and LCD. Following are the required chip select register values for correct PRU operation:

BRx = 01000007 hex, default base address shown but can be moved to any available memory map location.
ORx = FFFF80F0 hex

Communication Ports

The CMD-5xx board provides interfaces for up to 4 SCI serial ports, 3 TouCan ports and a DLC/J1850 port. COM-1 and COM-2 serial ports with female DB9 connectors are available for RS232 operation of host MPC5xx SCI A channels 1 and 2. COM-3 and COM-4 serial ports with 10 pin IDC to DB9 connector headers are available for RS232 operation of host MPC5xx SCI B channels 1 and 2 if available. All COM ports provide the following standard pinout in a standard female 9 pin serial connector (DB9-S):

Pin 1, 4, and 6 = connected for DTR/DSR flow control null
Pin 2 = TXD output (RS232 level)
Pin 3 = RXD input (RS232 level)
Pin 5 = Ground/Vss/Common
Pin 7 and 8 = connected for RTS/CTS flow control null
Pin 9 = open

Notes:

1. All COM ports provide connection pads so that flow control signals may be applied by user modification. Each connection pad is numbered for the associated serial connector pin. Each connection pad can be isolated from the others in it's group by cutting the associated trace on the bottom side of the board.
2. COM-2 has a DCE/DTE option, see below.

COM_SWITCH - Serial Port Configuration

The COM_SWITCH provides a means of isolating the individual SCI RXD and TXD signals from the RS232 interface translator device (U31). This allows the SCI channels to be used for other purposes. In conjunction with the **COM_PORT** header, additional signals can be applied to the RS232 interface translator. Following is a table of the SCI signals and switch positions used for enabling RS232 operation.

Switch Position and default condition	SCI Channel Signal	RS232 COM Port Connection	COM_PORT Signal Direction to RS232 interface translator
1 – On	SCI_A_ TXD1	COM-1	Output
2 – On	SCI_A_ RXD1	COM-1	Input
3 – On	SCI_A_ TXD2	COM-2	Output
4 – On	SCI_A_ RXD2	COM-2	Input
5 – Off	SCI_B_ TXD1	COM-3	Output
6 – Off	SCI_B_ RXD1	COM-3	Input
7 – Off	SCI_B_ TXD2	COM-4	Output
8 – Off	SCI_B_ RXD2	COM-4	Input

JP1 – COM-2 DCE/DTE Option

COM-2 is optioned as a DCE type RS232 connection by default (same as COM-1). This allows direct connection to a standard PC serial port.

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COM-2 DTE option. This requires a NULL modem adapter to connect to a standard PC com port.

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Data Link Controller / J1850

The CMD-5xx board provides a location to place a J1850 transceiver (Philips AU5780 or Harris HIP7010) for development of a J1850 interface with the MPC565 Data Link Controller integrated peripheral. The board provides a DLC_IN input connector for connection to the appropriate I/O port of the processor, a J1850 output connector for connection to the J1850 bus, and a termination selection (T_LOW) option jumper.

DLC_IN Connector

Pin 1 = DLC TX input
Pin 2 = DLC RX output
Pin 3 = Transceiver Loop Back, active low will cause transceiver to loopback data for testing.

J1850 Connector

Pin 1 = +V from J1850 bus (vehicle battery), can be left disconnected if +12V supply is used for CMD-5xx board.
Pin 2 = J1850 signal
Pin 3 = Ground or common.

T_LOW Option Jumper

Open = High impedance termination (slave).
Installed = Low impedance termination (master).

CAN Interface and Options

The CMD-5xx board provides 3 CAN (TouCAN) transceivers with I/O ports: CAN_A, CAN_B, and CAN_C. All three ports are supported by a Philips PCA82C250 1MBaud CAN transceiver. The CAN_A and CAN_B ports are directly interfaced to the host MPC5xx controller's TOUCAN channels A and B. The CAN_C port is available for connection to MPC5xx controller I/O ports that support a 3rd TouCAN channel but is not connected due to I/O port options associated with the 3rd channel. Following are the options associated with the CAN ports:

CAN_A_EN, CAN_B_EN, and CAN_C_EN Option Jumpers

These option jumpers provide output enable and slew rate control of the respective transceiver. Installing the option jumper (default) provides minimum slew rate (fast edge) and enables the output of the respective transceiver. Opening the option disables transceiver output to the CAN bus. With the option jumper removed, Pin 2 of the option header can be connected by the user to an available I/O port for software control of transceiver output (active low). Slew rate can be increased if necessary to reduce switching noise by increasing the value of R22, R23, or R24 for the respective CAN port A, B, or C. See the PCA82C250 data sheet for details.

CAN_A_RX and CAN_B_RX Option Jumpers

These option jumpers enable the receive connection from the CAN channel transceiver to the MPC5xx host controller CNRX0 I/O pin. Installed by default, the options allow the isolation of the RX signals so that the user may use a different connection or transceiver for the MPC5xx TouCAN port.

CAN_C_IN Connector

This connector provides the CAN C channel TX and RX signal to the transceiver. Depending on the MPC5xx in use, the respective CAN_C_IN pin would be connected to the associated MPC5xx I/O pin providing the TouCAN channel C signals by the user.

Pin 1 = TouCAN C TX signal (pin closest to label of connector), MPC561/2/34 =MIOS Port pin 31, MPC565/6 = MIOS Port pin 32.
Pin 2 = TouCAN C RX signal. MPC561/2/3/4 = MIOS Port pin 30, MPC565/6 = MIOS Port pin 33.

CAN_A, CAN_B, and CAN_C I/O Port Connectors

These ports provide the CAN transceiver input and output connection to the CAN bus. No bias or termination for the CAN bus is provided on the CMD-5xx board, if required the user must install these components in the proto area or elsewhere on the CAN bus. Following are the pin connections for the ports:

Pin 1 = CAN-Hi level signal
Pin 2 = CAN-Lo level signal
Pin 3 = Ground or common (this is required for proper return path on CAN bus)
Pin 4 = +5Vsupply for remote use or bias of CAN bus.

LCD-PORT and KEYPAD / KEY-PORT

The LCD Port provides a versatile connector to attach 80 or 160 character display modules and some graphics display modules with embedded drivers. The PRU (U20) provides address decode and LCD select control signals for the LCD and Keypad ports. Both ports are controlled by host processor chip select CS2 or CS3 (default) when enabled by PRU_EN option jumper .

> **USE CAUTION** when connecting your LCD to the LCD-PORT - make sure the power polarity (JP2) and correct placement of the LCD cable so that signals are correctly matched.

The KEYPAD and KEY_PORT connectors can be used to connect passive keypad devices to the board.

Example source code for the LCD and Keypad drivers are provided on the Axiom CMD-5xx support CD. The memory map offset for the LCD / Keypad are determined by the PRU is as follows:

LCD / Keypad Memory Map

0x0000	LCD_PORT, Command Register 1 for up to 80 character display.
0x0001	LCD_PORT, Display Data Register 1 for up to 80 character display.
0x0002	LCD_PORT, Command Register 2 for graphic or 160 character display.
0x0003	LCD_PORT, Display Data Register 2 for graphic or 160 character display.
0x0004	Keypad / KEY_PORT key data. Read Only.
0x0005	Keypad / KEY_PORT key data. Read Only.
0x0006 - 0xFFFF	Not used

LCD Display CONTRAST

The CONTRAST adjustment allows a contrast Vee voltage to be presented to the LCD_PORT of –5V to +5V DC.

JP2 - LCD_PORT Power Polarity Select

JP2 determines the display power pin polarity on the LCD_PORT. Depending on the type and location of the IDC connector on your display module, the power connections may need to be reversed. Care should be used to verify proper connection and signal matching at the IDC Cable Connector and LCD_PORT.

See the schematic to match this jumper setting to your LCD device connector. Contact support@axman.com for assistance applying a LCD module.

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Personality Module (PM-5xx) Options and Settings

The PM-5xx modules provide the CPU with associated support hardware such as oscillator(s), debug support connectors, and options for reconfiguring the CPU. Nexus 50 pin standard development connector is also provided on the MPC561-566 versions. The -T option PM boards provide a ZIF (zero insertion force) type socket for the host processor.

CONFIG Switch

The CONFIGURATION SWITCH provides user options for MODCK settings, RSTCNF* signal operation, and internal flash programming enables. All PM modules provide the 6 switches but not all devices support internal Flash.

POSITION OPTION

1,2,3 MODCK 1,2,3 setting.
ON = high level during RESET.
OFF = low level during RESET.
Default = 1,3 Off, 2 ON. 4MHz crystal oscillator reference, 20MHz default clock.

4 RSTCNF* Signal enable.
ON = External Reset Configuration Word Enabled
OFF = Internal Hard Reset Configuration Word
Default = ON. CMD-555 board provides configuration Word.

5 EPEE enable. MPC555/6 Internal CMF flash array programming enable.
ON = EPEE signal enabled for programming internal CMF flash array.
OFF = EPEE signal disabled.

6 VPP enable. MPC555/6 Internal CMF flash array VPP programming voltage enable.
ON = VPP enabled for programming CMF flash Boot Block.
OFF = VPP disabled.

PM-555/6 Hardware Options

VDDSRAM Voltage Source Option

VDDSRAM is connected to the 3.3V supply on the PM-555 board by a zero ohm resistor R11. To apply a different supply for the VDDSRAM pin, the R11 resistor should be removed and the CMD-555 POWER_PORT connection can be used for applying the new voltage source.

VDDSYN Voltage Source

The VDDSYN connection to the MPC555/6 may be isolated by from the 3.3V supply by removing inductor L1. Alternate voltage source can then be applied the VDDSYN at the CMD555 POWER_PORT.

KAPWR Voltage Source

The KAPWR connection is connected to the 3.3V supply on the PM-555 board by zero ohm resistor R8. To apply a different voltage source for low power back-up operations, R8 should be removed and the new source applied to the CMD555 POWER_PORT pin for the KAPWR connection.

VRH and VRL QADC Reference Supplies

Zero ohm resistors R9 and R10 provide isolation of VRH and VRL reference signals respectfully. One or both of these resistors may be removed to apply an external reference voltage at the CMD-555/6 QADC_A Port.

PM- 555/6 -T Additional Options

- **R36 / 37 Resistors -** BDM Port VFLS1 signal selection option.
- **R38 / 39 Resistors -** BDM Port VFLS0 signal selection option.
- **C4 XFC Filter -** PLL operation XFC filter capacitor value option.
- **R35 Resistor** - PORESET level detector isolation, remove to isolate 5V reset generator for PORESET signal.

PM-561/2/3/4 Hardware Options

JP1, 2, 3, 4 Option Jumpers

BDM Port operating voltage selection. All 4 jumpers must be optioned the same for correct interface levels on associated signals. The selection of 2.6V or 3.3V operation is dependent on the BDM Pod to be connected to the BDM_PORT. Default setting is 3.3V which selects the proper voltage outputs for most common BDM Pods. Refer to BDM Pod information for correct setting.

VDDSRAM Option

VDDSRAM pin is the input to an internal shunt regulator on the MPC561-4. The resistor R8 on the PM-561-4 board provides current limit input to this pin. To apply a different voltage to this pin, the R8 resistor should be removed and the CMD-561-4 POWER_PORT connection for VDDSRAM should be used for voltage input. If the CMD561-4 board POWER_PORT is used, the appropriate current limit resistor must be placed in series between the voltage source and the POWER_PORT or damage to the MPC561-4 will occur.

XFC Filter Capacitor Option

PM561-4 capacitor C3 provides the XFC filtering for the PLL circuits. The capacitor should be changed by the user if PLL locking problems are experienced at the frequency of operation selected. Current value is 3.3nF. Refer to MPC561 manual for more information.

VDDSYN Voltage Source

The VDDSYN connection to the MPC561-4 provides CUT-AWAY pad #2 for isolation. To apply a different voltage source for low power back-up operations, the #2 CUT-AWAY pad should be cut and the new source applied to the CMD561-4 POWER_PORT pin for the VDDSYN connection.

KAPWR Voltage Source

The KAPWR connection to the MPC561-4 provides CUT-AWAY pad #1 for isolation. to apply a different voltage source for low power back-up operations, #1 CUT-AWAY pad should be cut and the new source applied to the CMD561-4 POWER_PORT pin for the KAPWR connection.

VRH and VRL QADC Reference Supplies

CUT-AWAY pads #4 and #5 provide isolation of VRH and VRL reference signals respectfully. One or both of these pads can be cut to apply an external reference voltage to the CMD-561-4 QADC_A Port.

EPEE and BOEPEE CUTAWAY #3

The PM-563-4 board has the EPEE and BOEPEE signals connected by CUT_AWAY pad #3. This connection is for NEXUS port programming of the CMFI flash. This connection will cause the CONFIG_SW position 5 or 6 to enable both signals. If this is connection not desired by the user, cut the CUT-AWAY #3 pad.

PORESET CUT-AWAY #6

The PM-561-4 board provides a 5V Voltage Level Detector to operate the PORRESET signal from power on and provide a 300ms PORESET signal duration when the PORESET switch is applied. For external application of a PORESET signal, the user should cut the CUT-AWAY #6 pad and use the CMD-561-4 CONTROL_PORT connection to apply the external PORESET signal.

PM561/2/3/4-T Options

- **#3 CUT-AWAY -** VFLASH signal, Internal flash array voltage source option.
- **#4 CUT-AWAY -** EPEE / BOEPEE signal, option to separate the signals.
- **#5 CUT-AWAY** - PORESET signal, option to remove 5V reset generator.
- **R3 /R30 Resistors -** VDDSRAM voltage source and current options.
- **R4 / 5 Resistors -** QADC VRL and VRH reference voltage options.
- **R20 / 21 Resistors -** VFLS1 signal selection for BDM Port option.
- **R23 / 24 Resistors -** VFLS0 signal selection for BDM Port option.
- **C3 XFC Filter -** PLL operation XFC filter capacitor.

PM-565/6 Hardware Options

JP1, 2, 3, 4 Option Jumpers

BDM Port operating voltage selection. All 4 jumpers must be optioned the same for correct interface levels on associated signals. The selection of 2.6V or 3.3V operation is dependent on the BDM Pod to be connected to the BDM_PORT. Default setting is 3.3V which selects the proper voltage outputs for most common BDM Pods. Refer to BDM Pod information for correct setting.

VDDSRAM Option

VDDSRAM1, 2, and 3 pins are connected to the 2.6V supply on the PM-565 by zero ohm resistor R5 on the PM565/6 board. To apply a different source for the VDDSRAM, the R5 resistor should be removed and the CMD565/6 POWER_PORT connection for VDDSRAM should be used for applying the new source input.

XFC Filter Capacitor Option

PM565/6 capacitor C5 provides the XFC filtering for the PLL circuits. The capacitor should be changed by the user if PLL locking problems are experienced at the frequency of operation selected. Current value is 3.3nF. Refer to MPC565/6 manual for more information.

VDDSYN Voltage Source

The VDDSYN connection on the MPC565/6 provides zero ohm resistor R11 for isolation. To apply a different voltage source for low power back-up operations, R11 should be removed and the new source applied to the CMD565/6 POWER_PORT pin for the VDDSYN connection.

KAPWR Voltage Source

The KAPWR connection on the MPC565/6 to the PM565/6 2.6V supply is provided by zero ohm resistor R12. To apply a different voltage source for low power back-up operations, R12 should be removed and the new source applied to the CMD565/6 POWER_PORT pin for the KAPWR connection.

VRH and VRL QADC Reference Supplies

PM565/6 zero ohm resistors R9 and R10 provide connection to PM565/6 VDDA and VSSA for VRH and VRL reference signals respectfully. One or both of these resistors can be removed to apply an external reference voltage to the CMD561-4 QADC_A Port.

EPEE and BOEPEE CUTAWAY #3

The PM565/6 board has the EPEE and BOEPEE signals connected by CUT_AWAY pad #3. This connection is for NEXUS port programming of the CMFI flash. This connection will cause the CONFIG_SW position 5 or 6 to enable both signals. If this operation is not desired by the user, cut the CUT-AWAY #3 pad to isolate the signals from each other.

PORESET CUT-AWAY #6

The PM565/6 board provides a 5V Voltage Level Detector to operate the PORESET signal from power on and provide a 300ms PORESET signal duration when the PORESET switch is applied. For external application of a PORESET signal, the user should cut the CUT-AWAY #6 pad and use the CMD565/6 CONTROL_PORT connection to apply the external PORESET signal.

VDDA and VSSA QADC Primary Supplies

Resistors R7 and R8 provide isolation of VDDA and VSSA supply voltages respectfully. One or both of these resistors can be removed to apply an external supply voltage to the QADC.

VFLASH Voltage Source

The VFLASH pin of the MPC565/6 is connected to the +5V supply by resistor R6 on the PM565/6-T board. To apply a different voltage source to the internal flash array, R6 should be removed and the new source applied to the CMD565 POWER_PORT pin for the VFLASH connection.

VDDRTC Voltage Source

The VDDRTC pin of the MPC565/6 is connected to the +2.6V supply by resistor R47 on the PM565/6-T board. To apply a different voltage source to the VDDRTC pin, R47 should be removed and the new source applied to the CMD565 POWER_PORT pin for the VDDRTC connection.

VFLS0 / 1 Signal Options - The VFLS0 and VFLS1 signals provided to the BDM_PORT are the default IWP0 and IWP1 shared signal pins. The default signal connections are provided by 0 ohm resistors R50 and R48 respectfully. To change from the default VFLS0 and VFLS1 signals to the alternate MGPIO port 3 and 4 provided signals, resistors R50 and R48 should be removed and 0 ohm resistors or jumper wire installed in the R51 and R49 resistor positions.

TROUBLESHOOTING

The MEM bank should contain the “Axiom MON5xx” EPROM’s and this bank only should be assigned CS0 to boot.

1. If trying to boot from external EPROM devices (U15 and U16) be sure the following are all true:
    a. MODE_SW1 switch 5 must be ON, MODE SW3 position 5 OFF.
    b. MAP_SW 1 and 4 must be OFF.
    c. The MEM_EN jumper must be installed.
    d. The CFG_EN jumper must be installed

2. If trying to boot from onboard FLASH devices (U15 and U16) be sure the following are all true:
    a. MODE_SW1 and 3 switch 5 must be OFF
    b. MEM_EN must be OPEN.
    c. MAP_SW position 4 on, 1 and 8 must be off.
    d. CFG_EN jumper must be installed

3. BDM hardware can cause a small amount of power to be supplied to the micro while connected, and thus prevent the processor from resetting properly. For this reason, you may need to disconnect the BDM device before applying power to the board. The RESET LED should flash briefly when the PWR_ON RESET switch is pressed and released - indicating a proper reset condition. The BDM can then be connected to the board and should communicate properly.

4. Make sure the PM-5xx module is properly seated by pressing down firmly on the center of the microcontroller.

5. Be certain that your software is located at a correct address corresponding to the device you're loading it into. The chip select jumpers on the board (MAP Switch) should be set to match the corresponding chip select registers (BR0-3, OR0-3) in your software.

6. The external EPROM devices (U15 and U16) are 8 or 16-bit device bus devices and any software on them should be configured as such. For example, the 32-bit version of the sample monitor program writes 0x400003 to the CS0 Base address register, while the 16-bit version writes 0x400803 to keep the proper bus width.

7. When connecting a serial cable to the board, make sure you're using a "strait-through" serial cable (such as the one provided).

8. If you get an exception error or if your program "hangs" or appears to jump out into unused memory, it is usually caused by trying to access "un-mapped" or improperly configured memory addresses. Look at the Memory Map page of this manual for the default memory map as set by the monitor program. Memory device location and address range is all configured under your software control at run-time (or the BDM configuration registers if using a BDM). These registers include the BR0 - BR3 registers as well as the OR0 - OR3 registers. Consult microcontroller manual for more information on these registers.

9. On power-up, all memory addresses are mapped to addresses 0x00000000 - 0x00400000, and mirrored at each successive 0x00400000 memory blocks. If booting externally (from CS0) your software must be located at a valid address when it changes the BR0 register. For example: The MPC555 resets at address 0x0100. The monitor starts at the first 40 0000 block following the internal block (see memory map). When the MPC555 resets, the code in the CS0 device - in this case the monitor - is mirrored to every 40 0000 block in the map. This allows the monitor to jump to the __start address + 40 0000. The monitor initialization code then re-maps CS0 to address 40 0000 and everything works ok.

10. If you want to re-map one of the external memory devices (flash for example) to the 0x0000 address space you may have an address conflict with the internal CMFI flash memory. To make this work you must disable the onchip flash (see the FLEN bit of the IMMR register in the MPC5xx documentation). You can then relocate your code with interrupt handlers at 0x0, running out of external memory. Writing 0xFFF00000 to the SPR638 register in your BDM configuration file does this so you can debug external memory mapped at the 0x0 address space.

Contact support@axman.com for additional help or information. The MEM bank should contain the “Axiom MON5xx” EPROM’s and this bank only should be assigned CS0 to boot.