i.MX25 PDK Hardware

User's Guide

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About This Book

This document explains how to connect and operate the i.MX25 3-Stack Platform System.

Audience

This document is intended for software, hardware, and system engineers who are planning to use the product and for anyone who wants to understand more about the product.

Organization

This document contains the following chapters.

Chapter 1	Introduces the features and functionality of the 3-Stack board.
Chapter 2	Provides configuration and setup information.
Chapter 3	Provides block diagrams and memory mapping.
Chapter 4	Provides functional operation information.
Chapter 5	Describes the multiplexing pin signals.

Conventions

This document uses the following conventions:

`Courier`	Is used to identify commands, explicit command parameters, code examples, expressions, data types, and directives.
Italic	Is used for emphasis, to identify new terms, and for replaceable command parameters.

Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

APMS	Atlas Power Management System
ATA	Hard drive interface spec
CD	Compact Disk
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Custom Programmed Logic Devices
CPU	Central Processing Unit
CSI	Camera Sensor Imaging
CSPI	Serial Peripheral Interface
DCE	Data Communications Equipment
DDR	Double Data Rate
DIP	Dual In-line Package
DMA	Direct Memory Access

DTE	Data Terminal Equipment
DUART	Dual Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
FIR	Infra Red
GPIO	General Purpose Input/Output
GPO	General Purpose Output
I^2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
I/O	Input/Output
IrDA	Infrared Data Association
ISA	Instrumentation, System, and Automation Society
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-media Card
MCP	Multi-chip product
MS	Memory Stick
NVRAM	Non-volatile Random Access Memory
OTG	On the Go
PC	Personal Computer
PCMCIA	Personal Computer Memory Card International Association
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on Reset
PSRAM	Pseudo Random Access Memory
PWM	Pulse Width Modulation
QVGA	Graphics Adapter
RAM	Random Access Memory
SD	SanDisk (Smart Media)
SDRAM	Synchronous Dynamic Random Access Memory
SI	System International (international system of units and measures)
SIMM	Single In-Line Memory Module
SPST	Single Pole Single Throw
SSI2	Synchronous Serial Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Chapter 1
Introduction

The i.MX25 3-Stack Platform System helps you to develop multimedia communication applications using the i.MX25 ARM-9 CPU and the MC34704 power management chip.

The 3-Stack consists of a CPU Engine board, a Personality board and a Debug board. The system supports application software development, target board debugging, and optional circuit cards. The CPU board can be run in stand-alone mode for code development. A 5’7 LCD display panel is supplied with the 3-Stack.

Figure 1-1 shows the major components of the 3-Stack system.

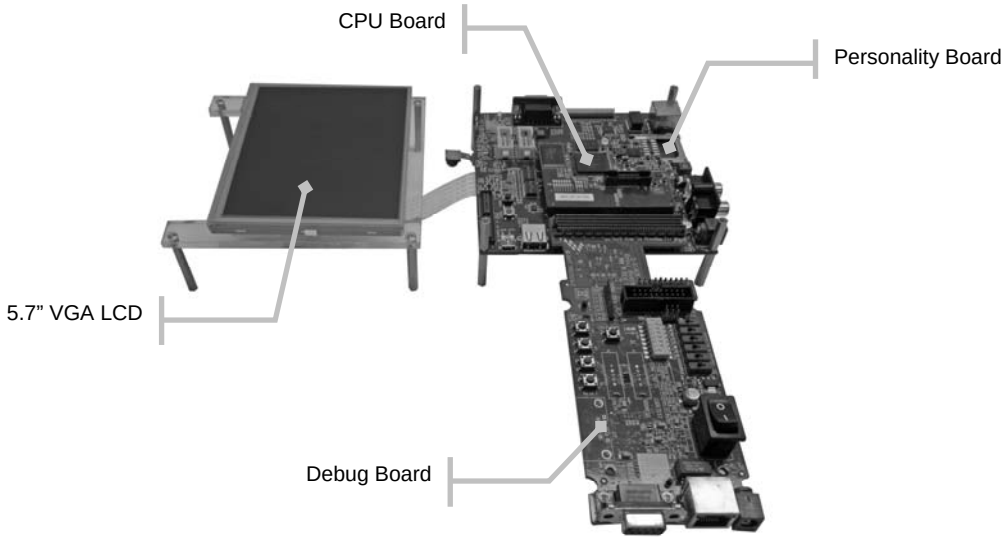

Figure1-1 Major Components of the 3-Stack

1.1 Features

The 3-Stack system can be used in two ways: the development mode requires a three-board assembly; the demonstration mode requires only a two-board assembly (without the Debug board).

The system includes the following features.

- Near form-factor demonstration modules and working platforms.
- Solid reference schematics that closely resemble final products to aid customers' designs.
- Three-board system, which includes:
  - — - CPU board with i.MX25 ARM-9 CPU, MC34704 chip
  - — - Personality board with peripheral components and interface connectors
  - — - Debug board with two RS232 interfaces, 10/100 Base-T Ethernet connector, and current measure connectors.
- Utilizes reliable high-density connector to interface between boards.

Figure 1-2 illustrates the three-board assembly, which can be set up for software development (three boards) or demonstration (two boards).

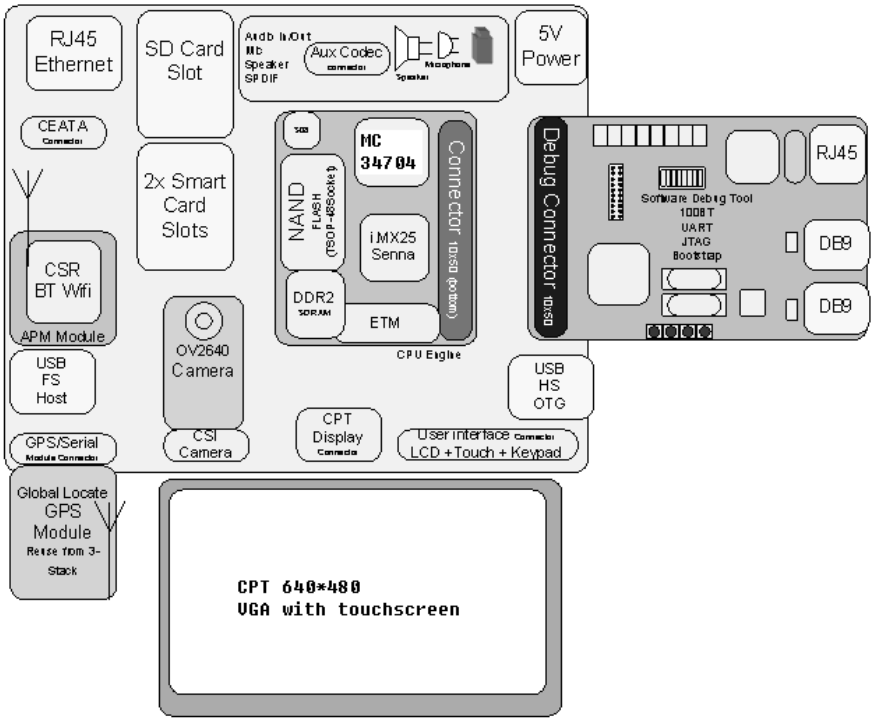

Figure1-2 3-Stack Primary Boards

1.2 Components

Table 1.1 describes the i.MX25 board components.

Table 1.1 Board Components

Item	Description
CE-ATA connector	One CE-ATA connector (not populated)
Audio codec header	Audio codec header to connect the audio feature card
Camera connector	Two image sensor camera connector which can support OV2640 and OV3640 (OV3640 not populated)
CAN bus connectors	One DB9 connector for the CAN bus, and one 10-pin connector for the CAN bus
Clocks	Two selectable system clock sources: 32.768KHz or 24Mhz
DDR2 memory	64MB of 16 bit DDR2 memory
Debug support	RealView-ICE® debug support
Flash memory, NAND	2 GB of MLC NAND Flash Memory
GPS connector	One connector to out board GPS module
Jacks and speaker terminals	Microphone jack, headphone and line in jack, stereo and mono (ear piece) speaker terminals
Keypad	On board keypad matrix.
Network connector	Ethernet network connector driven by internal FEC and DP83640 external PHY
Power management	Configurable intelligent management of system power through power management chip MC34704
Power supply	+5.0 VDC, 3 A universal power supply
Reset	Push button reset on CPU or reset control from MC34704 chip
SD card connectors	Card sense functionality.
Smart card connectors	Two Smart card connectors on Personality board
USB host transceiver	One USB fast-speed host transceiver, with standard USB host connector
USB OTG	One USB On-the-Go (OTG) high-speed transceiver with microAB USB connector
VGA LCD	5.7 inch LCD display panel with touch panel and LED backlight
WVGA LCD Connector	7 inch WVGA display panel connector with touch panel as optional LCD (not included)

1.3 System and User Requirements

You will need a PC that includes:

- Windows 98™, ME™, 2000™, XP™, or NT ™ (version 4.0) operating system
- One +5VDC, 2.4A power supply with a female (inside positive) power connector (included)

CAUTION

Never supply more than +5.5 V power to the i.MX25 3-Stack. Doing so can damage board components.

1.3.1 System Operating Specifications

Table 1.2 identifies the clock, environmental conditions, and dimensions of the i.MX25 3-Stack system.

Table 1.2 System Operating Specifications

Item	Specifications
Clock	Selectable 32.768KHz or 24 MHz
Temperature: Operating Storage	 -10 °C to + 50 °C -40 °C to +85 °C
Relative Humidity	0 to 90% (noncondensing)
Power Requirements	4.5V to 5.5 V DC @3 A
Dimensions	CPU Engine board: 61mm x 71 mm Personality board: 127mm x 127 mm Debug board: 71.400mm x 174.900mm

Chapter 2
Configuration and Connections

This section contains configuration information, connection descriptions, and other operational information that may be useful during the development process.

2.1 Debug Board Configuration

The Debug board provides an interface for programming and debugging the i.MX development systems and reference platforms.

The Debug board is a small card that you can insert or remove from the platform. The ability to remove the Debug board is a major advantage to marketing and sales teams who want to demonstrate and showcase a variety of products and ideas in a streamlined, near form factor way, without the added software development bulk.

2.1.1 Debug Board Top Switches and Connectors

Figure 2-1 identifies the switches and connectors located on the top of the Debug board. Table 2.1 describes the switches and connectors.

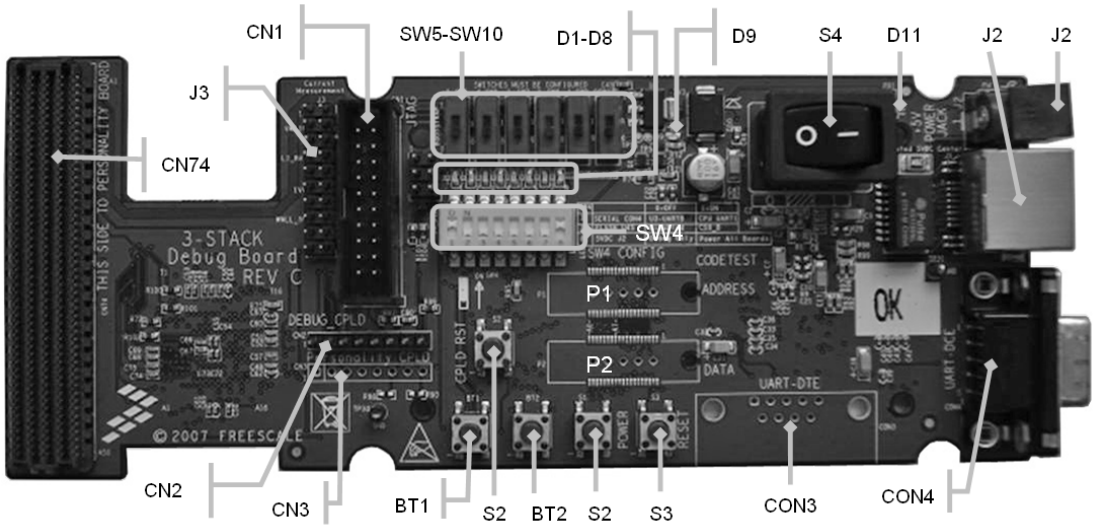

Figure 2-1 Debug Board Top View

Table 2.1 Debug Board, Top Components

Identifier	Component	Description
S1	Power Button	Connected to the ON1B input of the MC13783 through the 500 pin connector. The line is pulled up, and pushing it grounds the line. If MC13783 is in Off, User Off or Memory Hold Mode, the board can be powered on via pushing the button.
S2	Reset Button	Resets the Debug board.
S3	System reset switch	Connects the RESETB to MX35 The line is pulled up; pushing it grounds the line.
S4	Power on switch	Powers up the Debug board when set to 0.
J1	Ethernet connector	10/100 Base T Ethernet RJ45 Connector
J2	Power connector	5.0V DC power connector
J3	Current measurement connector	Measures the current at various points of CPU Engine and Personality board from the connector.
F1	Fuse	Re-settable fuse; re-settable over-current protection
D1 – D8	LEDs	LEDs for CPLD debug
D9	LED	LED for Debug board 3.3V power; lights when turned ON.
D11	LED	LED for DC power supply; lights when 5.0V DC power is applied
P1	WEIM Address measurement connector	Supports the CodeTest Interface Probe
P2	WEIM Data measure connector	Supports the CodeTest Interface Probe
BT1, BT2	Test buttons	Test buttons for CPLD
CN1	Connector	i.MX25 JTAG connector
CN2	Connector	Debug board CPLD JTAG connector
CN3	Connector	Personality board CPLD JTAG connector (Reserved)
CN74	Connector	500 pin connector to the Personality board
CON3	Connector	UART (DCE) DB9 male connector
CON4	Connector	UART (DCE) DB9 female connector
SW4	Enable switch	Switch designation settings (see next table):

Switch Designation	Setting	Effect
SW4-1 UART Port Select	ON	Serial port UART (DTE) CON3 is selected.
	OFF	Serial port UART (DCE) CON4 is selected.
SW4-2 NorFlash Enable	ON	Enable NorFlash on Debug board
	OFF	Disable Norflash on Debug board
SW4-8 Power Enable	ON	Power supply to three boards
	OFF	Power supply to Debug board only

2.1.2 Boot Mode Switches

Settings for SW9 and SW10 determine where the processor begins program execution. Table 2.2 shows the valid combinations of the switches.

Table 2.2 Boot Mode Settings

Boot Mode Device	SW5	SW6	SW7	SW8	SW9	SW10
UART/USB bootloader	X	0	0	0	1	1
8-bitNAND Int, SD/MMC and SPI Flash	X	0	0	0	0	0

2.1.3 Debug Board Bottom Connectors

Figure 2-2 illustrates the bottom view of the Debug board, where J4 identifies the 500-pin connector to the CPU Engine board, and F1 is the resettable fuse that provides overcurrent protection.

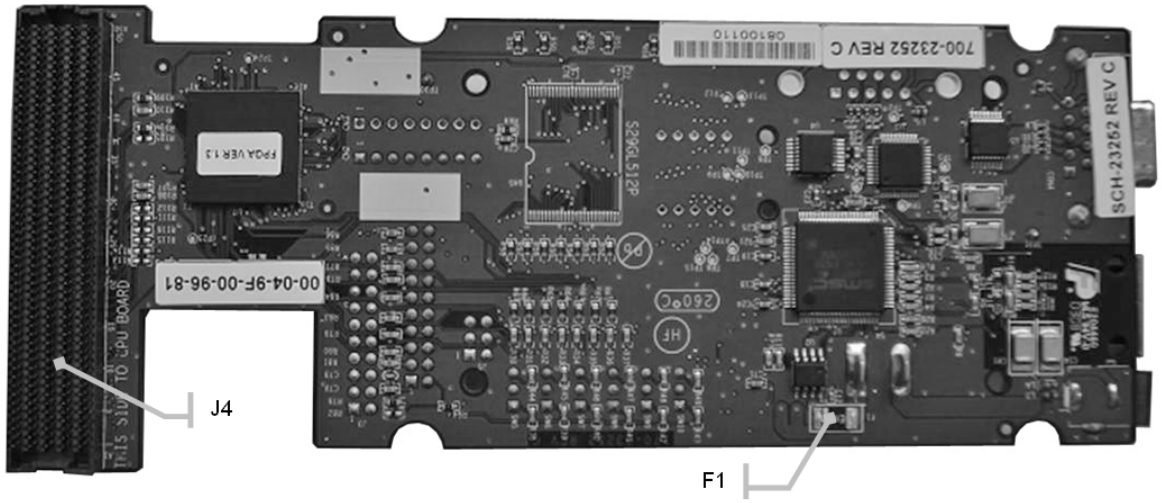

Figure2-2 Debug Board, bottom view

2.2 Personality Board Connectors

This section describes the switches and connectors on the top of the Personality board, and the connectors on the bottom of the Personality board.

2.2.1 Personality Board Top Connectors

Figure 2-3 identifies the connectors on the top of the Personality Board.

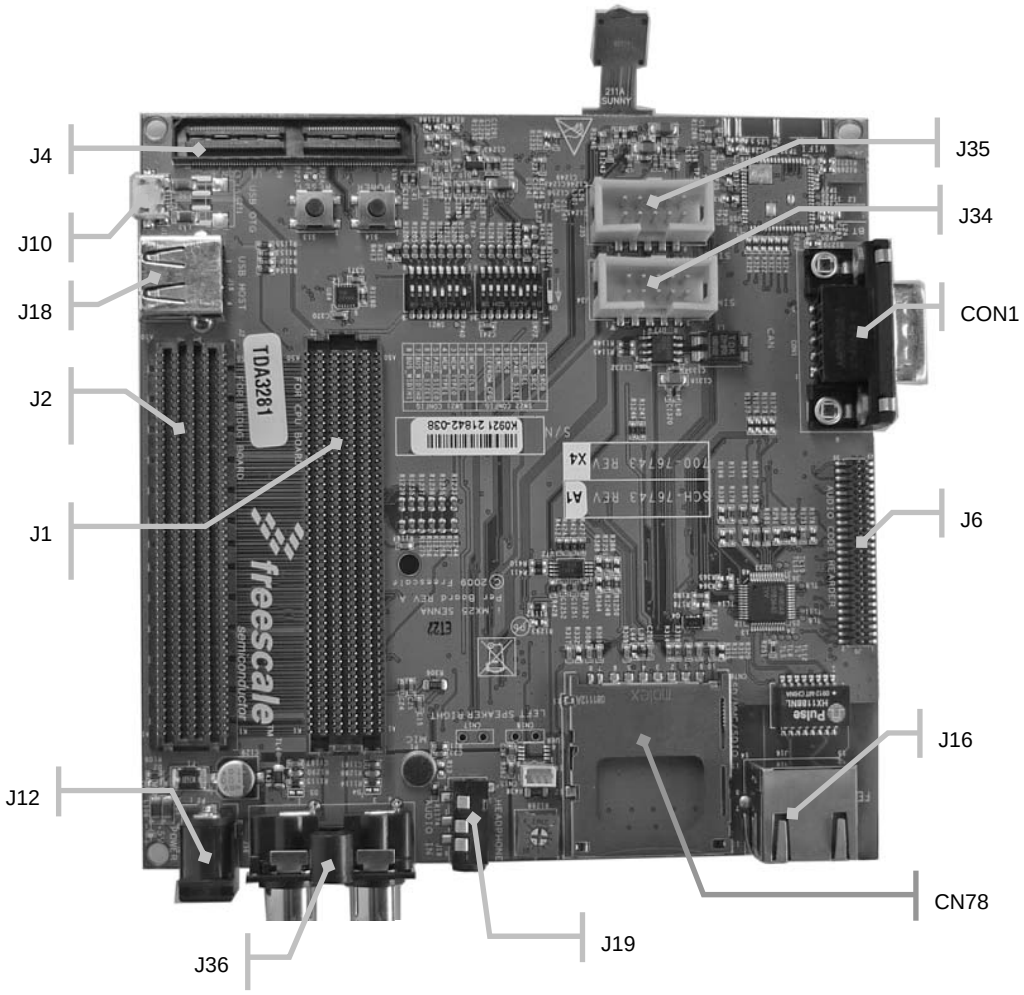

Figure 2-3 Personality Board Top View

Table 2.3 Personality Board Connectors, top

Component Identifier	Description
J12	5.0V DC power connector
J36	Line-in connector
J19	Audio jack
J6	ESAI connector
J16	10/100BT Fast Ethernet Connector
J34	SIM1 connector
J35	SIM2 connector
J4	U/I connector
J2	500 pin connector for connecting the Debug board
J1	500 pin connector for connecting the CPU board
J10	USB OTG connector
J18	USB Host connector
CON1	CAN bus connector
P3	MLB module connector
P4	I2C connector
CON1	CAN connector
CN78	SD Card socket
S13	RESET button
S14	POWER ON button
SW21, SW22	Boot config switch. Below is the detail function list

Switch Setting	Configuration
NAND Flash Boot Configuration	
SW21	1, 4 and 5 ON the rest OFF
SW22	3 ON the rest OFF
SD/MMC Card Boot Configuration	
SW21	1 and 2 ON the rest OFF
SW22	All OFF
SPI Flash Boot Configuration	
SW21	1,2,3,4 and 7 ON the rest OFF
SW22	All OFF
Bootstrap Mode Configuration (Used by ATK and RV-ICE)	
SW21	Ignored
SW22	Ignored

2.2.2 Personality Board Bottom Connectors

Figure 2-4 illustrates the bottom view of the Personality board. Table 2.4 describes the connectors.

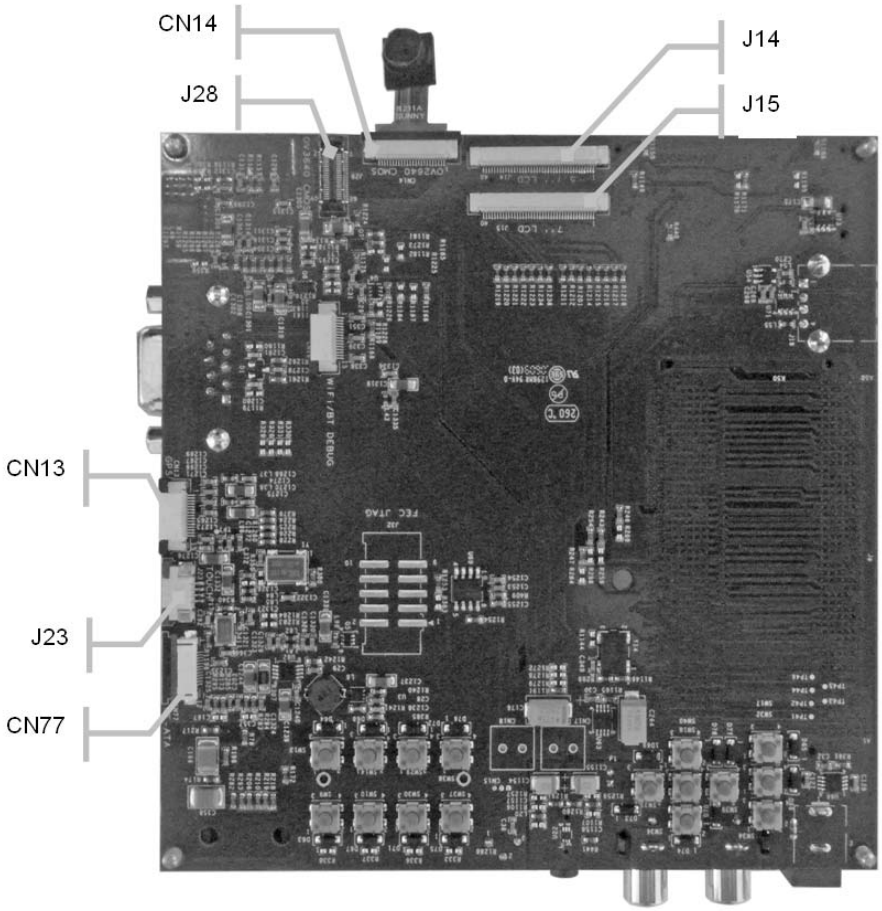

Figure2-3 Personality Board, bottom view

Table 2.4 Personality Board Bottom Connectors

Component Identifier	Description
CN77	CE-ATA connector
J14	VGA 5.7 inch LCD connector
J15	WVGA 7 inch LCD connector
J23	WVGA 7 inch LCD Touch Panel connector
J28	CMOS OV3640 module connector (not populated)
CN14	CMOS OV2640 module connector
CN23	GPS module connector

2.3 CPU Board Connectors

2.3.1 CPU Board Top Connector

Figure 2-5 illustrates the top of the CPU board, where P1 is the ETM Connector (not populated).

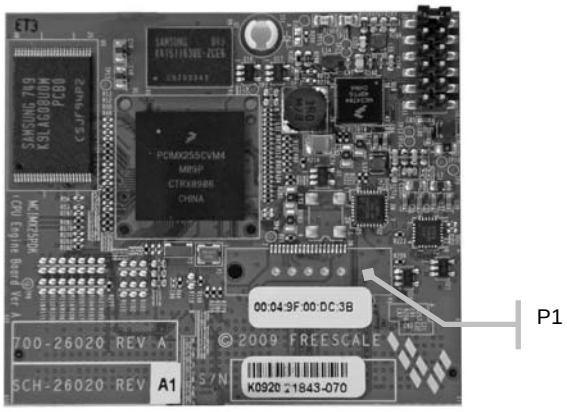

Figure2-4 CPU Board, top view

2.3.2 CPU Board Bottom Connector

Figure 2-6 illustrates the bottom view of the CPU Engine board, where J2 is the 500-pin connector to the Personality board.

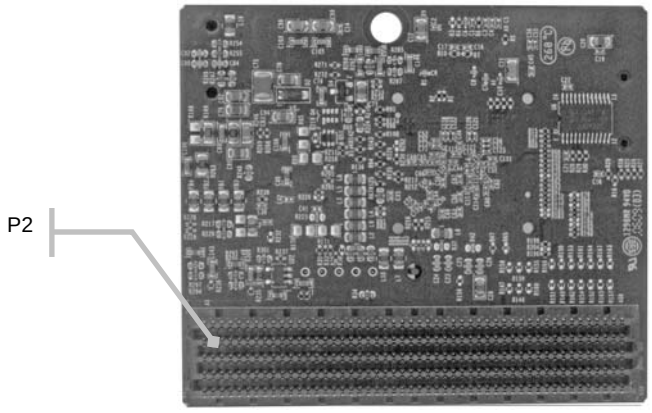

Figure2-5 CPU Engine Board, Bottom View

2.4 Setting Up the 3-Stack Platform

2.4.1 Set the Debug Board Switches

To set the Debug board switches, use these steps:

1. Set CPU Engine and Personality board power enable switch SW4-8.
2. Set Boot Mode Switches, SW9 and SW10.

2.4.2 Connect the CPU and Debug Boards to the Personality Board

Figure 2-7 illustrates the connected boards.

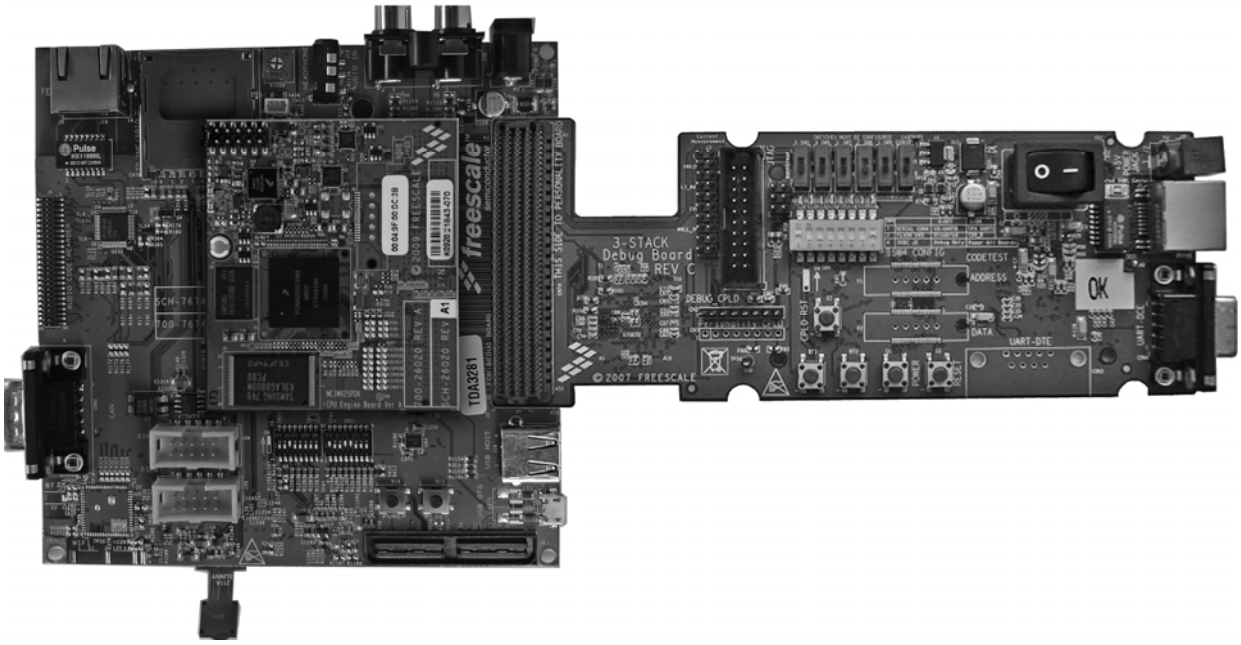

Figure2-6 Connected Boards

2.4.3 Connect the CPU Engine board with Personality board

In Demo Mode the CPU Engine board can be connected with Personality board directly without Debug board.

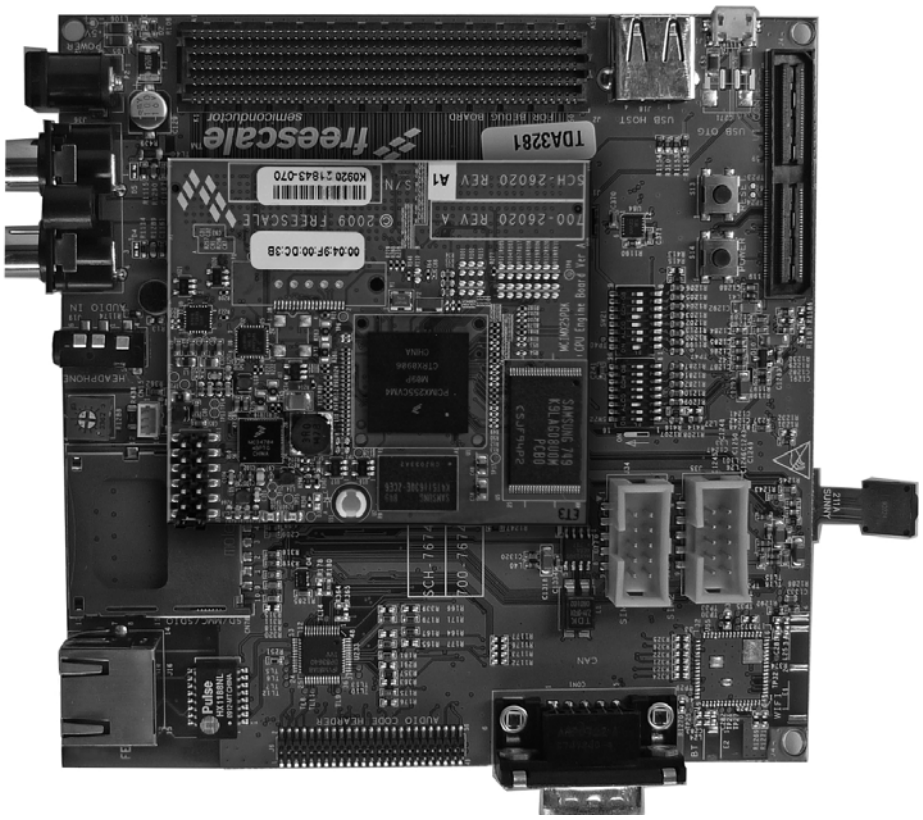

Figure2-7 Connecting the CPU Engine board to Personality board

2.4.4 Connect Power to the 3-Stack

The 3-Stack boards provide two DC power jacks: one in the Debug board and one in the Personality board (Figure 2-10).

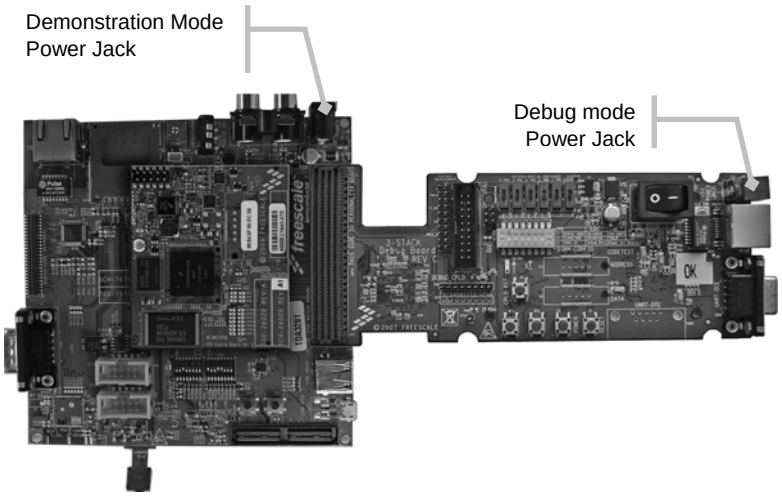

Figure2-8 3-Stack Power Input

For software development, the three boards are assembled together. The 5.0V DC power should be plugged into the Debug board DC power jack. Press S4 on Debug board to "0" in order to power on the 3-Stack.

For demonstration purposes, the Personality board and CPU Engine board are assembled together, without the Debug board. The 5.0V DC power should be plugged into the Personality board DC power jack. The 3-Stack will be powered on directly.

Chapter 3
Functional Operation

3.1 Functional Block Diagrams

Figure 3-1 illustrates the functional blocks of 3-Stack.

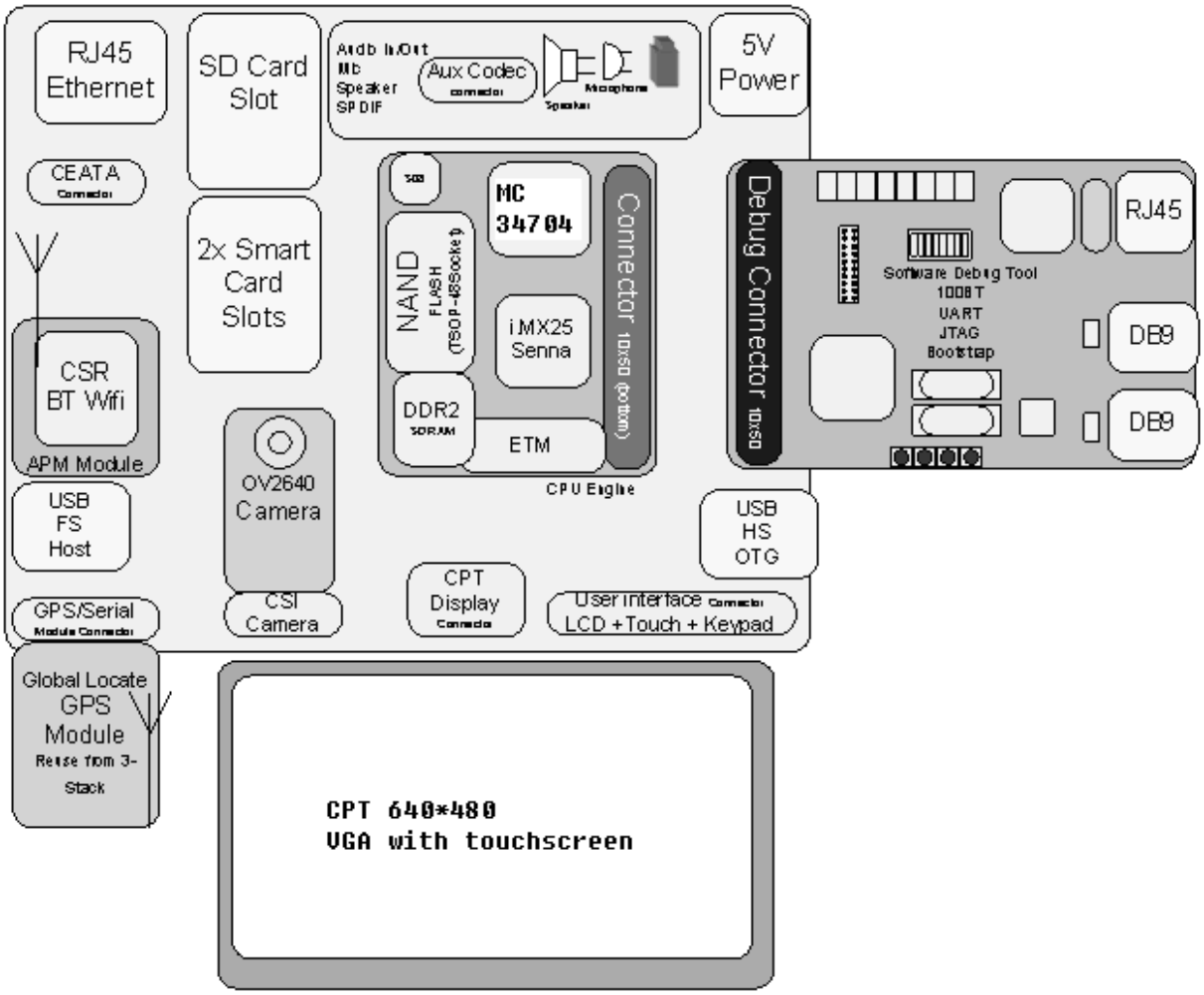

Figure3-1 i.MX25 3DS Functional Block

3.2 3-Stack Memory Map

Table 3.1 describes the memory map for the 3-Stack system. None of the memories take up the entire address space of the associated chip selects, and the software can access the same physical memory location at more than one range of address. For instance, DDR SDRAM occupies only 128 MB of the 256MB space available to CSD0, so it appears in two different ranges of addresses.

Table 3.1 Memory Map

Peripheral	Chip Select	Address Range (HEX)	Size
DDR2	$\overline{\text{CSD0(CS2)}}$	0x8000_0000 to 8FFF_FFFF	128MB

3.3 CPLD on the Debug Board

A complex programmable logic device (CPLD) is an electronic component used to build reconfigurable digital circuits. The CPLD provides a great deal of functionality, including glue logic, which is needed to achieve compatible interfaces between two (or more) different off-the-shelf integrated circuits. For the 3-Stack board, glue logic provides peripheral bus address decoding, board control and status signals, board revision registers, and other functions, and is implemented with a CPLD on the Debug board.

3.3.1 CPLD Features

The CPLD provides the following key features:

- Address decode and control for the Ethernet controller
- Address decode and control for the external UART controller
- Level shift for Ethernet signals and UART signals
- Control and status registers for various board functions

3.3.2 CPLD Memory Map

Table 3.2 CPLD Memory Map

CS5_B	A16	A15	A14	A5	A4	A3	A2	Description
0	0	0	0	x	x	x	x	SMSC LAN9217 Ethernet 10/100BT
0	0	0	1	x	x	x	x	External UART-A
0	0	1	0	x	x	x	x	External UART-B
0	0	1	1	x	x	x	x	Reserved
0	1	0	0	0	0	0	0	Read/Write LED's (1=on, 0=off)
0	1	0	0	0	0	0	1	Read Only Switches/Buttons
0	1	0	0	0	0	1	0	Read Only Status - Interrupts, Interrupt latch
0	1	0	0	0	0	1	1	Read/Write - Interrupt Mask
0	1	0	0	0	1	0	0	Write - Interrupt reset
0	1	0	0	0	1	0	1	R/W Software Override: Set UART-B/CPU UART routing
0	1	0	0	0	1	1	0	R/W Software Override: Enable/Disable Flash Access, select CSx
0	1	0	0	0	1	1	1	Software Override 3 reserved
0	1	0	0	1	0	0	0	Read Only Returns AAAA
0	1	0	0	1	0	0	1	Read Only Returns 5555
0	1	0	0	1	0	1	0	Read Only CPLD Code Version #
0	1	0	0	1	0	1	1	Read Only Returns CAFÉ
0	1	0	0	1	1	0	0	Reserved

Table 3.3 SPI Write Operation

Counter	Memory Signal	Input	Output	Description
0	NA	1	NA	Designates operation as a write
1	CS5_B	1	NA	Memory map initinally not selected
2	A[16]	Address	NA	Input 17 bit address
3	A[15]	Address	NA	Input 17 bit address
4	A[14]	Address	NA	Input 17 bit address
5	A[13]	Address	NA	Input 17 bit address
6	A[12]	Address	NA	Input 17 bit address
7	A[11]	Address	NA	Input 17 bit address
8	A[10]	Address	NA	Input 17 bit address
9	A[9]	Address	NA	Input 17 bit address
10	A[8]	Address	NA	Input 17 bit address
11	A[7]	Address	NA	Input 17 bit address
12	A[6]	Address	NA	Input 17 bit address
13	A[5]	Address	NA	Input 17 bit address
14	A[4]	Address	NA	Input 17 bit address
15	A[3]	Address	NA	Input 17 bit address
16	A[2]	Address	NA	Input 17 bit address
17	A[1]	Address	NA	Input 17 bit address
18	A[0]	Address	NA	Input 17 bit address
19	CS5_B	0	NA	Select memory map
20	WR_B	1	NA	Write not enabled until data is input
21	WR_B	1	NA	Write not enabled until data is input
22	WR_B	1	NA	Write not enabled until data is input
23	WR_B	1	NA	Write not enabled until data is input
24	D[15]	Data	NA	Input 16 bit data
25	D[14]	Data	NA	Input 16 bit data
26	D[13]	Data	NA	Input 16 bit data
27	D[12]	Data	NA	Input 16 bit data
28	D[11]	Data	NA	Input 16 bit data
29	D[10]	Data	NA	Input 16 bit data
30	D[9]	Data	NA	Input 16 bit data
31	D[8]	Data	NA	Input 16 bit data
32	D[7]	Data	NA	Input 16 bit data
33	D[6]	Data	NA	Input 16 bit data

Counter	Memory Signal	Input	Output	Description
34	D[5]	Data	NA	Input 16 bit data
35	D[4]	Data	NA	Input 16 bit data
36	D[3]	Data	NA	Input 16 bit data
37	D[2]	Data	NA	Input 16 bit data
38	D[1]	Data	NA	Input 16 bit data
39	D[0]	Data	NA	Input 16 bit data
40	WR_B	1	NA	Write not enabled
41	WR_B	0	NA	Write enabled, load data to registers
42	WR_B	0	NA	Write enabled, load data to registers
43	WR_B	1	NA	Write not enabled, data loading done
44	WR_B	1	NA	Write not enabled, data loading done
45	CS5_B	1	NA	Deselect memory map, write is done

Table 3.4 SPI Read Operation

Counter	Memory Signal	Input	Output	Description
0	NA	1	NA	Designates operation as a read
1	CS5_B	1	NA	Memory map initially not selected
2	A[16]	Address	NA	Input 17 bit address
3	A[15]	Address	NA	Input 17 bit address
4	A[14]	Address	NA	Input 17 bit address
5	A[13]	Address	NA	Input 17 bit address
6	A[12]	Address	NA	Input 17 bit address
7	A[11]	Address	NA	Input 17 bit address
8	A[10]	Address	NA	Input 17 bit address
9	A[9]	Address	NA	Input 17 bit address
10	A[8]	Address	NA	Input 17 bit address
11	A[7]	Address	NA	Input 17 bit address
12	A[6]	Address	NA	Input 17 bit address
13	A[5]	Address	NA	Input 17 bit address
14	A[4]	Address	NA	Input 17 bit address
15	A[3]	Address	NA	Input 17 bit address
16	A[2]	Address	NA	Input 17 bit address
17	A[1]	Address	NA	Input 17 bit address
18	A[0]	Address	NA	Input 17 bit address
19	CS5_B	0	NA	Select memory map

Counter	Memory Signal	Input	Output	Description
20	OE_B	1	NA	Write not enabled
21	OE_B	0	NA	Read enabled prior to data output
22	OE_B	0	NA	Read enabled prior to data output
23	OE_B	0	NA	Read enabled prior to data output
24	D[15]	NA	Data	output 16 bit data
25	D[14]	NA	Data	output 16 bit data
26	D[13]	NA	Data	output 16 bit data
27	D[12]	NA	Data	output 16 bit data
28	D[11]	NA	Data	output 16 bit data
29	D[10]	NA	Data	output 16 bit data
30	D[9]	NA	Data	output 16 bit data
31	D[8]	NA	Data	output 16 bit data
32	D[7]	NA	Data	output 16 bit data
33	D[6]	NA	Data	output 16 bit data
34	D[5]	NA	Data	output 16 bit data
35	D[4]	NA	Data	output 16 bit data
36	D[3]	NA	Data	output 16 bit data
37	D[2]	NA	Data	output 16 bit data
38	D[1]	NA	Data	output 16 bit data
39	D[0]	NA	Data	output 16 bit data
40	OE_B	0	NA	Read enabled after data output
41	OE_B	1	NA	Read not enabled, data output done
42	OE_B	1	NA	Read not enabled, data output done
43	OE_B	1	NA	Read not enabled, data output done
44	OE_B	1	NA	Read not enabled, data output done
45	CS5_B	1	NA	Deselect memory map, read is done

3.3.3 Programming the CPLD

To program the CPLD, use these steps:

1. Install Lattice ispLEVER Project Navigator Ver 6.0 on the PC.
2. From the **Start** menu, select **Programs** > **Lattice Semiconductor** > **Accessories** > **ispVM System**.
3. Connect the **Lattice CPLD ispDOWNLOAD Cable** to the PC parallel port.
4. Attach the **JTAG** connector to **CN2** on the Debug board.
5. Power on the Debug board.
6. Scan **Chain**.

   The CPLD device list is displayed (Figure 3-2).

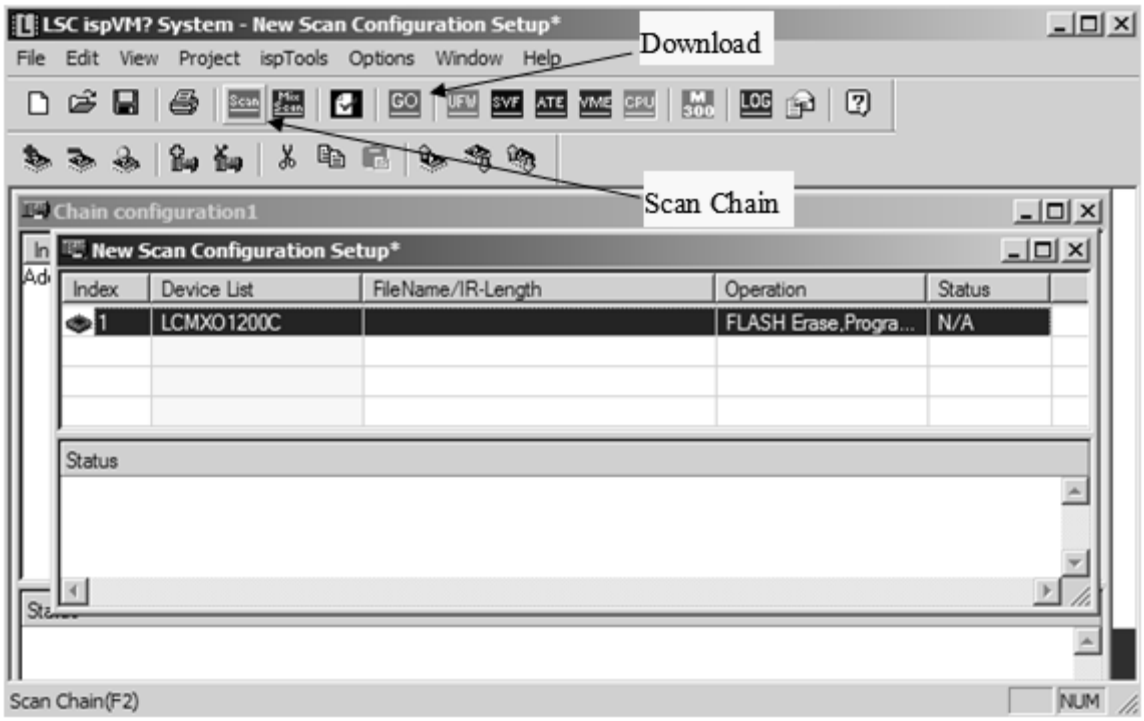

Figure3-2 Scan CPLD Devices

7. Double-click **LCMXO1200C**.
8. Select the CPLD data file (Figure 3-3).

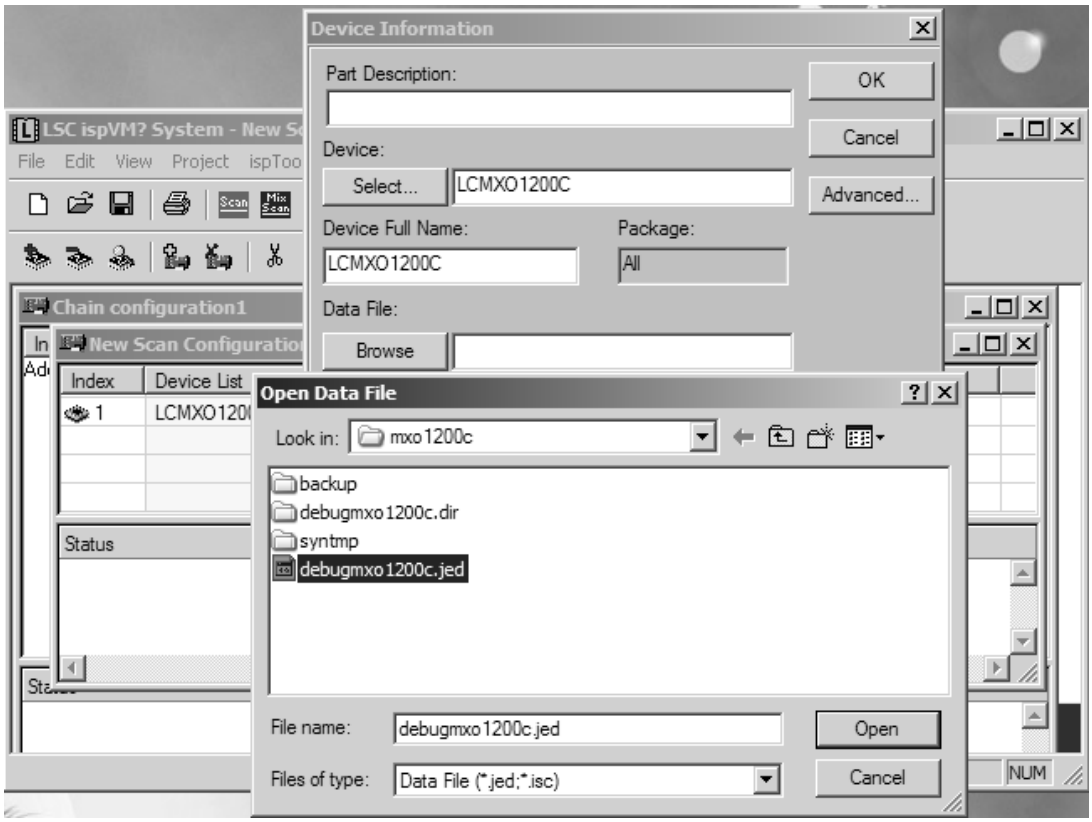

Figure 3-3 Selecting the CPLD Data File

9. Click GO to download the data file in the CPLD.
10. Wait about 10 seconds.

    When the Status section displays **PASS**, programming the CPLD is completed.

3.4 i.MX25 GPIO Grouping

The i.MX25 3-Stack uses an MCU and its GPIO to perform control operations. Table 3.5 describes the GPIO pins.

Table 3.5 MCU GPIO Grouping Descriptions

Pin Name	Description
A10	Headphone detect
A14	SD1_WP
A15	SD1_DET
A16	GPS_INT_B
A17	FEC_Enable
A18	SSI_Reset
A19	CSI_PWDN
A20	CMOS_RST_B
A21	USB_BT_CS
A22	ParallelConnect_GPIO
A23	HDD_PWR_EN
A24	CODEC_CTRL
A25	ON_OFF
D8	GPS_PWEN
D9	GPS_RST
D10	WiFi_BT_RST_B
D11	WiFi_PWEN
D12	FEC_RESET_B
D13	AudioAMP_Shutdown_B
D14	CAN_PWDN
D15	LCD_LCS1_RST
CS0	GPIO_CLAMSHELL
ECB	SD2_DET
LBA	SD2_WP
EXT_ARMCLK	ESAI_GPIO
VPLL_BYPCLK	ESAI_RST_B
VSTBY_REQ	LCD_EN
VSTB_ACK	GPS_CLK_EN
POWER_FALL	FEC_PWDN
PWM	DEBUG_INT_B
GPIO_B	USB_OTG_OC
GPIO_A	USB_OTG_EN

Chapter 4
Connectors and Signals

This chapter provides connector pin assignments and signals for i.MX25 3-Stack CPU, Personality, and Debug boards.

- The tables in this section list signal names as they appear in the board schematics.
- The use of "_B" at the end of a name indicates an active low signal.

4.1 500 Pin Board to Board Connector

Table 4-1 500 Pins Connector Pin-Out

c	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row J	Row K
1	GND	USB_5V_VBUS	GND	CURRENT_MEAS_1	AUDIO_LIN_R	AUDIO_LIN_L	AUDIO_LOUT_R	AUDIO_LOUT_L	TOUCH_X0	TOUCH_Y0
2	LI_BATTERY	USB_5V_VBUS	VMAIN	CURRENT_MEAS_2	RFU	GND	HEADPHONE_RIGHT	HEADPHONE_LEFT	TOUCH_X1	TOUCH_Y1
3	LI_BATTERY	GND	VMAIN	GND	MIC_IN_P	RFU	HEADPHONE_RETURN	GND	GND	GND
4	GND	3V3	GND	CURRENT_MEAS_3	MIC_BIAS	BOOTSTRAP_0	SPEAKER_RIGHT_P	SPEAKER_LEFT_P	TV_DAC_C_RETURN	TV_DAC_C
5	1V8	3V3	LINEAR_A	CURRENT_MEAS_4	HEADPHONE_DETECT	BOOTSTRAP_1	SPEAKER_RIGHT_N	SPEAKER_LEFT_N	TV_DAC_B_RETURN	TV_DAC_B
6	1V8	GND	LINEAR_B	GND	ADC_1	BOOTSTRAP_2	GND	GND	TV_DAC_A_RETURN	TV_DAC_A
7	GND	WALL_5V_IN	LINEAR_C	CURRENT_MEAS_5	ADC_2	BOOTSTRAP_3	SIM2_CLK	SPDIF2	SIM_CLK	SIM_RX
8	LCD_BKLT_18MA_RETURN	WALL_5V_IN	GND	CURRENT_MEAS_6	GND	BOOTSTRAP_4	SSI_RST	RFU	SIM_RST	SIM_PD
9	LCD_BKLT_18MA_BOOST	GND	LINEAR_D	GND	ADC_3	BOOTSTRAP_5	SIM2_RST	RFU	SIM_VEN	SIM_TX
10	BKLT_5V_60MA_A	2V775	LINEAR_E	CURRENT_MEAS_7	ADC_4	VDD_BOOTSTRAP	SIM2_VEN	VDD_CSI_IO	VDD_SIM_IO	JTAG_TRST_B
11	BKLT_5V_60MA_K	2V775	LINEAR_F	CURRENT_MEAS_8	ADC_5	DAC	SIM2_RX	GND	CHRG_LED	JTAG_TDI
12	DEBUG_INT_B	RFU	SLEEP_VSTBY	CURRENT_MEAS_9	ADC_6	RFU	CSI_RESET_B	CSI_HSYNC	VDD_JTAG	JTAG_TMS
13	MASTER_RESET_B	RFU	GND	CURRENT_MEAS_10	GND	RFU	CSI_PWDN	CSI_VSYNC	CODEC_CTRL	JTAG_TCK
14	OSC_32KHz	BATTERY_TEMP	ON_OFF	LCD_EN	CAN_PWDN	GND	KP_ROW_7	CSI_MCLK	CPLD_PGM_TDI	GND
15	GND	OSC_26MHZ	LI_CELL	WIFI_PWEN	ESAI_TX0	ESAI_TX1	KP_ROW_6	GND	CPLD_PGM_TDO	JTAG_RTCK
16	UART2_RX	RFU	VDD_I2C_IO	VDD_USB_IO	ESAI_TX2_RX3	ESAI_TX3_RX2	KP_ROW_5	CSI_PIXCLK	CPLD_PGM_TMS	JTAG_DE_B
17	UART2_TX	RFU	I2C1_DATA	ESAI_GPIO	ESAI_TX4_RX1	ESAI_TX5_RX0	KP_ROW_4	CSI_D0	CPLD_PGM_TCK	JTAG_TDO
18	UART2_CTS	RFU	I2C1_CLOCK	ESAI_RST_B	ESAI_FSR	ESAI_FST	KP_ROW_3	CSI_D1	SSI1_STXD	JTAG_RESET_B
19	UART2_RTS	RFU	GND	HDD_PWR_EN	ESAI_SCKR	ESAI_SCKT	KP_ROW_2	GND	SSI1_SRXD	MLB_SIG
20	UART3_RX	GND	I2C2_CLOCK	HDD_DMARQ	ESAI_HCKR	ESAI_HCKT	KP_ROW_1	CSI_D2	SSI1_SFS	MLB_DAT
21	UART3_TX	RFU	I2C2_DATA	HDD_DIOW	GND	RFU	KP_ROW_0	CSI_D3	GND	MLB_CLK
22	UART3_CTS	RFU	CSPI1_MOSI	HDD_DIOR	HDD_D0	FEC_TXD2	KP_COL_7	CSI_D4	SSI1_SCK	RFU
23	UART3_RTS	DEBUG	GND	HDD_IORDY	HDD_D1	FEC_TXD3	KP_COL_6	GND	SSI2_STXD	CAN TX1 RFU
24	UART1_RX	PERSONALITY1	CSPI1_MISO	HDD_DMACK	HDD_D2	FEC_RX_ER	KP_COL_5	CSI_D5	SSI2_SRXD	CAN RX1 RFU

c	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row J	Row K
25	UART1_TX	PERSONALITY2	CSPI1_SS0	HDD_INTRQ	GND	FEC_TXD0	KP_COL_4	CSI_D6	GND	CAN TX2 RFU
26	UART1_CTS	PERSONALITY3	CSPI1_SS1	HDD_DA1	HDD_D3	FEC_RXD1	KP_COL_3	CSI_D7	SSI2_SFS	CAN RX2 RFU
27	UART1_RTS	CPU1	GND	HDD_DA0	HDD_D4	FEC_RXD2	KP_COL_2	GND	SSI2_SCK	VDD_MLB
28	RFU	CPU2	CSPI1_SCLK	HDD_CS0	HDD_D5	FEC_RXD3	KP_COL_1	CSI_D8	SD1_D0	SD1_CMD
29	VDD_LCDIO	CPU3	CSPI1_RDY	HDD_DA2	GND	FEC_TXD1	KP_COL_0	CSI_D9(MSB)	SD1_D1	SD1_DET
30	LCD_SD_I	LCD_SD_DIO	LCD_DRDY0	HDD_CS1	HDD_D6	FEC_MDIO	GPIO	GPIO	SD1_D2	SD1_WP
31	LCD_HSYNC	LCD_LSCLK_PLCK_FPSHIFT	GND	HDD_RESET_B	HDD_D7	FEC_MDC	GPIO	GND	SD1_D3	SD1_CLK
32	LCD_VSYNC	LCD_RD	LCD_SER_RS_DEN	ATA_ENABLE_B	HDD_D8	FEC_CRS	GPIO	GPIO	VDD_SD2_IO	VDD_SD1_IO
33	LCD_LCS1_RST	LCD_WR	LCD_SD_CLK	ATA_DIR	GND	FEC_INT_B	GPIO	GPIO	SD2_D0	SD2_CMD
34	LCD_G-1	LCD_G-2	LCD_LCS0	RFU_LCD2	HDD_D9	FEC_TX_CLK	GPIO	GPIO	SD2_D1	SD2_DET
35	LCD_R-1	LCD_R-2	LCD_VSYNC0	RFU_LCD2	HDD_D10	FEC_RXD0	OSC_CLKO	GND	SD2_D2	SD2_WP
36	LCD_B-1	LCD_B-2	LCD_PAR_RS	RFU_LCD2	HDD_D11	FEC_RX_DV	D14	D15	SD2_D3	SD2_CLK
37	LCD_B0_D0	LCD_CONTRAST	GND	RFU_LCD2	GND	FEC_RESET_B	D12	D13	VDD_EIM_ADDR	GND
38	LCD_B1_D1	LCD_CLS	RFU_LCD2	RFU_LCD2	HDD_D12	FEC_RX_CLK	D10	D11	A24	A25
39	LCD_B2_D2	LCD_SPL_SPR	RFU_LCD2	RFU_LCD2	HDD_D13	FEC_COL	D8	D9	A22	A23
40	GND	LCD_REV	RFU_LCD2	RFU_LCD2	HDD_D14	FEC_TX_ER	VDD_EIM_DATA	GND	A20	A21
41	LCD__R5_D17	GND	RFU_LCD2	RFU_LCD2	GND	FEC_ENABLE	D6	D7	A18	A19
42	LCD_R3_D15	LCD_R4_D16	RFU_LCD2	RFU_LCD2	HDD_D15	FEC_TX_EN	D4	D5	A16	A17
43	LCD__R2_D14	RFU_LCD2/GND	RFU_LCD2	RFU_LCD2	VDD_HDD_IO	VDD_FEC_IO	D2	D3	A14	A15
44	LCD_R0_D12	LCD_R1_D13	GND	RFU_LCD2	RFU_LCD2	RFU_LCD2	D0	D1	A12	A13
45	LCD__G5_D11	RFU_LCD2/GND	RFU_LCD2	RFU_LCD2	GND	RFU_LCD2	ECB_WAIT	BCLK	A10	A11
46	LCD_G3_D9	LCD__G4_D10	GND	RFU_LCD2	RFU_LCD2	EB0	EB1	GND	A8	A9
47	LCD_G2_D8	RFU_LCD2/GND	RFU_LCD2	RFU_LCD2	GND	1_WIRE_DATA	OE_B	RW_B	A6	A7
48	LCD_G0_D6	LCD_G1_D7	GND	RFU_LCD2	RFU_LCD2	LBA	CS4_B	CS5_B	A4	A5
49	LCD__B5_D5	RFU_LCD2/GND	RFU_LCD2	GND	GND	USB_OTG_UID	CS2_B	CS3_B	A2	A3
50	LCD_B3_D3	LCD_B4_D4	GND	USB_OTG_D_MINUS	USB_OTG_D_PLUS	GND	CS0_B	CS1_B	A0	A1

Table 4.2 500 Pin Connector Signal Descriptions

Signal	Pin	Description
GND	A1, A4, A7, A15, A40, B3, B6, B9, B20, B41, C1, C4, C8, C13, C19, C23, C27, C31, C37, C44, C46, C48, C50, D3, D6, D9, D49, E8, E13, E21, E25, E29, E33, E37, E41, E45, E47, E49, F2, F14, F50, G6, H3, H6, H11, H15, H19, H23, H27, H31, H35, H40, H46, J3, J21, J25, K3, K14, K37	Signal Ground
LI_BATTERY	A2, A3	Li_battery interface
1V8	A5, A6	From LDO U21, for peripheral devices use
LCD_BKLT_18MA_RETURN	A8	LCD backlight power return
LCD_BKLT_18MA_BOOST	A9	LCD backlight power
BKLT_5V_60MA_A	A10	5V, 60mA backlight drive Anode
BKLT_5V_60MA_K	A11	5V, 60mA backlight drive Negative
DEBUG_INT_B	A12	Debug board interrup
MASTER_RESET_B	A13	i.MX25 reset signal, low active, from reset button on Personality board or Debug board
OSC_32KHz	A14	32.768KHz frequency output
UART2_RX	A16	i.MX25 UART2 serial data receive
UART2_TX	A17	i.MX25 UART2 serial data transmit
UART2_CTS	A18	i.MX25 UART2 clear to send
UART2_RTS	A19	i.MX25 UART2 request to send
UART3_RX	A20	i.MX25 UART3 serial data receive
UART3_TX	A21	i.MX25 UART3 serial data transmit
UART3_CTS	A22	i.MX25 UART3 clear to send
UART3_RTS	A23	i.MX25 UART3 request to send
UART1_RX	A24	i.MX25 UART1 serial data receive
UART1_TX	A25	i.MX25 UART1 serial data transmit
UART1_CTS	A26	i.MX25 UART1 clear to send
UART1_RTS	A27	i.MX25 UART1 request to send
RFU	A28, B12, B13, B16, B17, B18, B19, B21, B22, D15, E2, A14, F2, F12, F13, F21, G7, G8, G9, G10, G11, H7, H8, H9, J13, K22,	Reserved for future use
VDD_LCDIO	A29	LCD IO power supply
LCD_SD_I	A30	NC for i.MX25
LCD_HSYNC	A31	LCD Line sync
LCD_VSYNC	A32	LCD Vsync
LCD_LCS1_RST	A33	LCD module reset
LCD_G-1	A34	LCD data23
LCD_R-1	A35	LCD data21
LCD_B-1	A36	LCD data19
LCD_B0_D0	A37	LCD data0

Signal	Pin	Description
LCD_B1_D1	A38	LCD data1
LCD_B2_D2	A39	LCD data2
LCD__R5_D17	A41	LCD data17
LCD_R3_D15	A42	LCD data15
LCD__R2_D14	A43	LCD data14
LCD_R0_D12	A44	LCD data12
LCD__G5_D11	A45	LCD data11
LCD_G3_D9	A46	LCD data9
LCD_G2_D8	A47	LCD data8
LCD_G0_D6	A48	LCD data6
LCD__B5_D5	A49	LCD data5
LCD_B3_D3	A50	LCD data3
USB_5V_VBUS	B1, B2	USB OTG 5V VBUS
3V3	B4, B5	3.3V power supply
WALL_5V_IN	B7, B8	DC 5.0V power supply
2V8	B10, B11	2.8V power supply
POR_B	B12	POR_B
GPIO_CLAMSHELL	B13	GPIO
BATTERY_TEMP	B14	NC for i.MX25
DEBUG	B23	NC for i.MX25
PERSONALITY1	B24	Personality board version code
PERSONALITY2	B25	Personality board version code
PERSONALITY3	B26	Personality board version code
CPU1	B27	CPU board version code
CPU2	B28	CPU board version code
CPU3	B29	CPU board version code
LCD_SD_DIO	B30	NC for i.MX25
LCD_LSCLK_PLCK_FPS HIFT	B31	LCD pixel clk
LCD_RD	B32	LCD Asynch. Port read
LCD_WR	B33	LCD Asynch. Port write
LCD_G-2	B34	LCD data22
LCD_R-2	B35	LCD data20
LCD_B-2	B36	LCD data18
LCD_CONTRAST	B37	LCD backlight contrast adjust
LCD_CLS	B38	NC for i.MX25
LCD_SPL_SPR	B39	NC for i.MX25
LCD_REV	B40	NC for i.MX25
RFU_LCD2	B43, B45, B47, B49, C38, C39, C40, C41, C42, C43, C45, C47, C49, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, E44, E46, E48, F44, F45	Reserved for LCD future use

Signal	Pin	Description
LCD_R4_D16	B42	LCD data16
LCD_R1_D13	B44	LCD data13
LCD__G4_D10	B46	LCD data10
LCD_G1_D7	B48	LCD data7
LCD_B4_D4	B50	LCD data4
VMAIN	C2, C3	Application power supply, from DC power or battery
LINEAR_A	C5	Linear regulator A(1.3V)
LINEAR_B	C6	Linear regulator B(1.5V)
LINEAR_C	C7	Linear regulator C(1.5V)
LINEAR_D	C9	Linear regulator D(3V)
LINEAR_E	C10	NC for i.MX25
LINEAR_F	C11	Linear regulator F(5V)
SLEEP_VSTBY	C12	Power management state retention
ON_OFF	C14	System On/Off signal
LI_CELL	C15	Coincell battery
VDD_I2C_IO	C16	I2C power supply
I2C1_DATA	C17	I2C1 data
I2C1_CLOCK	C18	I2C1 clock
I2C2_CLOCK	C20	I2C2 clock
I2C2_DATA	C21	I2C1 data
CSPI1_MOSI	C22	CSPI1 Master out/ Slave in
CSPI1_MISO	C24	CSPI1 Master in/ Slave out
CSPI1_SS0	C25	CSPI1 Slave select 0
CSPI1_SS1	C26	CSPI1 Slave select 1
CSPI1_SCLK	C28	CSPI1 serial clock
CSPI1_RDY	C29	CSPI1 signal ready
LCD_DRDY0	C30	LCD DRDY/VLD
LCD_SER_RS_DEN	C32	NC for i.MX25
LCD_SD_CLK	C33	NC for i.MX25
LCD_LCS0	C34	Asynch. Port chip select
LCD_VSYNC0	C35	NC for i.MX25
LCD_PAR_RS	C36	Asynch. Parallel Port data/comm
CURRENT_MEAS_1	D1	Current Measure 1 (DDR in CPU board)
CURRENT_MEAS_2	D2	Current Measure 2 (Core in CPU board)
CURRENT_MEAS_3	D4	Current Measure 3 (VMAIN in CPU board)
CURRENT_MEAS_4	D5	Current Measure 4 (3V3 in CPU board)
CURRENT_MEAS_5	D7	Current Measure 5
CURRENT_MEAS_6	D8	NC for i.MX25
CURRENT_MEAS_7	D10	NC for i.MX25
CURRENT_MEAS_8	D11	NC for i.MX25

Signal	Pin	Description
CURRENT_MEAS_9	D12	NC for i.MX25
CURRENT_MEAS_10	D13	NC for i.MX25
LCD_EN	D14	LCD ENABLE
WIFI_PWEN	D16	WIFI power enable
ESAI_GPIO	D17	ESAI GPIO
ESAI_RST_B	D18	ESAI reset
HDD_PWR_EN	D19	HDD power enable
HDD_DMARQ	D20	NC for i.MX25
HDD_DIOW	D21	NC for i.MX25
HDD_DIOR	D22	NC for i.MX25
HDD_IORDY	D23	NC for i.MX25
HDD_DMACK	D24	NC for i.MX25
HDD_INTRQ	D25	NC for i.MX25
HDD_DA1	D26	NC for i.MX25
HDD_DA0	D27	NC for i.MX25
HDD_CS0	D28	NC for i.MX25
HDD_DA2	D29	NC for i.MX25
HDD_CS1	D30	NC for i.MX25
HDD_RESET_B	D31	NC for i.MX25
ATA_ENABLE_B	D32	NC for i.MX25
ATA_DIR	D33	NC for i.MX25
USB_FS_D_MINUS	D48	USB FS data minus
USB_OTG_D_MINUS	D50	USB OTG data minus
AUDIO_LIN_R	E1	Audio Line in right
MIC_IN_P	E3	Microphone amplifier input
MIC_BIAS	E4	Microphone supply output with intergrated bias resistor and detect
HEADPHONE_DETECT	E5	Headphone insert detect
ADC_1	E6	ADC input 1(To distinguish the headphone or TV out insert)
ADC_2	E7	ADC input 2 (SD card write protect detect)
ADC_3	E9	ADC input 3
ADC_4	E10	ADC input 4
ADC_5	E11	NC for i.MX25
ADC_6	E12	NC for i.MX25
CAN_PWDN	E14	CAN power down
ESAI_TX0	E15	ESAI_TX0
ESAI_TX2_RX3	E16	ESAI_TX2_RX3
ESAI_TX4_RX1	E17	ESAI_TX4_RX1
ESAI_FSR	E18	ESAI_FSR
ESAI_SCKR	E19	ESAI_SCKR
ESAI-HCKR	E20	ESAI-HCKR
HDD_D0	E22	NC for i.MX25

Signal	Pin	Description
HDD_D1	E23	NC for i.MX25
HDD_D2	E24	NC for i.MX25
HDD_D3	E26	NC for i.MX25
HDD_D4	E27	NC for i.MX25
HDD_D5	E28	NC for i.MX25
HDD_D6	E30	NC for i.MX25
HDD_D7	E31	NC for i.MX25
HDD_D8	E32	NC for i.MX25
HDD_D9	E34	NC for i.MX25
HDD_D10	E35	NC for i.MX25
HDD_D11	E36	NC for i.MX25
HDD_D12	E38	NC for i.MX25
HDD_D13	E39	NC for i.MX25
HDD_D14	E40	NC for i.MX25
HDD_D15	E42	NC for i.MX25
VDD_HDD_IO	E43	HDD IO Power supply
USB_FS_D_PLUS	E48	USB FS data plus
USB_OTG_D_PLUS	E50	USB OTG data plus
AUDIO_LIN_L	F1	Audio Line in left
BOOTSTRAP_0	F4	Boot Strap 0
BOOTSTRAP_1	F5	Boot Strap 1
BOOTSTRAP_2	F6	NC for i.MX25
BOOTSTRAP_3	F7	NC for i.MX25
BOOTSTRAP_4	F8	NC for i.MX25
BOOTSTRAP_5	F9	NC for i.MX25
VDD_BOOTSTRAP	F10	Boot Strap Power supply
SIM2_PD	F11	SIM2_PD
SIM2_TX	F12	SIM2_TX
ESAI_TX1	F15	ESAI_TX1
ESAI_TX3_RX2	F16	ESAI_TX3_RX2
ESAI_TX5_RX0	F17	ESAI_TX5_RX0
ESAI_FST	F18	ESAI_FST
ESAI_SCKT	F19	ESAI_SCKT
ESAI_HCKT	F20	ESAI_HCKT
FEC_TXD2	F22	NC for i.MX25
FEC_TXD3	F23	NC for i.MX25
FEC_RX_ER	F24	FEC interface
FEC_TXD0	F25	FEC interface
FEC_RXD1	F26	FEC interface
FEC_RXD2	F27	NC for i.MX25
FEC_RXD3	F28	NC for i.MX25

Signal	Pin	Description
FEC_TXD1	F29	FEC interface
FEC_MDIO	F30	FEC interface
FEC_MDC	F31	FEC interface
FEC_CRS	F32	NC for i.MX25
FEC_INT_B	F33	NC for i.MX25
FEC_TX_CLK	F34	FEC interface
FEC_RXD0	F35	FEC interface
FEC_RX_DV	F36	FEC interface
FEC_RESET_B	F37	FEC interface
FEC_RX_CLK	F38	NC for i.MX25
FEC_COL	F39	NC for i.MX25
FEC_TX_ER	F40	NC for i.MX25
FEC_ENABLE	F41	FEC interface
FEC_TX_EN	F42	FEC interface
VDD_FEC_IO	F43	FEC interface
EB0	F46	NC for i.MX25
1_WIRE_DATA	F47	1 Wire data
LBA	F48	NC for i.MX25
USB_OTG_UID	F49	USB OTG ID signal
AUDIO_LOUT_R	G1	Audio Line out right
HEADPHONE_RIGHT	G2	Headphone right
HEADPHONE_RETURN	G3	Headphone return(Connect with GND)
SPEAKER_RIGHT_P	G4	Handset loudspeaker and alert amplifier positive terminal
SPEAKER_RIGHT_N	G5	Handset loudspeaker and alert amplifier minus terminal
SIM2_CLK	G7	SIM2_CLK
SSI_RESET	G8	SSI_RESET
SIM2_RST	G9	SIM2_RST
SIM2_VEN	G10	SIM2_VEN
SIM2_RX	G11	SIM2_RX
CSI_RESET_B	G12	Camera sensor reset signal
CSI_PWDN	G13	Camera sensor power down
KP_ROW_7	G14	NC for i.MX25
KP_ROW_6	G15	NC for i.MX25
KP_ROW_5	G16	NC for i.MX25
KP_ROW_4	G17	NC for i.MX25
KP_ROW_3	G18	Keypad row 3
KP_ROW_2	G19	Keypad row 2
KP_ROW_1	G20	Keypad row 1
KP_ROW_0	G21	Keypad row 0
KP_COL_7	G22	NC for i.MX25
KP_COL_6	G23	NC for i.MX25

Signal	Pin	Description
KP_COL_5	G24	NC for i.MX25
KP_COL_4	G25	NC for i.MX25
KP_COL_3	G26	Keypad column 3
KP_COL_2	G27	Keypad column 2
KP_COL_1	G28	Keypad column 1
KP_COL_0	G29	Keypad column 0
GPIO	G30	GPS Interrupt
GPIO	G31	USB,BT cs signal
GPIO	G32	FEC power down
GPIO	G33	GPS reset signal
GPIO	G34	GPS clk enable
OSC_CLKO	G35	i.MX25 clock out
D14	G36	NC for i.MX25
D12	G37	NC for i.MX25
D10	G38	NC for i.MX25
D8	G39	NC for i.MX25
VDD_EIM_DATA	G40	EIM data power supply
D6	G41	NC for i.MX25
D4	G42	NC for i.MX25
D2	G43	NC for i.MX25
D0	G44	NC for i.MX25
ECB_WAIT	G45	NC for i.MX25
EB1	G46	NC for i.MX25
OE_B	G47	NC for i.MX25
CS4_B	G48	NC for i.MX25
CS2_B	G49	NC for i.MX25
CS0_B	G50	NC for i.MX25
AUDIO_LOUT_L	H1	Audio Line out Left
HEADPHONE_LEFT	H2	Headphone Left
SPEAKER_LEFT_P	H4	Handset earpiece speaker amplifier output positive terminal
SPEAKER_LEFT_N	H5	Handset earpiece speaker amplifier output minus terminal
VDD_CSI_IO	H10	Camera sensor power supply
CSI_HSYNC	H12	Camera sensor horizontal Sync
CSI_VSYNC	H13	Camera sensor vertical Sync
CSI_MCLK	H14	Camera sensor master clock
CSI_PIXCLK	H16	Camera sensor data latch clock
CSI_D0	H17	Camera sensor data 0
CSI_D1	H18	Camera sensor data 1
CSI_D2	H20	Camera sensor data 2
CSI_D3	H21	Camera sensor data 3

Signal	Pin	Description
CSI_D4	H22	Camera sensor data 4
CSI_D5	H24	Camera sensor data 5
CSI_D6	H25	Camera sensor data 6
CSI_D7	H26	Camera sensor data 7
CSI_D8	H28	Camera sensor data 8
CSI_D9(MSB)	H29	Camera sensor data 9
GPIO	H30	GPS module power enable
GPIO	H32	GPS reset, active low
GPIO	H33	WiFi reset, active low
GPIO	H34	Bluetooth reset, active low
D15	H36	NC for i.MX25
D13	H37	NC for i.MX25
D11	H38	NC for i.MX25
D9	H39	NC for i.MX25
D7	H41	NC for i.MX25
D5	H42	NC for i.MX25
D3	H43	NC for i.MX25
D1	H44	NC for i.MX25
BCLK	H45	NC for i.MX25
RW_B	H47	NC for i.MX25
CS5_B	H48	NC for i.MX25
CS3_B	H49	NC for i.MX25
CS1_B	H50	NC for i.MX25
TOUCH_X0	J1	Touch screen X0
TOUCH_X1	J2	Touch screen X1
TV_DAC_C_RETURN	J4	TV DAC return (reserved for future use)
TV_DAC_B_RETURN	J5	TV DAC return (reserved for future use)
TV_DAC_A_RETURN	J6	TV DAC return (reserved for future use)
SIM_CLK	J7	Sim card interface
SIM_RST	J8	Sim card interface
SIM_VEN	J9	Sim card interface
VDD_SIM_IO	J10	Sim card power supply
CHRG_LED	J11	NC for i.MX25
VDD_JTAG	J12	JTAG power supply
CPLD_PGM_TDI	J14	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TDO	J15	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TMS	J16	CPLD JTAG interface (Reserved for future use)
CPLD_PGM_TCK	J17	CPLD JTAG interface (Reserved for future use)
SSI1_STXD	J18	SSI1 interface TxD signal
SSI1_SRXD	J19	SSI1 interface RxD Signal

Signal	Pin	Description
SSI1_SFS	J20	SSI1 interface Frame Sync
SSI1_SCK	J22	SSI1 interface Serial Clock
SSI2_STXD	J23	SSI2 interface TxD signal
SSI2_SRXD	J24	SSI2 interface RxD Signal
SSI2_SFS	J26	SSI2 interface Frame Sync
SSI2_SCK	J27	SSI2 interface Serial Clock
SD1_D0	J28	SD card 1 data 0
SD1_D1	J29	SD card 1 data 1
SD1_D2	J30	SD card 1 data 2
SD1_D3	J31	SD card 1 data 3
VDD_SD2_IO	J32	SD card 2 power supply
SD2_D0	J33	SD card 2 data 0
SD2_D1	J34	SD card 2 data 1
SD2_D2	J35	SD card 2 data 2
SD2_D3	J36	SD card 2 data 3
VDD_EIM_ADDR	J37	EIM address power supply
A24	J38	NC for i.MX25
A22	J39	NC for i.MX25
A20	J40	NC for i.MX25
A18	J41	NC for i.MX25
A16	J42	NC for i.MX25
A14	J43	NC for i.MX25
A12	J44	NC for i.MX25
A10	J45	NC for i.MX25
A8	J46	NC for i.MX25
A6	J47	NC for i.MX25
A4	J48	NC for i.MX25
A2	J49	NC for i.MX25
A0	J50	NC for i.MX25
TOUCH_Y0	K1	Touch screen Y0
TOUCH_Y1	K2	Touch screen Y1
TV_DAC_C	K4	TV DAC (reserved for future use)
TV_DAC_B	K5	TV DAC (reserved for future use)
TV_DAC_A	K6	TV DAC (reserved for future use)
SIM_RX	K7	Sim card interface (reserved for future use)
SIM_PD	K8	Sim card interface (reserved for future use)
SIM_TX	K9	Sim card interface (reserved for future use)
JTAG_TRST_B	K10	JTAG TAP Reset
JTAG_TDI	K11	JTAG TAP Data In
JTAG_TMS	K12	JTAG TAP Mode select
JTAG_TCK	K13	JTAG TAP clock

Signal	Pin	Description
JTAG_RTCK	K15	JTAG ARM Debug Test Clock
JTAG_DE_B	K16	JTAG Debug Enable
JTAG_TDO	K17	JTAG TAP data out
JTAG_RESET_B	K18	JTAG reset signal
MLB_SIG	K19	Reserved for Future use
MLB_DAT	K20	Reserved for Future use
MLB_CLK	K21	Reserved for Future use
CAN TX1 RFU	K23	CAN TX
CAN RX1 RFU	K24	CAN RX
CAN TX2 RFU	K25	Reserved for Future use
CAN RX2 RFU	K26	Reserved for Future use
VDD_MLB	K27	Reserved for Future use
SD1_CMD	K28	SD card 1 Command signal
SD1_DET	K29	SD card 1 Detect signal
SD1_WP	K30	SD card 1 write protect
SD1_CLK	K31	SD card 1 clock signal
VDD_SD1_IO	K32	SD card 1 power supply
SD2_CMD	K33	SD card 2 Command signal
SD2_DET	K34	SD card 2 Detect signal
SD2_WP	K35	SD card 2 write protect
SD2_CLK	K36	SD card 2 clock signal
A25	K38	NC for i.MX25
A23	K39	NC for i.MX25
A21	K40	NC for i.MX25
A19	K41	NC for i.MX25
A17	K42	NC for i.MX25
A15	K43	NC for i.MX25
A13	K44	NC for i.MX25
A11	K45	NC for i.MX25
A9	K46	NC for i.MX25
A7	K47	NC for i.MX25
A5	K48	NC for i.MX25
A3	K49	NC for i.MX25
A1	K50	NC for i.MX25

4.2 Audio Jack

The J19 jack is the audio output for the i.MX25 PDK. HEADPHONE_DETECT line is used by the software to detect headphone insertion.

Figure 4-1 illustrates the J19 Audio jack pin signals.

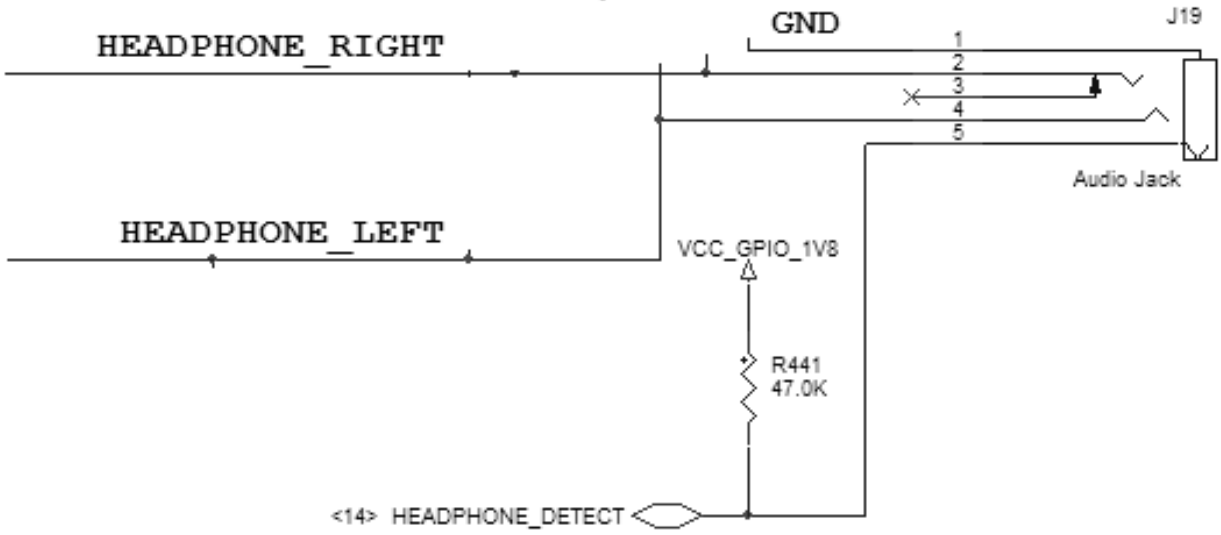

Figure4-1 Audio Jack Pin-Signals

4.3 LCD Connector

On the Personality board, J14 is the connector to the CPT 5.7 ‘’ VGA Display LAA057VA01CT. Table 4.3 provides the pin information of the connector.

Table 4.3 LCD Connector Pin-Out

Pin Number	Symbol	Description
1	U/D	Up or Down Display Control
2	NC	Customer non-connect: initial pull high = DE mod
3	Hsync	Horizontal SYNC
4	V_{LED}	Power Supply for LED
5	V_{LED}	Power Supply for LED
6	V_{LED}	Power Supply for LED
7	V_{cc}	Power Supply for LCD
8	V_{sync}	Vertical SYNC
9	DE	Data Enable
10	X2	TSP control (Left)
11	Y1	TSP control (Up)
12	ADJ	Adjust for LED brightness
13	B5	Blue Data 5 (MSB)
14	B4	Blue Data 4
15	B3	Blue Data 3
16	V_{SS}	Power Ground
17	B2	Blue Data 2
18	B1	Blue Data 1
19	B0	Blue Data 0 (LSB)
20	V_{SS}	Power Ground
21	G5	Green Data 5 (MSB)
22	G4	Green Data 4
23	G3	Green Data 3
24	V_{SS}	Power Ground
25	G2	Green Data 2
26	G1	Green Data 1
27	G0	Green Data 0 (LSB)
28	V_{SS}	Power Ground

Pin Number	Symbol	Description
29	R5	Red Data 5 (MSB)
30	R4	Red Data 4
31	R3	Red Data 3
32	V_{SS}	Power Ground
33	R2	Red Data 2
34	R1	Red Data 1
35	R0	Red Data 0 (LSB)
36	X1	TSP control (Right)
37	Y2	TSP control (Down)
38	DCLK	Clock Signals
39	V_{SS}	Power Ground
40	L/R	Left/Right Display Control

4.4 Keypad

The Personality Board provides 16-push buttons Keypad for applications which requires it.

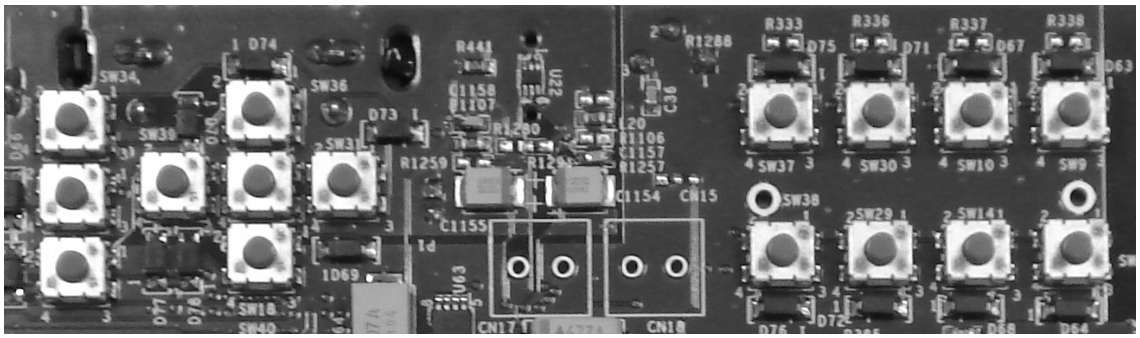

Figure 4-2 On Board Keypad