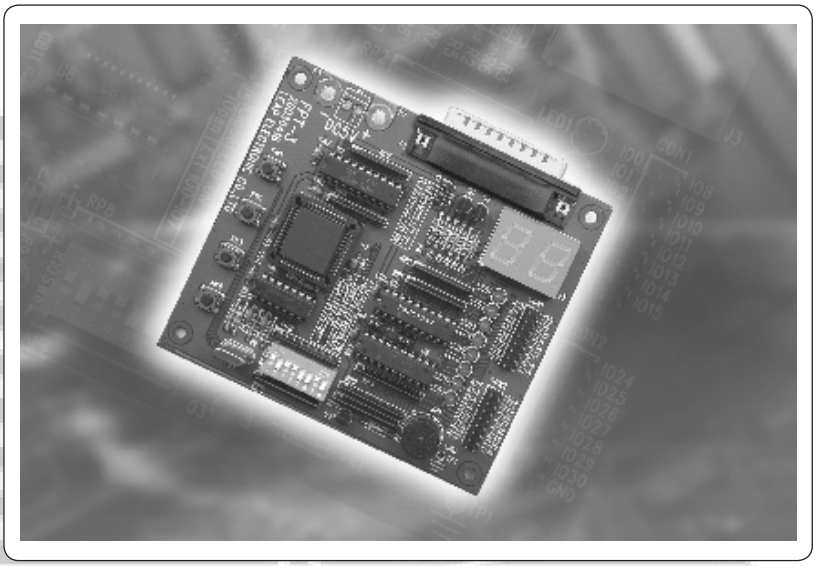
FPT-3 CPLD/FPGA SIMPLE LOGIC CIRCUIT DESIGN BOARD



Features

- Exploit CPLD/FPGA hardware/software development system to learn the newest design of logicalIC to instead of the complex hardware design of TTL/CMOS.
- Capable to use Circuit Graphic and VHDL to develop hardware circuit.
- Directly download the designed program from the development system to CPLD via printer port to operate independently.

Specifications

- Support Altera CPLD MAX7000S devices series

1. EPM7064/32SLC44-10(alternative)
2. PLD on EEPROM structure
3. 5V working voltage
4. Support 1250 logic gates and 64 LCs
5. 32 I/O availably

- System clock: 1.8432MHz
- ISP programming interface
- Dimension:100 x 115 x 21.8 mm
- Weight: 500 g
- Input: 5V DC

Input Unit

- 8 logic DIP switch
- 4 sets of negative pulse press button

Output Unit

- 8 LED (low voltage drove)
- Buzzer x 1
- 2 digits 7 segment display

(Common cathode: low voltage drove)

Experiment Content

- Basic logic
  1. Logic experiment (DIP SW + LED)
  2. Relationship experiment (DIP SW + LED)
  3. Complier/Decoder
- Arithmetic logic circuit
  1. Adder
  2. Subtracter
  3. Multiplexer
- Frequency divide and count
  1. 7 segment display
     (Binary to Decimalism)
  2. 8 LED
     (Binary to Decimalism)
  3. Frequency divide test (LED)
  4. All I/O test
  5. Upward counter
  6. Traffic light display
  7. Simple electric piano

Optional Accessories

- ALTERA EPM7064SLC44-10
- ALTERA EPM7032SLC44-10