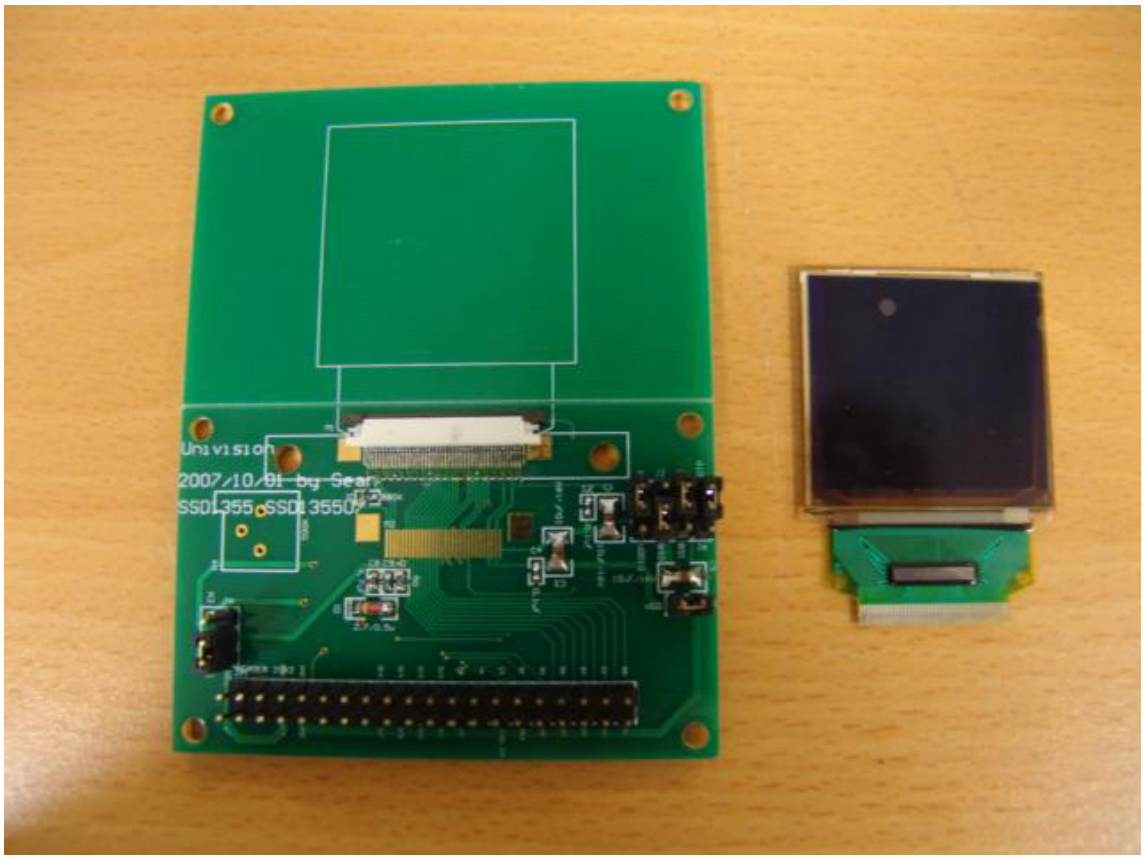
OLED DISPLAY MODULE

Application Notes

PRODUCT NUMBER	DD-128128FC-5B with EVK board



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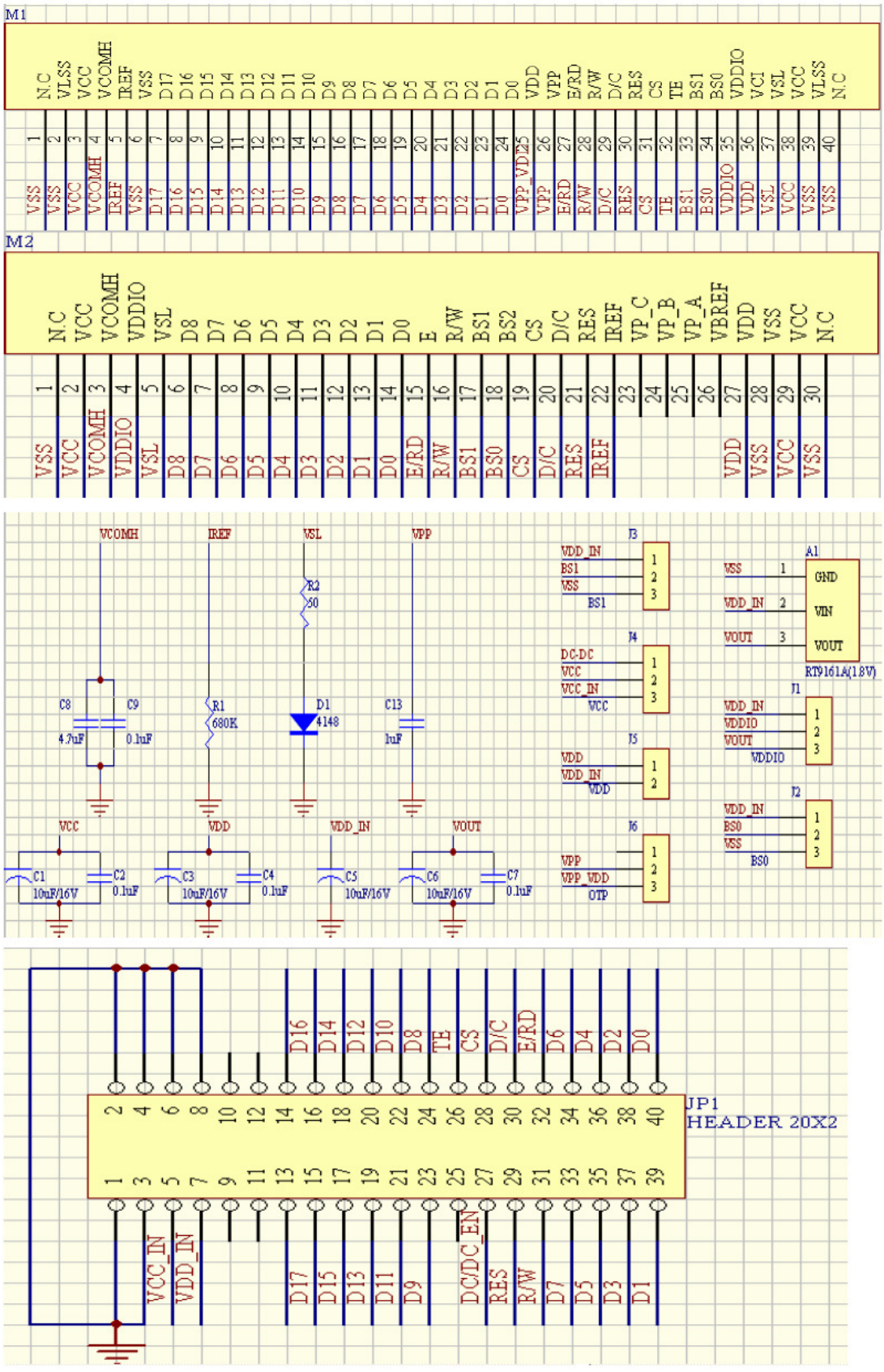
REVISION RECORD

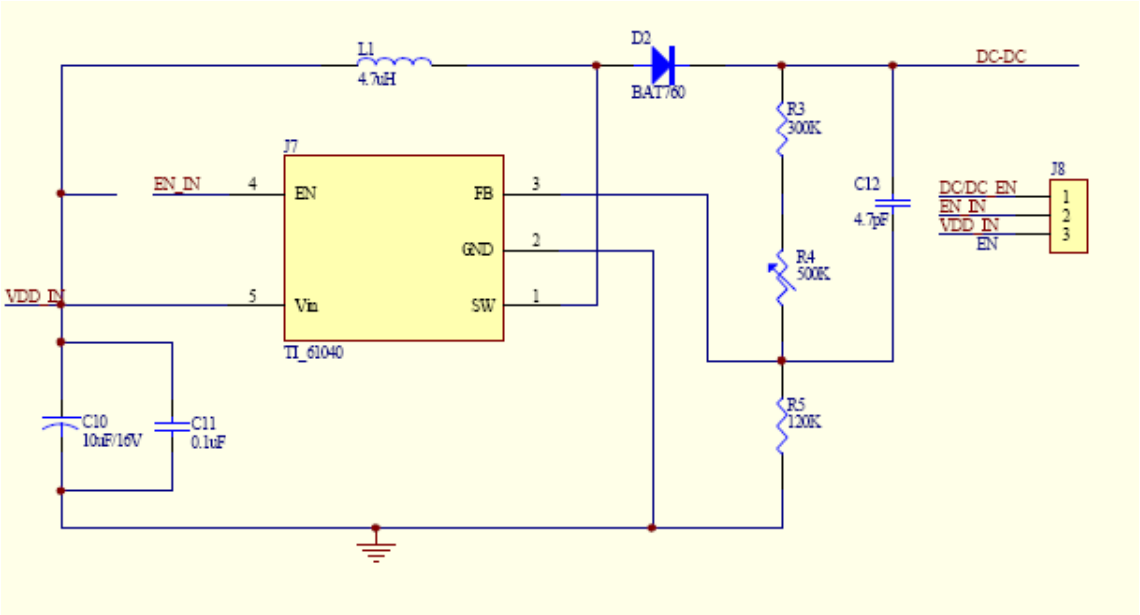
Rev.	Date	Page	Chapt.	Comment	ECR no.
A	27 June 08			First Issue	
B	06 May 09			Updated Schematic	

1 Schematic

1.1 EVK Schematic



1.2 DC-DC Schematic



2 Symbol Definition

D0-D17：These pins are 18-bit bi-directional data bus to be connected to the MCU's data bus.

BS0, BS1, BS2, BS3：These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table. User can fix these pins by jumper (J2, J3). Unlike BS0,BS1 which are controlled by hardware, BS2,BS3 is controlled by software command 0x36.

BS[3.0]	Interface
0000	4 line SPI
0001	3 line SPI
0011	8-bit 6800 parallel
0010	8-bit 8080 parallel
0111	16-bit 6800 parallel
0110	16-bit 8080 parallel
1111	18-bit 6800 parallel
1110	18-bit 8080 parallel

Table 1 – MCU Interface Selection Setting

E/RD#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.
When connecting to an 8080-microprocessor, this pin receives the Read (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD) must be connected to VSS.

R/W#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.
When 8080 interface mode is selected, this pin is the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W must be connected to VSS.

D/C#：This pin is Data/Command control pin. When the pin is pulled high, the data at D0-D8 is treated as display data. When the pin is pulled low, the data at D0-D8 is transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams at following pages and datasheet.

RES#：This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS#：This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

VCC：This is the most positive voltage supply pin of the chip.

VDD：Power supply pin for logic operation of the driver.

GND：Power supply ground.

VDDIO：This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source (1.8V). All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS01, 2,3, M/S, CLS, D0-D17, control signals) pull high, they should be connected to VDDIO. In the EVK PCB board which is use a jump (J1) connect to VDD (Default). Customer can put out the jump and input the 1.8V through this jump

VSL：This is segment voltage reference pin. For reduce power consumption, we suggest add a resistor and Zenor diode between this pin and GND.

VCOMH：This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When V**COMH** is generated internally, a capacitor should be connected between this pin and GND.

3 Timing characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 2 6800-Series MPU Parallel Interface Timing Characteristics

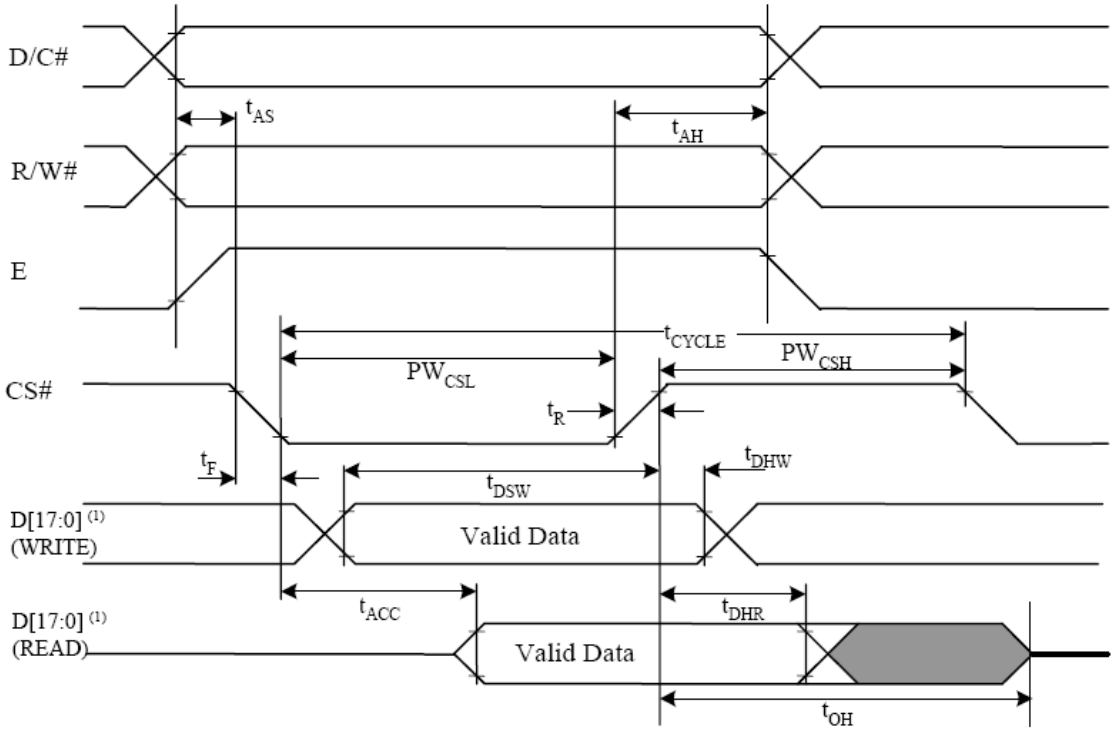


Figure 1 6800-series MPU parallel interface characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Table 3 8080-Series MPU Parallel Interface Timing Characteristics

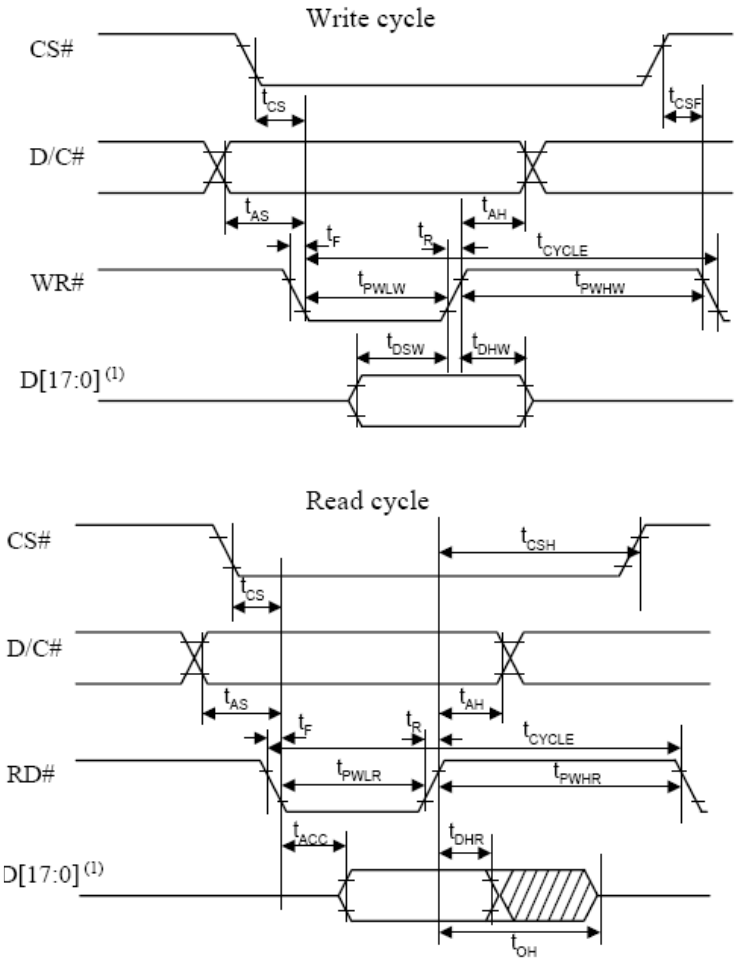


Figure 2 8080-series MPU parallel interface characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{C1} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 4: 4-bit SPI-Series Timing Characteristics

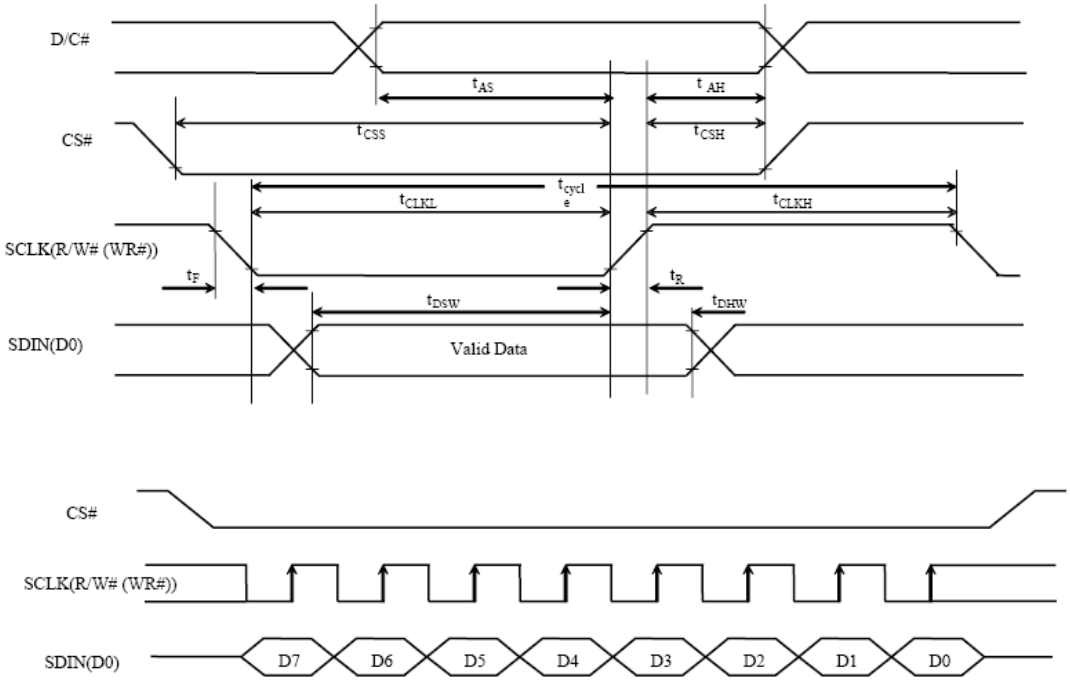


Figure 3: 4-bit SPI-Series characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 5: 3-bit SPI-Series Timing Characteristics

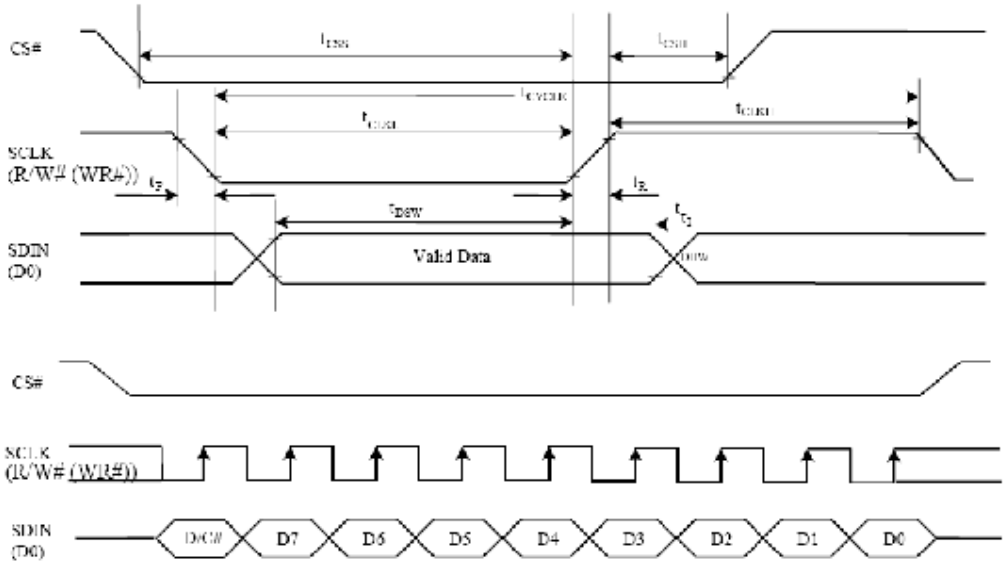


Figure 4: 3-bit SPI-Series characteristics

4 Connection Between OLED and EVK

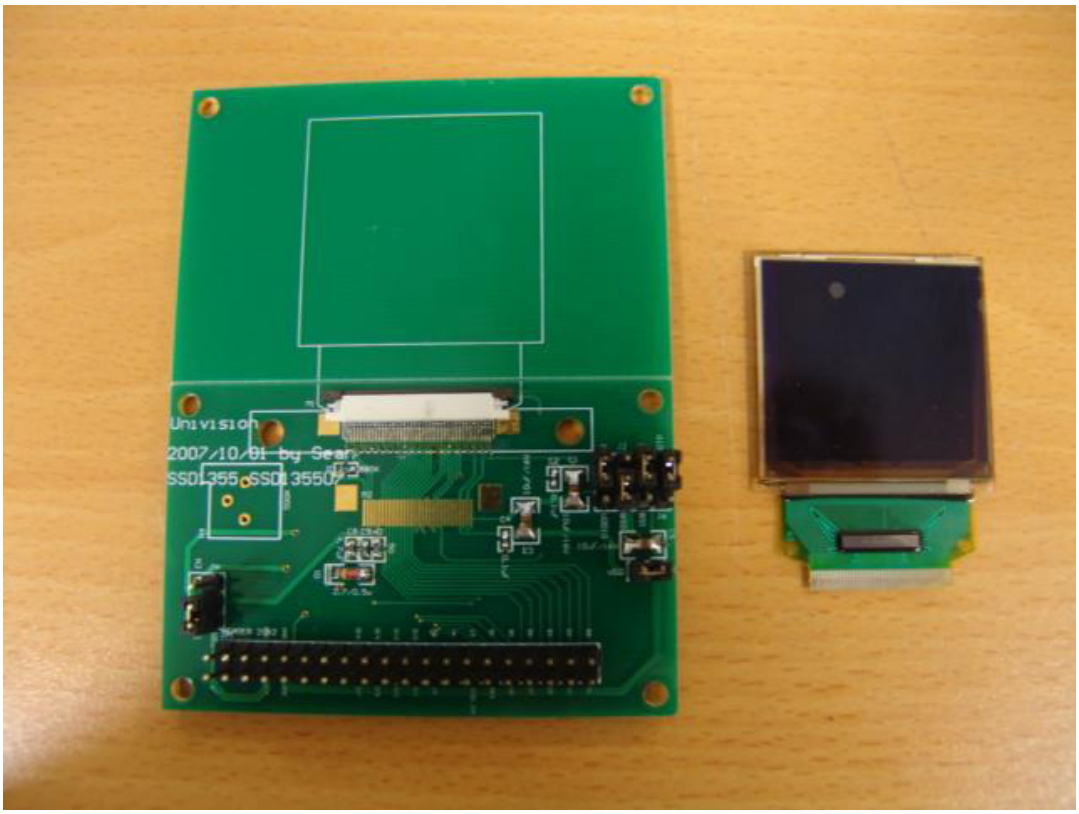


Figure 5 EVK PCB and DD-128128FC-5B Module

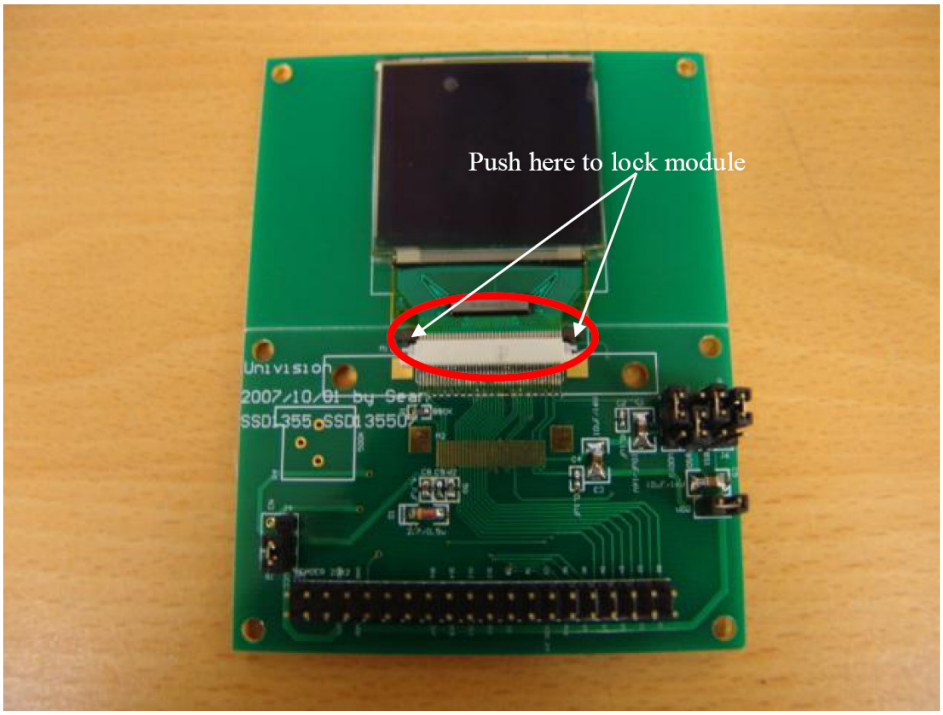


Figure 6 the DD-128128FC-5B and EVK assembled (Top view)

Because the package of DD-128128FC-5B is COF, the connect pads are on the top of the module, and the connector which on the EVK PCB board is double size connect type. So when assemble the module with EVK, the module must face up first and plug into the connector. When finished assembling the module and EVK, then push the locking pad to lock the module. See figure 6.
When finished assembling the module and EVK, the user can use leading wire to connect the EVK with customers system. Example shown in figure 7.

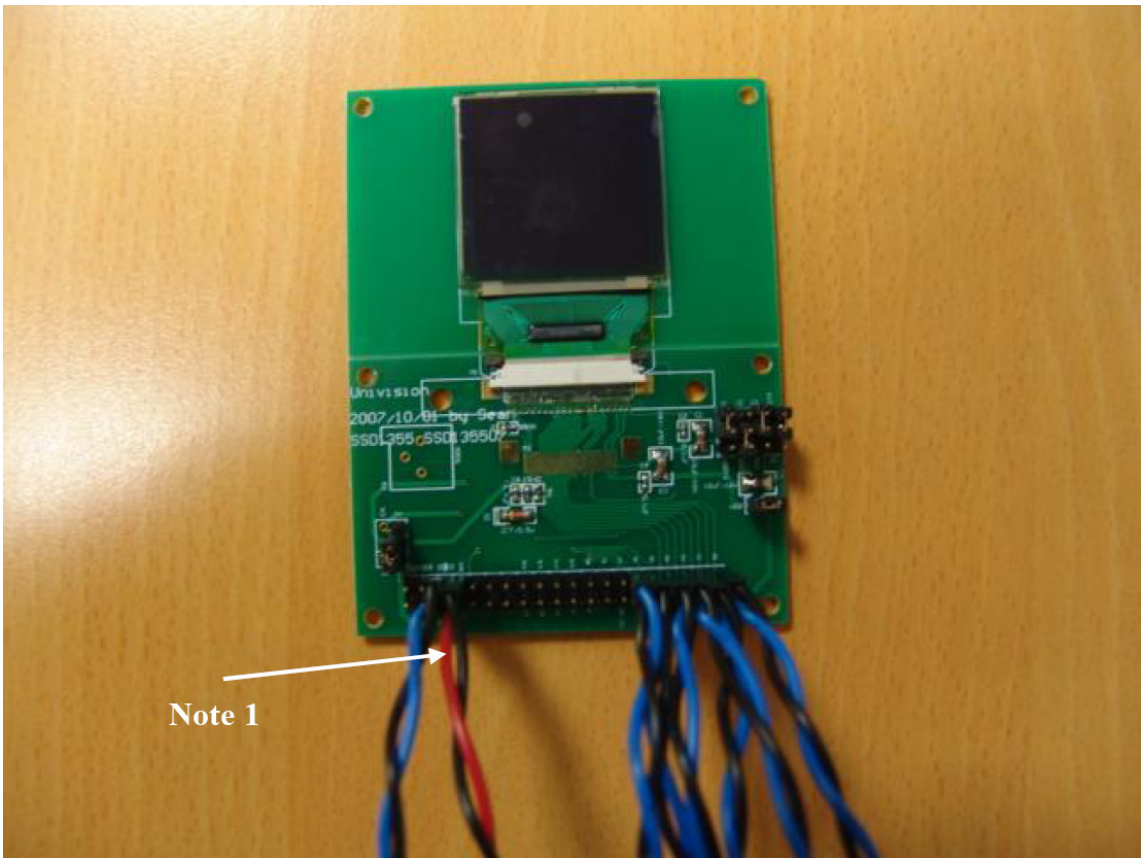


Figure 7 control MCU (not supplied) connected with EVK

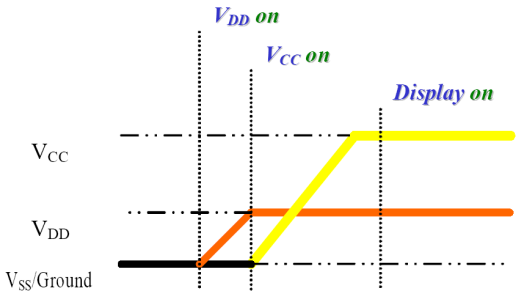
Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.

5 Power Down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that the panel has enough time to charge up or discharge before/after operation.

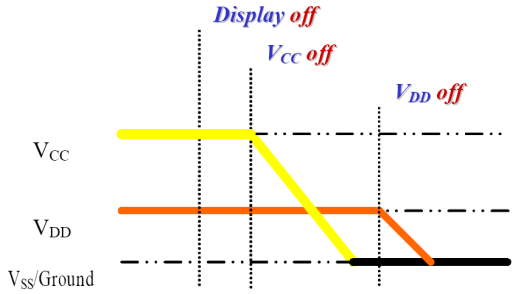
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
(when V_{DD} is stable)
7. Send Display on command

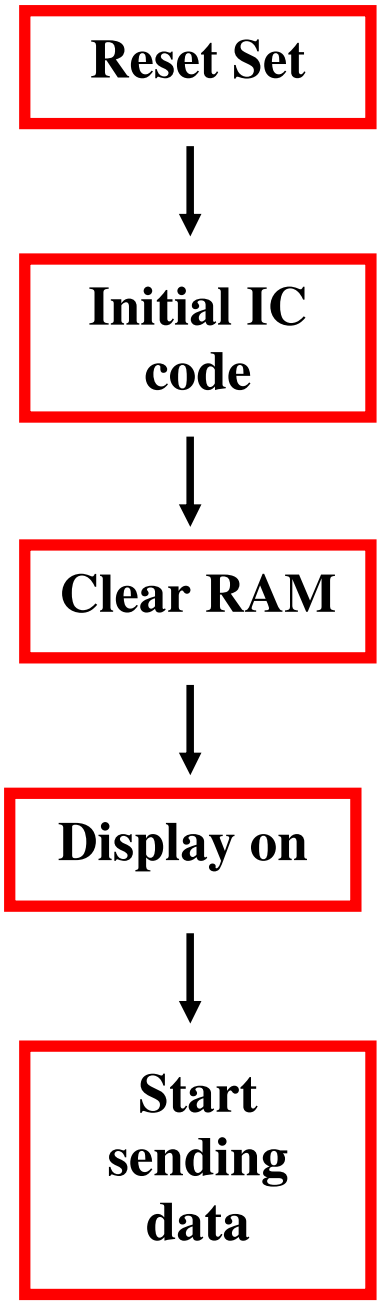


Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
(when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



6 How to use the DD-128128FC-5B



RES#=0; Delay 100ms; RES#=1

Suggest all registers set again

6.1 Recommended Initial code

```
write_c(0xfd); //Command Lock
write_d(0xb3);
write_c(0xd3); //Function Selection
write_d(0x01);
write_c(0xd6); //High Power protection
write_d(0x07);
write_c(0xcc); //Enable External VSL
write_d(0xb0);
write_d(0x16);
write_c(0x35); //Enable Tearing Effect
write_d(0x00);
write_c(0xca); //Set MUX Ratio
write_d(0x7f);
write_c(0xba); //Set Contrast For Color A
write_d(0x1c);
write_c(0xbb); //Set Contrast For ColorB
write_d(0x15);
write_c(0xbc); //Set Contrast For ColorC
write_d(0x23);
write_c(0xcf); //Set Second Precharge Speed
write_d(0x03);
write_c(0xcd); //Set Phase Length
write_d(0x32);
write_c(0xd2); //Set Display Clock Divider/Oscillator Frequency
write_d(0x10);
write_c(0xce); //Set Second Precharge Period
write_d(0x0b);
write_c(0xbd); //Set First Precharge Voltage
write_d(0x09);
write_c(0xe3); //Low Gray Scale Enhancement
write_d(0x02);
write_c(0x51); //Write Lumimance
write_d(0xf0);
write_c(0xd3); //Set VcomH
write_d(0x04);
write_c(0xd1); //contrast compensation
write_d(0x00);
write_d(0x00);
write_c(0xd0); //First Per-charge Compensation
write_d(0x04);
write_d(0x3f);
write_c(0x36); //Memory Access Control
write_d(0x00);
write_d(0x01);
write_c(0x11); //Sleep out
write_c(0x3a); //Interface Pixel Format
write_d(0x06);
write_c(0x2a); //Set Column Address
write_d(0x00);
write_d(0x7f);
write_c(0x2b); //Set Row Address
write_d(0x00);
write_d(0x7f);
write_c(0xbe); //Gamma Lock UpTable
write_d(1); //1
write_d(6); //3
```

```
write_d(7); //5
write_d(8); //7
write_d(10); //9
write_d(12); //11
write_d(13); //13
write_d(13); //15
write_d(14); //17
write_d(14); //19
write_d(15); //21
write_d(16); //23
write_d(17); //25
write_d(18); //27
write_d(19); //29
write_d(23); //31
write_d(28); //33
write_d(33); //35
write_d(34); //37
write_d(38); //39
write_d(41); //41
write_d(49); //43
write_d(50); //45
write_d(53); //47
write_d(65); //49
write_d(67); //51
write_d(79); //53
write_d(85); //55
write_d(96); //57
write_d(106); //59
write_d(116); //61
write_d(127); //63
write_d(1); //1
write_d(8); //3
write_d(10); //5
write_d(13); //7
write_d(15); //9
write_d(16); //11
write_d(17); //13
write_d(18); //15
write_d(18); //17
write_d(19); //19
write_d(20); //21
write_d(29); //23
write_d(32); //25
write_d(33); //27
write_d(34); //29
write_d(35); //31
write_d(39); //33
write_d(43); //35
write_d(49); //37
write_d(50); //39
write_d(53); //41
write_d(58); //43
write_d(65); //45
write_d(67); //47
write_d(72); //49
write_d(80); //51
write_d(84); //53
write_d(94); //55
```

```
write_d(99); //57
write_d(110); //59
write_d(116); //61
write_d(127); //63
write_d(1); //1
write_d(4); //3
write_d(6); //5
write_d(9); //7
write_d(10); //9
write_d(12); //11
write_d(13); //13
write_d(13); //15
write_d(14); //17
write_d(14); //19
write_d(15); //21
write_d(16); //23
write_d(17); //25
write_d(18); //27
write_d(19); //29
write_d(22); //31
write_d(28); //33
write_d(32); //35
write_d(34); //37
write_d(36); //39
write_d(43); //41
write_d(49); //43
write_d(50); //45
write_d(55); //47
write_d(64); //49
write_d(68); //51
write_d(80); //53
write_d(87); //55
write_d(97); //57
write_d(106); //59
write_d(116); //61
write_d(127); //63
write_c(0x29); //Disable All Pixels On/Off
```

Sub function for 80 interface:

```
void write_c(unsigned char out_command)

{
bD_C=0;
bCS=0;
bR_W=0;
P1=out_command;
bR_W=1;
bCS=1;
bD_C=1;
}
```

```
void write_d(unsigned char out_data)

{
bD_C=1;
bCS=0;
bR_W=0;
P1=out_data;
bR_W=1;
bCS=1;
}
```

Note：
1. For 80 series CPU interface.
2. For 8 Bbit Ttiple Transfer 252K support.