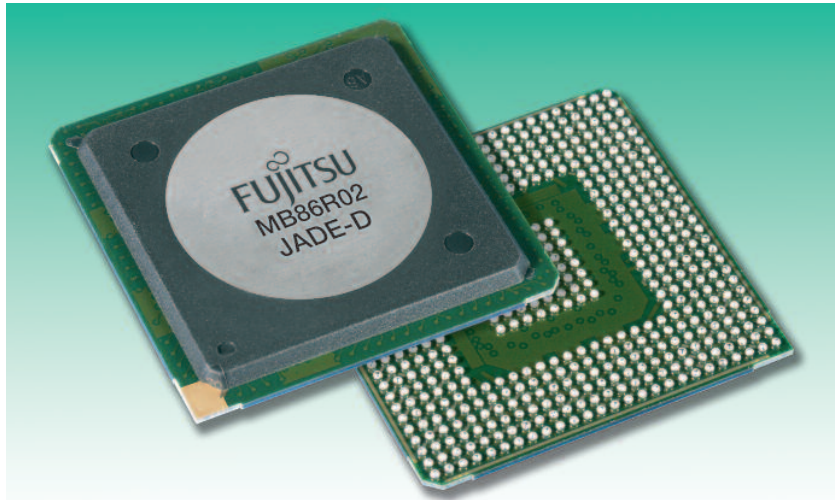# MB86R02 'JADE-D' system-on-chip graphics controller

The new system-on-chip graphics controller MB86R02 is a very versatile device with a large palette of interfaces, offering a wide scope of potential application fields

Description

MB86R02 'Jade-D' is a highly-integrated device for embedded automotive graphics applications. Incorporating an ARM926EJ-S CPU core, together with an enhanced version of the successful MB86296 'Coral PA' graphics processor and a number of external interfaces, this 90nm technology device is highly optimised for various types of applications that require outstanding CPU performance in combination with sophisticated 2D/3D graphics features in a compact SoC. Target applications include on-board and mobile navigation systems, graphical dashboard systems, HUD (head-up display) units, rear seat entertainment systems, point-of-sale terminals and industrial control panels.

Key features

- CMOS 90nm technology
- ARM926EJ-S CPU core with 16kB instruction and 16kB data cache
- CPU core: 16kB ITCM / 16kB DTCM, ETM9 and JTAG ICE interface
- Internal/memory frequency: 320MHz
- Display resolutions typically from 320 x 240 up to 1024 x 768
- 6 layers of overlay display (Windows)
- Alpha plane and constant alpha value for each layer
- Dual display output (2 separate display controllers are integrated supporting RGB8, RGB16 and RGB24)
- Dual digital video input (2 separate video capture units supporting various formats including YUV, RGB and ITU656)

- Video scaler (up/down scaling)
- Brightness, contrast, saturation control
- Rendering engine for 2D/3D graphic acceleration functions
- Geometry processor supporting floating point transformations
- Texture mapping unit (up to 4096 x 4096)
- Bit BLT Unit for transfers up to 4096 x 4096 surfaces
- Spread-spectrum clock generator (SSCG) for improved EMI reduction
- Alpha Bit BLT and ROP2 functions
- Run-length Decoder unit (RLD)
- External DDR2-SDRAM interface (320MHz) for graphic memory (up to 128MBytes), 3 chip selects
- Parallel flash/SRAM host interface with decryption engine
- CAN interface (2 ports)
- MediaLB interface
- Innovative APIX™ GBit/s interface (Automotive Pixel Link) 2 channels, both individually configurable for Tx (=clk master mode) or Rx (=slave mode)
- Embedded Timing Controller (TCON) for direct display connection and control
- I²C interface (x2)
- I²S interface
- UART interface (x6)
- BGA-484 package
- Temperature range -40 to +105°C
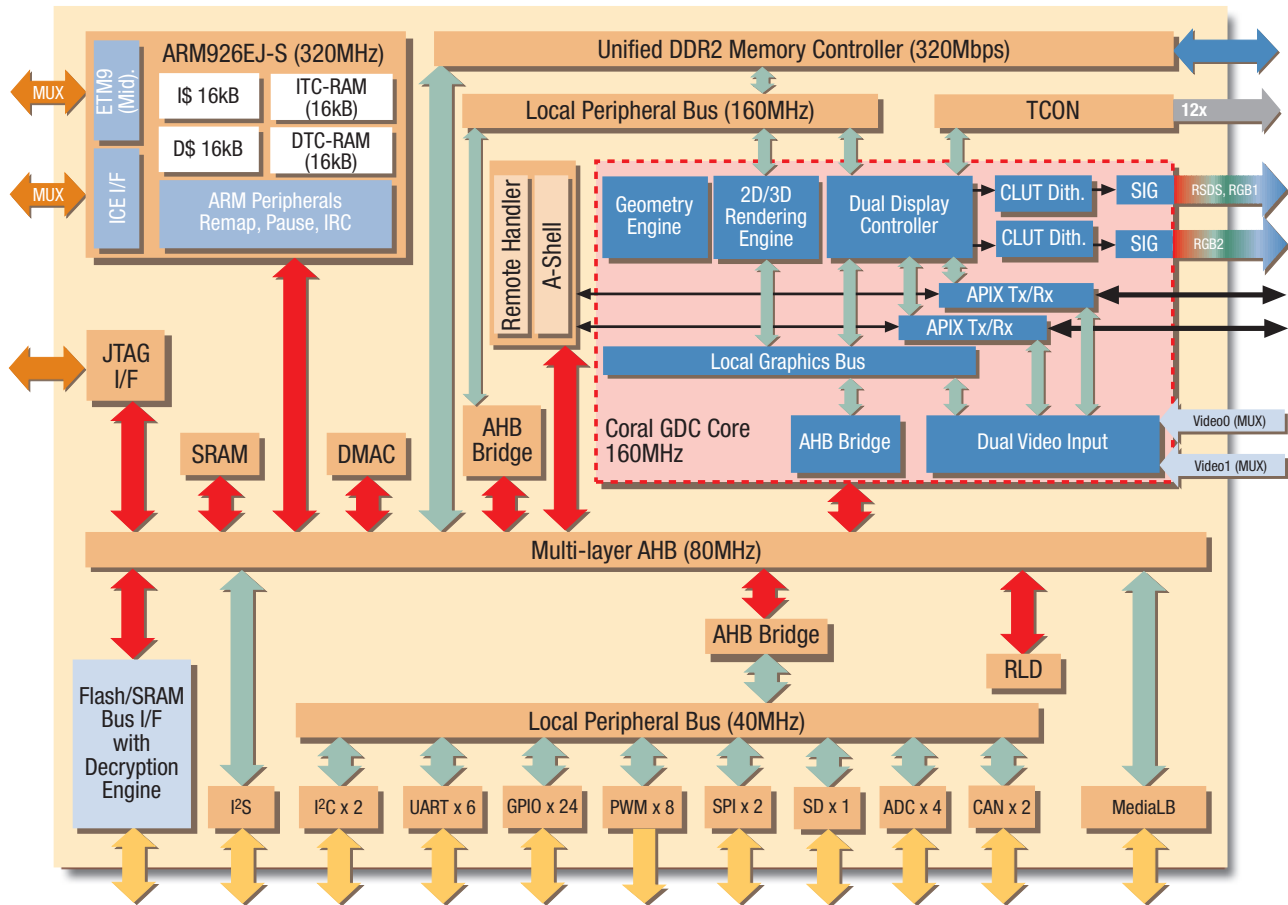
MB86RO2 block diagram

One of the unique features of the MB86RO2 is the dual APIX™ serial gigabit interface from Inova Semiconductors. The APIX technology is becoming the new standard for peer to peer real-time transmissions of video and peripheral data in the car. It meets the strict EMC requirements of display applications in vehicles and because of its SoC-integration options, it leads to higher performance at significantly lower system costs.

Fujitsu was the first silicon vendor on the market to integrate this new video interface into a portfolio of microcontrollers and graphics controllers. The built-in links in the MB86RO2 can be used for various link speeds up to 1Gbit/s. Both are configurable as transmitter or receiver, and support the sideband channel for peripheral data.

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