A DIVISION OF CIRRUS LOGIC

CS6420

Full-Duplex Speakerphone Chip

Features

- Single-chip full-duplex hands-free operation
- Automatic gain control
- Optional 34 dB microphone preamplifier
- Integrated mute and volume control
- Integrated 80 dB IDR dual codec
- Speech-trained Network and Acoustic Echo Cancellers
- Powerdown mode
- Microcontroller Interface

General Description

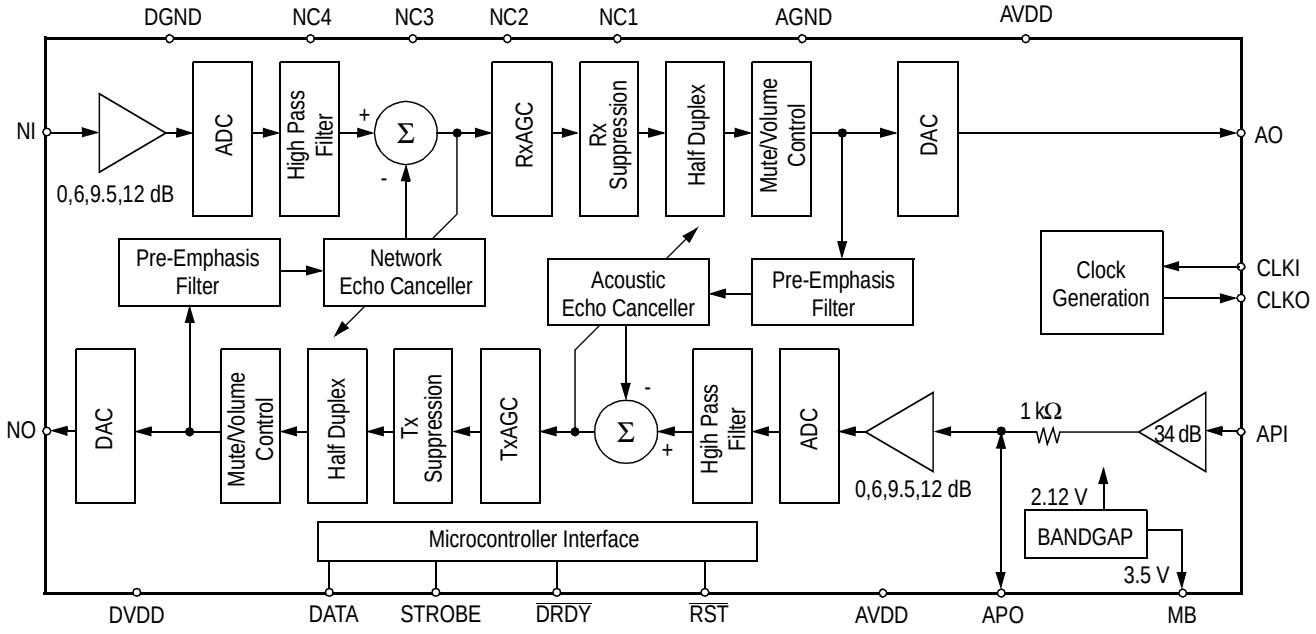
Most modern speakerphones use half-duplex operation, which switches transmission between the far-end talker and the speakerphone user. This is done because the acoustic coupling between the speaker and microphone is much higher in speakerphones than in handsets where the coupling is mechanically suppressed.

The CS6420 enables full-duplex conversation with a single-chip solution. The CS6420 can easily replace existing half-duplex speakerphone ICs with a huge increase in conversation quality.

The CS6420 consists of telephone & audio interfaces, two codecs and an echo-cancelling DSP.

ORDERING INFORMATION

CS6420-CS	20-pin SOIC
CDB6420	Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (AVDD, DVDD)			-0.3	6.0	V
Input Current (Except supply pins)		I_{in}	-10	+10	mA
Input Voltage	Analog Digital	V_{ina} V_{ind}	-0.3 -0.3	AVDD+0.3 DVDD+0.3	V
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (AVDD, DVDD)		4.5	5.0	5.5	V
Ambient Operating Temperature	T_{AOp}	0	25	70	°C

POWER CONSUMPTION (T_A = 25°C, DVDD = AVDD = 5V, f_{XTAL} = 20.480 MHz) (Note 1)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Current, Analog ($\overline{RST}$=0)	P_{DA0}			1	mA
Power Supply Current, Analog ($\overline{RST}$=1)	P_{DA}		10	20	mA
Power Supply Current, Digital ($\overline{RST}$=0)	P_{DD0}			1	mA
Power Supply Current, Digital ($\overline{RST}$=1)	P_{DD}		50	60	mA

Notes: 1. AO and NO outputs are not loaded.

ANALOG CHARACTERISTICS (T_A = 25°C, DVDD = AVDD = 5V, f_{XTAL} = 20.480 MHz)

Parameter		Symbol	Min	Typ	Max	Units
Input Offset Voltage (APO, NI)				2.12		V
Output Offset Voltage (AO, NO)				2.12		V
Transmit Group Delay	(Note 2)				6	ms
Receive Group Delay	(Note 2)				6	ms
Settling Time from $\overline{RST}$ rising				104		ms
MB Output Voltage				3.5		V
MB Drive Capability				10		µA
Input Impedance (APO, NI)	(Note 2)	Z_{in}		300		kΩ
Load Impedance (AO, NO)	(Note 2)	Z_{load}	10			kΩ
Power Supply Rejection (1 kHz)				40		dB

Notes: 2. These parameters are guaranteed by design or by characterization.

ANALOG TRANSMISSION CHARACTERISTICS (T_A = 25°C, DVDD = AVDD = 5V, f_{XTAL} = 20.480 MHz, RVol=TVol=RGain=TGain= 0 dB, HD=TSD=RSD=1, analog inputs and ouputs loaded with resistors and capacitors as shown in the typical connection diagram, Figure 2)

Parameter		Symbol	Min	Typ	Max	Units
Idle Channel Noise	A-weighted (0-20 kHz)				-69	dBV
(Inputs grounded	C-Message weighted (0-4 kHz)			17		dBrnC0
through a capacitor)	Psophometrically weighted (0-4 kHz)			-67		dBm0p
Signal-to-Noise Ratio	A-weighted (0-20 kHz)	SNR	69			dB
(Full Scale, 1 kHz	C-Message weighted (0-4 kHz)			17		dBrnC0
sine wave input)	Psophometrically weighted (0-4 kHz)			-67		dBm0p
Total Harmonic Distortion	C-Message Weighted (0-4 kHz)	THD			0.1	%
Programmable Gain	RGain/TGain = 00			0		dB
	RGain/TGain = 01			6		
	RGain/TGain = 10			9.5		
	RGain/TGain = 11			12		
Volume Control Stepsize (TVol/RVol)				3		dB
ADC Full-scale Voltage Input			0.9	1.0		Vrms
DAC Full-scale Voltage Output				1.0	1.1	Vrms
ADC Noise Floor	C-Message Weighted (0-4 kHz)				-80	dBV
DAC Noise Floor, DAC muted	C-Message Weighted (0-4 kHz)				-85	dBV

MICROPHONE AMPLIFIER (T_A = 25°C, DVDD = AVDD = 5V,f_{XTAL} = 20.480 MHz)

Parameter		Symbol	Min	Typ	Max	Units
Gain (Zsource = 50Ω)		A_{mic}		34		dB
Signal-to-Noise Ratio	A-weighted (0-20 kHz)	SNR_m		63		dB
Input Impedance		Z_{inm}		5		kΩ
Input Offset Voltage		V_{offm}		2.12		V

DIGITAL CHARACTERISTICS (T_A = 25°C, DVDD = AVDD = 5V,f_{XTAL} = 20.480 MHz)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	DVDD-1.0			V
Low-Level Input Voltage	V_{IL}			1.0	V
Input Leakage Current	I_{leak}			10	µA
Input Capacitance	C_{IN}		5		pF

SWITCHING CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Input rise time	t_{rise}			1.0	µs
$\overline{RST}$ low time	t_{RSTL}	1.0			µs
CLKI frequency	f_{XTAL}	18.432	20.480	22.528	MHz
CLKI duty cycle	t_{LCLKI}	40	50	60	%
$\overline{DRDY}$ frequency	f_{DRDY}	DC		f_{XTAL}/ 2560	kHz
STROBE frequency	f_{STROBE}	DC		9.0	MHz
$\overline{DRDY}$ to STROBE setup time	t_{sDRDY}	30			ns
DATA to STROBE setup time	t_{sDATA}	30			ns
STROBE to DATA hold time	t_{hDATA}	30			ns
STROBE to $\overline{DRDY}$ hold time	t_{hDRDY}	30			ns

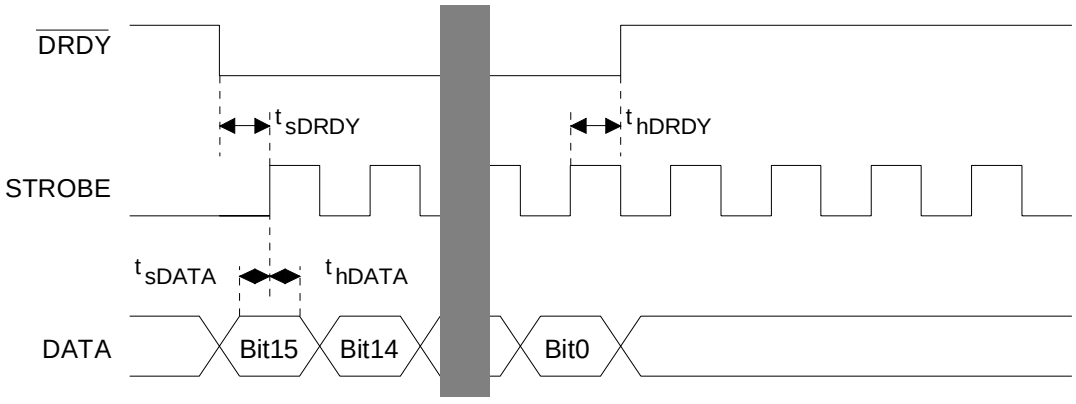


Figure 1. Microcontroller Interface Switching Characteristics

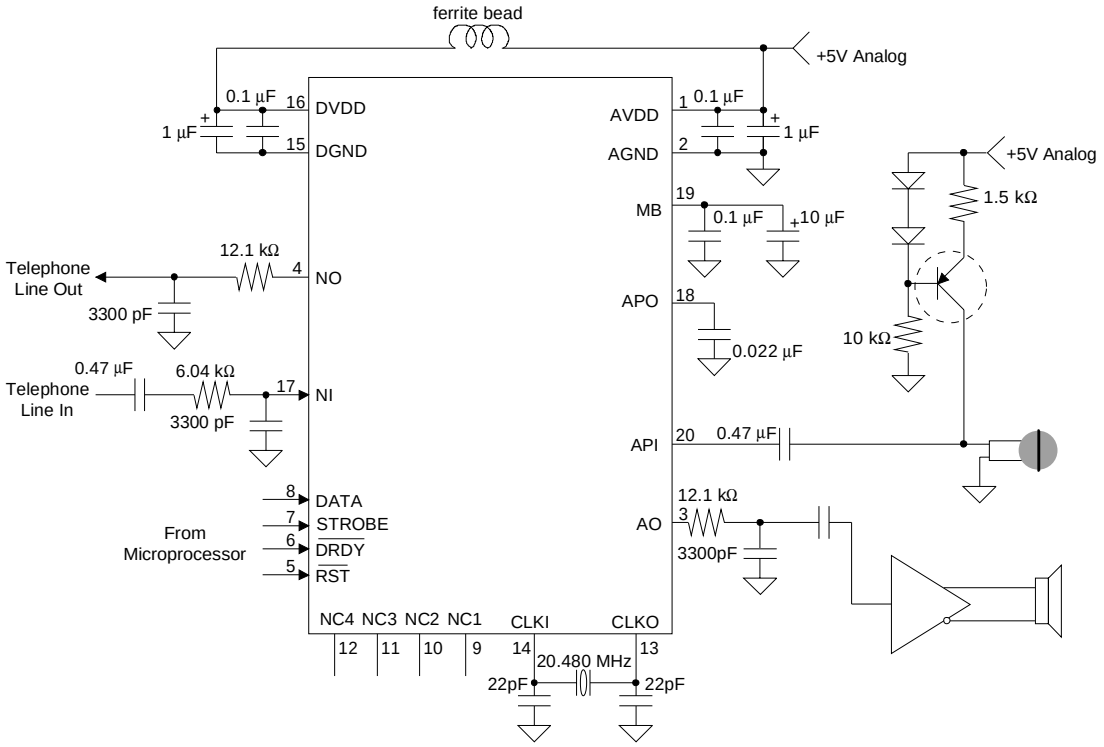


Figure 2. Typical Connection Diagram (Microphone Preamplifier Enabled)

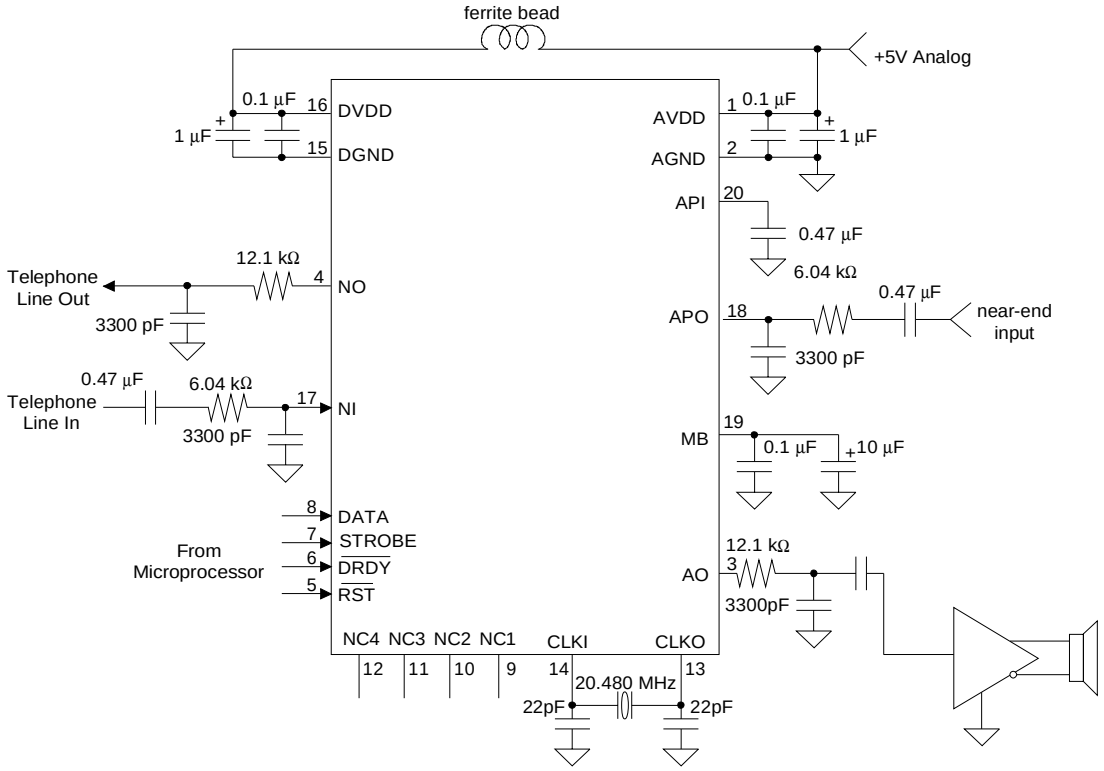


Figure 3. Typical Connection Diagram (Microphone Preamplifier Disabled)

OVERVIEW

The CS6420 is a full-duplex speakerphone chip for use in hands-free communications with telephony quality audio. Common applications include speakerphones, inexpensive video-conferencing, and cellular phone car kits. The CS6420 requires very few external components and allows system control through a microcontroller interface.

Hands-free communication through a microphone and speaker typically results in acoustic feedback or howling because the loop gain of the system exceeds unity by the time audio amplitudes are adjusted to a reasonable level. The solution to the howling problem has typically been half-duplex, where either the transmit or the receive channel is active, never both at the same time. This prevents the howling, but diminishes the overall communication quality by clipping words and forcing the talker at each end to wait for the talker at the other end to stop speaking.

Full-duplex conversation, where both transmit and receive channels are active simultaneously, is the conversation quality we enjoy when using handsets. Full-duplex for hands-free communications is achieved in the CS6420 using a digital signal processing technique called “Echo Cancellation.” The end result is a more natural conversation than half-duplex, with no awkward breaks and pauses, as if both parties were speaking to each other directly.

Echo Cancellation reduces overall loop gain and the acoustic coupling between speaker and microphone. This coupling reduction prevents the annoying effect of hearing one’s own delayed speech, the effect being worse when there is delay in the system, such as vocoder delay in digital cellular phones.

The CS6420 is a complete system implementation of a Digital Signal Processor with RAM and program ROM, running Echo Cancellation algorithms developed at Crystal Semiconductor using customer input, integrated with two delta-sigma codecs. The CS6420 is intended to provide a full-duplex speakerphone solution with a minimum of design effort while displacing existing half-duplex speakerphone chips.

FUNCTIONAL DESCRIPTION

The CS6420 is roughly divided into four external interface blocks. The analog interfaces connect the chip to the transmit and receive paths. Certain control functions are accessible through the microcontroller interface. Two pins accommodate either a crystal or an externally applied digital clock signal. Analog and digital power and ground are provided through four pins.

Analog Interface

In a speakerphone application, one input of the CS6420 connects to the signal from the microphone, sometimes called the near-end input or transmit input, and one output connects to the speaker. The output that leads to the speaker is sometimes called the near-end output or receive output. Together, the input and output that connect to the microphone and speaker are referred to as the Acoustic Interface.

The signal received at the near-end input is then passed to the far-end output or transmit output after acoustic echo cancellation. This signal is sent to the telephone line. The signal from the telephone line is received at the far-end input, also called the receive input, and this signal is passed to the receive output after network echo cancellation. Together, the far-end input and output form the Network Interface.

The analog interfaces are physically implemented using delta sigma converters running at an output word rate of 8 kHz, resulting in a passband from DC to 4 kHz. Because the inputs are analog to digital converters (ADCs), certain design considerations must be kept in mind: specifically, anti-aliasing and full-scale input voltage. The ADCs expect a single-pole RC filter with a corner at 8 kHz,

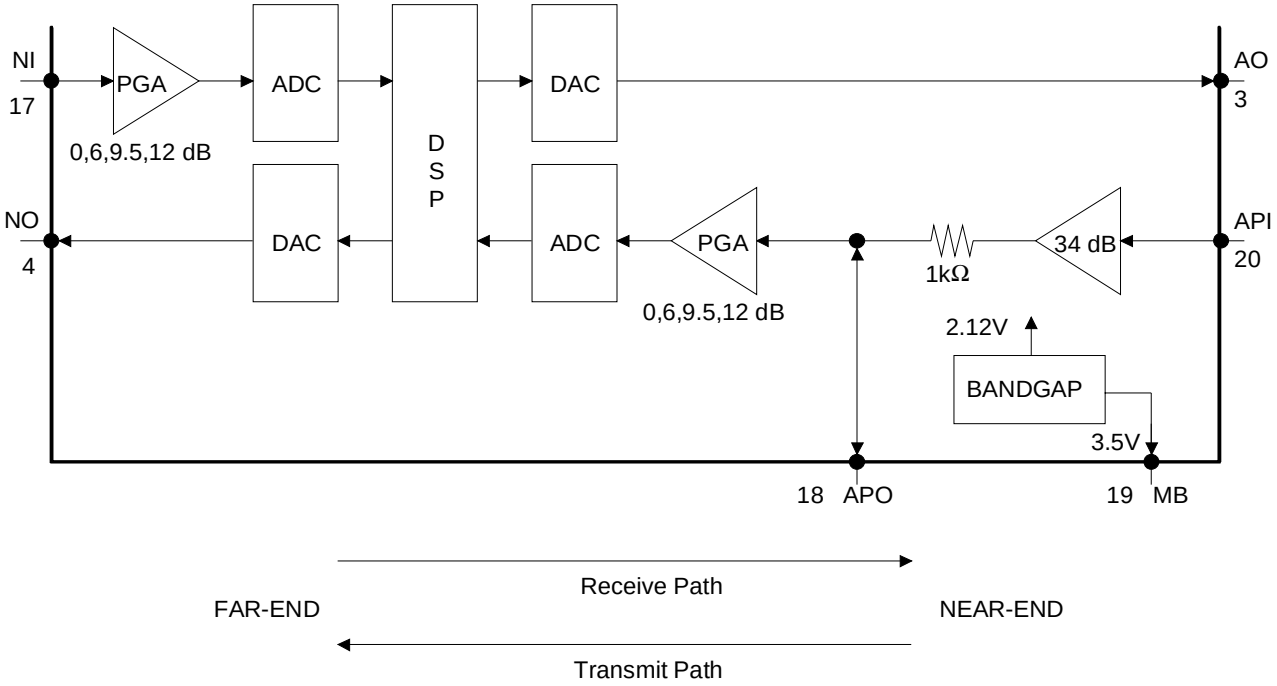


Figure 4. Analog Interface

and they are post-compensated internally to prevent any resultant passband droop. The ADCs also expect a maximum of 1 V_{rms} (2.8 V_{pp}) at their inputs (which are biased around 2.12 VDC). A signal of higher amplitude will clip the ADC input and may result in poor echo canceller performance. See the *Design Considerations* section for more details.

The outputs are delta-sigma digital to analog converters (DACs) and have similar requirements to the ADCs. The DACs are pre-compensated to expect a single-pole RC filter with a corner frequency at 4 kHz. The full scale voltage output from a DAC is 1 V_{rms} (2.8 V_{pp}) swinging around a DC bias of 2.12 V.

Acoustic Interface

The pins API (pin 20), APO (pin 18), MB (pin 19), and AO (pin 3) make up the Acoustic Interface. A block diagram of the Acoustic Interface is shown in Figure 4.

API and APO are, respectively, the input and output of the built-in analog pre-amplifier. The pre-amplifier is an inverting amplifier with a fixed gain of 34 dB biased around an input offset voltage (V_{off}) of 2.12 V. APO is the output of the pre-amplifier after a 1 kΩ resistor. The circuitry connected to the amplifier input must present low source impedance (<100Ω) to the API pin or the gain will be reduced. When using the pre-amplifier, connecting a 0.022 µF capacitor to ground off APO will provide the anti-aliasing filter required by the ADC, as shown in Figure 2. The pre-amplifier may be bypassed by clearing Mic (Register 0, bit 15) using the Microcontroller Interface (see *Microcontroller Interface* section), grounding API through a capacitor, and driving APO directly. In this case, the signal into APO must be low-pass filtered by a single-pole RC filter with a corner frequency at 8 kHz (see Figure 3).

Following the pre-amplifier is a programmable analog gain stage (PGA) which is controllable through the Microcontroller Interface. This gain

stage allows gains of 0 dB, 6 dB, 9.5 dB, and 12 dB to be added prior to the ADC input. The default gain stage setting is 0 dB.

The signal at APO should not exceed 2.8 V_{pp} at the default gain stage setting. If other gain stages are used then the full-scale signal at APO must also change. Table 1 shows full-scale voltages as measured at APO for given programmable gains:

Gain Setting	Full-scale Voltage
0 dB	2.8 V_{pp}
6 dB	1.4 V_{pp}
9.5 dB	0.94 V_{pp}
12 dB	0.71 V_{pp}

Table 1. Full scale voltages for each gain stage.

MB provides a stable 3.5 VDC output from the onboard voltage reference of the CS6420. MB may not be connected to any load. MB serves to provide decoupling for the internal 2.12 VDC bandgap reference, and must have a 0.1 µF and a 10 µF capacitor to ground for bypass. **Noise on MB will strongly influence the overall analog performance of the CS6420.**

The acoustic output, AO, should connect to a single-pole low-pass RC network with a corner frequency of 4 kHz, which will filter out-of-band components. The maximum voltage swing at AO is 2.8 V_{pp}. AO is capable of driving down to a 10 kΩ load.

Network Interface

The pins NI (pin 17) and NO (pin 4) make up the Network Interface. The details of the Network Interface are shown in Figure 4.

NI is the input from the telephone network side into the CS6420. The signal into NI must be low pass filtered by a single-pole RC filter with a corner frequency of 8 kHz.

A programmable analog gain stage (PGA) accessible through the Microcontroller Interface amplifies signals received at NI. This gain stage allows gains of 0 dB, 6 dB, 9.5 dB, and 12 dB to be added prior to the ADC input. The default gain stage setting for the network side is 0 dB.

The signal at NI should not exceed 2.8 V_{pp} at the default gain stage setting. If other gain stages are used then the full-scale signal at NI must also change. Table 1 shows full-scale voltages as measured at NI for given programmable gains.

The output to the telephone network side, NO, should connect to a single pole RC network with a corner frequency at 4 kHz, which will filter out-of-band components. The maximum swing NO is capable of producing is 2.8 V_{pp}. NO is capable of driving down to a 10 kΩ load.

Microcontroller Interface

Several control functions of the CS6420 are accessible through its Microcontroller Interface, which consists of three pins: DATA (pin 8), STROBE (pin 7), and $\overline{\text{DRDY}}$ (pin 6). These inputs are intended to connect to the outputs of a microcontroller to allow write-only access to the 16-bit Microcontroller Control Register (MCR).

The $\overline{\text{RST}}$ (pin 5) pin, which affects the entire integrated circuit, is especially significant to the Microcontroller Interface. $\overline{\text{RST}}$ is used to place the CS6420 into a known state of operation. Two subtypes of reset are possible: cold reset and warm reset.

Description

The Microcontroller Interface is implemented by a serial shift register gated by $\overline{\text{DRDY}}$. The microcontroller begins the transaction by setting $\overline{\text{DRDY}}$ low and STROBE low. The most significant bit (MSB), Bit 15, of the 16-bit data word should be presented to the DATA pin and then STROBE should be brought high to shift the data bit into the CS6420. STROBE should be brought low again so it is ready

to shift the next bit into the shift register. The next data bit should then be presented to the DATA pin ready to be latched by the rising edge of STROBE. This procedure repeats for all sixteen bits as shown in Figure 5. After the last bit has been shifted in, $\overline{\text{DRDY}}$ should be brought high to indicate the conclusion of the transfer, and four extra STROBE pulses must be applied to latch the data into the CS6420.

Since the MCR is a shift register, the STROBE can be run arbitrarily slow with a duty cycle limited only by the hold time specified in the *Switching Characterstics* table. The Microcontroller Interface is read once every 125 µs, so it must not be updated faster than this.

Register Definitions

The four control registers accessible through the MCR are described in detail in the following tables. These registers are addressed by bits b2 and b1 of the MCR. Bit b0 must always be 0. Table 2 shows the relative bit positions of all the registers. Tables 3 to 6 show the four control registers in more detail.

The Register Map at the top of each register description shows the names of all the bits, with their reset values below the bitfield name. The reset value can also be found in the Word column of the bitfield summary as indicated by an '*'.

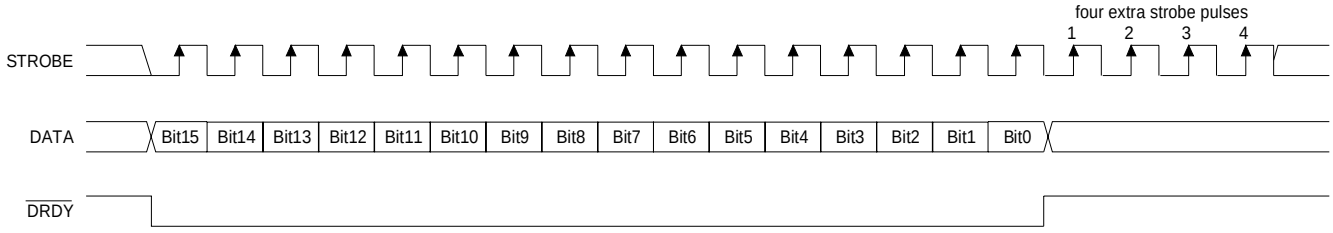


Figure 5. Microcontroller Interface

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Mic	TSD	GB		ACC		RVol					TGain		0	0	0
HD	RSD	Taps		NCC		TVol					RGain		0	1	0
NErle		NFNse		RHDet		HDly		NseRmp		RSThd		PCSen	1	0	0
AErle		AFNse		THDet		TSAtt		TSBias		TSThd		HHold	1	1	0

Table 2. MCR Control Register Mapping

Register 0

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Mic	TSD	GB		ACC		RVol					TGain		0	0	0
1	0	10		00		00100					00		0	0	0

Bits	Name	Function	Word	Operation
15	Mic	Microphone Preamplifier Enable	0 1*	disable preamp enable preamp
14	TSD	Tx Suppression Disable	0* 1	enable Tx suppression disable Tx suppression
13-12	GB	Graded Beta	00 01 10* 11	0.00 dB/ms 0.75 dB/ms 0.38 dB/ms 0.19 dB/ms
11-10	ACC	AEC Coefficient Control	00* 01 10 11	Normal Clear Freeze *reserved*
9-5	RVol	Rx Volume Control	00000 00001 --- 00100* --- 01010 01011 --- 11101 11110 11111	+30 dB +27 dB +18 dB +0 dB -3 dB -57 dB -60 dB mute
4-3	TGain	Tx Analog Gain	00* 01 10 11	0 dB 6 dB 9.5 dB 12 dB

* Denotes reset value

Table 3. Register 0 Bit Definitions

Mic - Microphone Preamplifier Enable

The microphone preamplifier described in the *Acoustic Interface* section is enabled by default, but may be disabled by setting Mic to 0. Refer to the *Acoustic Interface* section for more details on using/disabling the Microphone Preamplifier.

TSD - Transmit Suppression Disable

The Transmit Supplementary Echo Suppression function is a non-linear echo control mechanism. The Transmit Suppression will introduce TSAtt (see Register 3) dB of attenuation into the transmit path only when there is speech detected in the receive path and no near-end speech. When only near-end speech is present, or if there is no speech in either direction, the suppression attenuation is removed. By default, the transmit suppression function is enabled.

GB - Graded Beta

The room-size adjustment scheme called “graded beta,” provided for the acoustic echo canceller in the

CS6420, is controlled by GB. The network echo canceller does not support graded beta.

Graded beta is an architectural enhancement to the CS6420 which takes advantage of the fact that acoustic echoes tend to decay exponentially with time. The CS6420 can increase the beta, or update gain, for the coefficients of the adaptive filter which occur earlier in time and decrease it for those that occur later in time, which increases convergence speed while maintaining stability. In order to make this improvement, there is an implicit assumption that the decay rate of the echo is known. The graded beta control allows the system designer to adjust this. For very acoustically live rooms, use either no decay (00) or slight decay (11). Cars and acoustically dead rooms can benefit from the most rapid decay (01).

ACC - Acoustic Coefficient Control

The coefficients of the AEC adaptive filters in the CS6420 are controlled by ACC. The default position (00) yields normal operation, which means the coefficients are free to adjust themselves to the echo path in order to cancel echo. When set to the clear position (01), the adaptive filter coefficients are all held at zero, so the echo canceller is effectively disabled. Note that unless the half-duplex mode is disabled, this will force the CS6420 into half-duplex mode. The freeze position (10) causes the coefficients to hold their current values.

RVol - Receive Volume Control

Volume in the receive path is set by RVol. The volume control in the receive direction is implemented by a peak-limiting automatic gain control (AGC) and digital attenuation at the near-end output DAC.

The AGC is discussed in detail in the *Design Considerations* section. See the sub-section on *AGC* for a full explanation of how it functions.

When the reference level is set to +0 dB, the AGC is effectively disabled. Volume control is implemented by digital attenuation in 3 dB steps from this point on down. The maximum gain is +30 dB and the minimum is -60 dB in 3 dB steps. The lowest gain setting (11111) mutes the receive path.

The default setting for the receive reference level is +18 dB.

TGain - Transmit Analog Gain

TGain selects the amount of additional on-chip analog gain to be supplied to the acoustic input of the CS6420. A programmable gain amplifier (PGA) exists before each ADC which allows 0 dB, 6 dB, 9.5 dB, or 12 dB of gain to be added to the signal path. The acoustic side defaults to 0 dB of gain.

Note: Changing the analog gain will change the full-scale voltage as applied to the input pin. Make sure that the ADC input does not clip with the gain stage on.

Register 1

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
HD	RSD	Taps		NCC		TVol					RGain		0	1	0
0	0	10		00		01010					00		0	1	0

Bits	Name	Function	Word	Operation
15	HD	Half-Duplex Disable	0* 1	enable half-duplex disable half-duplex
14	RSD	Rx Suppression Disable	0* 1	enable Rx suppression disable Rx suppression
13-12	Taps	AEC/NEC Tap Allocation	00 01 10* 11	444/0 (55.5ms/disabled) 380/128 (47.5ms/16ms) 316/192 (39.5ms/24ms) 252/256 (31.5ms/32ms)
11-10	NCC	NEC Coefficient Control	00* 01 10 11	Normal Clear Freeze *reserved*
9-5	TVol	Tx Volume Control	00000 00001 --- 00100 --- 01010* 01011 --- 11101 11110 11111	+30 dB +27 dB +18 dB +0 dB -3 dB -57 dB -60 dB mute
4-3	RGain	Rx Analog Gain	00* 01 10 11	0 dB 6 dB 9.5 dB 12 dB

* Denotes reset value

Table 4. Register 1 Bit Definitions

HD - Half-Duplex Disable

In normal operation, the CS6420 will be in a half-duplex mode if the echo canceller is not providing enough loop gain reduction to prevent howling. This half-duplex mode would be active at power-up, for example, before the adaptive filter has had a chance to adapt. This half-duplex mode prevents howling and also masks the convergence process.

In some cases, such as when measuring convergence speed (see *Testing Issues*), the half-duplex mode is undesirable. By default, the half-duplex mode is enabled.

RSD - Receive Suppression Disable

The Receive Supplementary Echo Suppression function is a non-linear echo control mechanism. Supplementary Echo Suppression attenuates signals in the receive direction by 24 dB when far-end speech is absent in the receive path. The attenuation is released only when the receive channel is active. It is also designed to not be triggered by

network echo. By default, the receive suppression function is enabled.

Taps - AEC/NEC Tap Allocation

The CS6420 has a total of 63.5 ms of echo canceller taps that it can partition for use by the network and acoustic echo cancellers. By default, the CS6420 allocates 39.5 ms for the AEC and 24 ms for the NEC. Some applications will never have a network echo path, and so should allocate all taps for the AEC. See NErle and NFNse in Register 2, and AErle and AFNse in Register 3 for more options when an echo path is nonexistent.

NCC - Network Coefficient Control

The NEC adaptive filter's coefficients are controlled by NCC. See ACC in Register 0 for more details. The default setting for NCC is Normal mode.

TVol - Transmit Volume Control

Volume in the transmit path is controlled by TVol. Like receive volume, the transmit volume is controlled by an AGC. See RVol in Register 0 for more details. The default setting for the transmit reference level is +0 dB.

RGain - Receive Analog Gain

RGain selects the amount of additional on-chip analog gain to be supplied to the network input of the CS6420. A programmable gain amplifier (PGA) exists before each ADC which allows 0 dB, 6 dB, 9.5 dB, or 12 dB of gain to be added to the signal path. The network side defaults to 0 dB of gain.

Note: Changing the analog gain will change the full-scale voltage as applied to the input pin. Make sure that the ADC input does not clip with the gain stage on.

Register 2

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
NErle		NFNse		RHDet		HDly		NseRmp		RSThd		PCSen	1	0	0
00		00		00		00		00		00		0	1	0	0

Bits	Name	Function	Word	Operation
15-14	NErle	NEC ERLE Threshold	00* 01 10 11	24 dB 18 dB 30 dB *reserved*
13-12	NFNse	NEC Full-Duplex Noise Threshold	00* 01 10 11	zero -42 dB -54 dB *reserved*
11-10	RHDet	Rx Half-Duplex Detection Threshold	00* 01 10 11	5 dB 3 dB 6 dB *reserved*
9-8	HDly	Half-Duplex Holdover Delay	00* 01 10 11	200 ms 100 ms 150 ms *reserved*
7-6	NseRmp	Background Power Estimator Ramp Rate	00* 01 10 11	1 s 0.5 s 2 s *reserved*
5-4	RSThd	Rx Suppression Threshold	00* 01 10 11	5 dB 3 dB 6 dB *reserved*
3	PCSen	Path Change Sensitivity	0* 1	high sensitivity low sensitivity

* Denotes reset value

Table 5. Register 2 Bit Definitions

NErle - Network ERLE Threshold

The CS6420 will allow full-duplex operation only when the Network ERLE exceeds the threshold set by NErle. See also NFNse. See *Glossary* for a definition of ERLE.

NFNse - Network Full-Duplex Noise Threshold

NFNse works in conjunction with NErle to determine when the CS6420 should transition into full-duplex operation. If the current noise level at the far-end input is greater than NFNse, then NErle is used to determine if full-duplex is allowed. If the noise level is below the level of NFNse, the CS6420 uses an internal estimate of asymptotic performance to determine whether or not to transition to full-duplex. If NFNse is zero, NErle is always used as the full-duplex criterion. The other values exist for cases where there is not a network path to converge to, or the existence of a network path can not be determined prior to placing a call.

RHDet - Receive Half-Duplex Detection Threshold

The sensitivity of the speech detector controls channel switching and ownership in half-duplex mode. The receive speech detector registers speech if the receive channel signal power is RHDet above the noise floor for the receive channel.

HDly - Half-Duplex Holdover Delay

After a channel goes idle in the half-duplex mode of operation, a change of channel ownership is inhibited for HDly in order to prevent false switching due to echoes. The half-duplex will be more immune to false switching if this delay is longer, but it will also prevent a fast response to legitimate channel changes.

NseRmp - Background Noise Power Estimator Ramp Rate

The background noise power estimators increase at a rate of 3 dB/NseRmp until the background noise power estimate equals the current input power estimate. The background noise power estimators quickly track drops in the current input power estimate. Choose small values of NseRmp if the environment is expected to have rapidly varying noise levels. Choose large values of NseRmp if the environment is expected to have relatively constant noise power.

RSThd - Receive Suppression Threshold

This parameter sets the threshold for far-end speech detection for disengaging receive suppression. The speech detector that disengages the receive suppression has its sensitivity controlled by RSThd. The suppression is inserted into the receive path unless signal from the far-end exceeds the receive channel noise power by RSThd, in which case speech is assumed to be detected and the suppression is defeated until speech is no longer detected. Decreasing RSThd to make the speech detector more sensitive could result in false detections due to spurious noise events which may cause an unpleasant noise modulation at the near-end. Increasing RSThd to make it robust to spurious noise, but may cause weak far-end talkers to not be heard. RSThd does not affect the ability of the receive suppressor to attenuate residual network echo.

PCSen- Path Change Sensitivity

The Acoustic Interface is likely to have many path changes, for example, as people move about in the room where the full-duplex speakerphone is being used. The sensitivity of the path change detector can be changed with the PCSen Bit. Set PCSen to 0 for high sensitivity and 1 for low sensitivity.

If PCSen is set to high, extended doubletalk may cause the CS6420 to briefly drop into half-duplex. When PCSen is set to low, brief echo may be heard during path changes.

Register 3

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AErle		AFNse		THDet		TSAtt		TSBias		TSThd		HHold	1	1	0
00		00		00		00		00		00		0	1	1	0

Bits	Name	Function	Word	Operation
15-14	AErle	AEC ERLE Threshold	00* 01 10 11	24 dB 18 dB 30 dB *reserved*
13-12	AFNse	AEC Full-Duplex Noise Threshold	00* 01 10 11	zero -42 dB -54 dB *reserved*
11-10	THDet	Tx Half-Duplex Detection Threshold	00* 01 10 11	5 dB 3 dB 6 dB *reserved*
9-8	TSAtt	Tx Suppression Attenuation	00* 01 10 11	18 dB 12 dB 24 dB *reserved*
7-6	TSBias	Tx Suppression Bias	00* 01 10 11	18 dB 15 dB 21 dB *reserved*
5-4	TSThd	Tx Suppression Threshold	00* 01 10 11	15 dB 12 dB 9 dB *reserved*
3	HHold	Hold in Half-Duplex on Howl	0* 1	disable enable

* Denotes reset value

Table 6. Register 3 Bit Definitions

AErle - Acoustic ERLE Threshold

The CS6420 will allow full-duplex operation only when the Acoustic ERLE it provides exceeds AErle. See also AFNse. See *Glossary* for a definition of ERLE.

AFNse - Acoustic Full-Duplex Noise Threshold

AFNse works in conjunction with AErle to determine when the CS6420 should transition into full-duplex operation. If the current noise level at the near-end input is greater than AFNse, then AErle is used to determine if full-duplex is allowed. If the noise level is below the level of AFNse, the CS6420 uses an internal estimate of asymptotic performance to determine whether or not to transition to full-duplex. If AFNse is zero, AErle is always used as the full-duplex criterion. The other values exist for cases where there may not be an acoustic path to converge to.

THDet - Transmit Half-Duplex Detection

Threshold

The sensitivity of the speech detector controls channel switching and ownership in half-duplex mode. The transmit speech detector registers speech if the transmit channel signal power is TH-Det above the noise floor of the transmit channel.

TSAtt - Transmit Suppression Attenuation

This parameter sets the amount of suppression attenuation inserted into the transmit path when transmit suppression is engaged.

TSBias - Transmit Suppression Bias

The bias level affects the ease with which near-end speech may break-in or be crushed by far-end speech. See the *Design Considerations* section on *Transmit Suppression* for full details.

TSThd - Transmit Suppression Threshold

This parameter sets the ERLE requirement for discrimination between echo and near-end speech by the supplementary echo suppressor. See the *Design Considerations* section on *Transmit Suppression* for full details.

HHold - Hold in Half-Duplex on Howl

This is a control flag which, if enabled, holds the system in the half-duplex operation if it were to howl for any reason and the howl detectors trip and clear coefficients. The system may transition to full-duplex if the flag is subsequently cleared.

Reset

A hardware reset, achieved by bringing $\overline{\text{RST}}$ low for at least 1 µs and then high again, must be applied after initial power-on.

When $\overline{\text{RST}}$ is held low, the various internal blocks of the CS6420 are powered down. When $\overline{\text{RST}}$ is brought high, the oscillator is enabled and approximately 4 ms later, all digital clocks begin operating. The ADCs and DACs are calibrated and all internal digital initializations occur. The MCR is sampled after the reset timer expires (104 ms after the rise of $\overline{\text{RST}}$ or sooner if using the early exit described below) to determine whether the reset was warm or cold. After the MCR is initially sampled, the default (reset) values of the MCR are restored to it.

Cold reset is a total reset of all the components of the CS6420. The ADCs and DACs are reset, the echo canceller memories and registers are all cleared, and the default settings of the MCR are restored. Cold reset is the default reset mode upon power up or in the absence of a microcontroller.

Warm reset is like cold reset except that the echo canceller coefficients and certain key variables are not cleared, but instead keep their pre-reset value. This gives the CS6420 a headstart in adapting to its environment if the echo environment is relatively stable, assuming a cold reset happened at least once since power up.

The CS6420 is warm reset by raising the $\overline{\text{RST}}$ pin high, waiting 4 ms for the digital clocks to start, and then writing 0111111111111110 (0x7FFE) to the MCR within 104 ms after $\overline{\text{RST}}$ goes high. If no control word is sent, the CS6420 will cold reset. If the control word is sent after the timer has expired, it is interpreted as a normal control word.

Another special reset option is to exit the 100 ms reset timer before the 100 ms has elapsed. This is accomplished by writing a control word to the MCR with Bit 15 set high. To exit the timer early in cold reset, write 1000000000000 (0x8000). The timer may be bypassed and warm reset asserted by sending 1111111111111110 (0xFFFE). The 100 ms timer prevents operation until the bias voltages generated on-chip settle, but the startup delay might be objectionable in some applications.

Clocking

The clock for the converters and DSP is provided via the clocking pins, CLKI (pin 14) and CLKO (pin 13). A 20.480 MHz parallel resonant crystal

placed between these two pins and loaded with 22 pF capacitors will allow the on-chip oscillator to provide this system clock. Alternatively, the CLKI pin may be driven by a CMOS level clock signal. The clock may vary from 20.480 MHz by up to 10%, however, this will change the sampling rate of the converters and echo canceller, which will affect the bandwidth of the analog signals and the duration of echo that the echo canceller can accommodate. CLKO is not connected when CLKI is driven by the CMOS signal.

Power Supply

The pins AVDD (pin 1) and AGND (pin 2) power the analog sections of the CS6420, and DVDD (pin 16) and DGND (pin 15) power the digital sections. This distinction is important because internal to the part, the digital power supply is likely to contain high-frequency energy. The analog power supply is kept clean internally by drawing current from a different pin, thereby achieving high performance in the converters.

The digital supply of the CS6420 should not be connected to the system digital supply, if there is one, as the CS6420 has internal timing mechanisms designed to minimize the detrimental effects of its own digital noise, but cannot use these to compensate for externally introduced digital noise. The CS6420 digital power supply should be derived from its analog power supply through a ferrite bead with low (< 1 Ω) DC impedance**.**

Power Down Mode

Typical power consumption of the CS6420 is 60 mA, assuming normal operating conditions. This current consumption can be further reduced by invoking the powerdown mode, which is entered by holding $\overline{\text{RST}}$ low. Holding $\overline{\text{RST}}$ low will power down all the internal blocks of the CS6420 and stop the oscillator. In powerdown mode, current consumption drops to less than 1 mA.

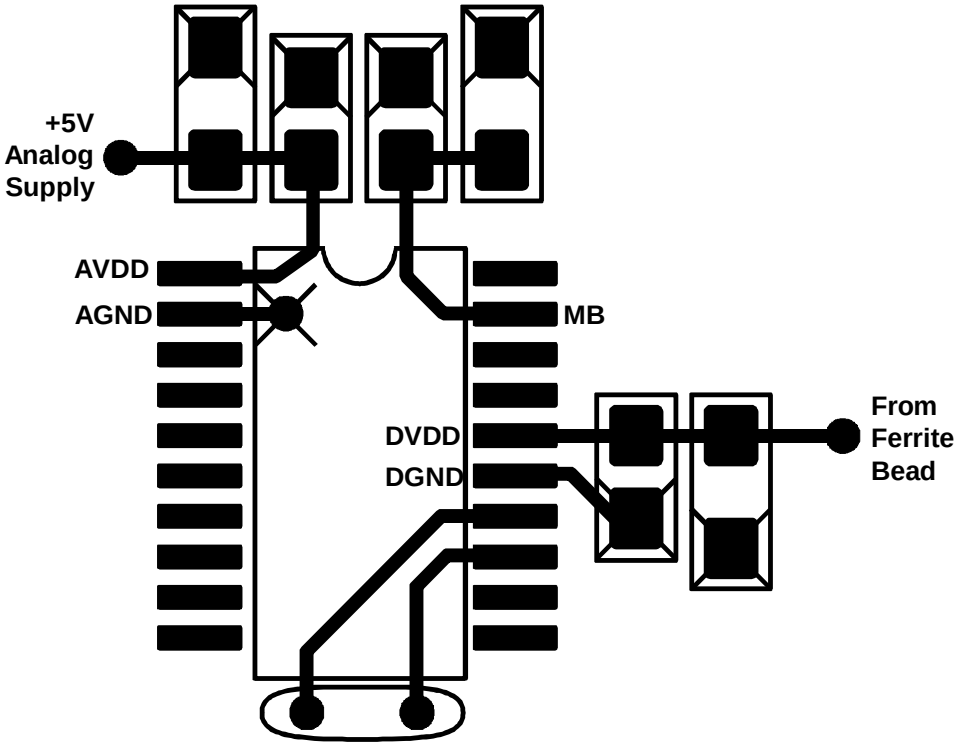


Figure 6. Suggested Layout

Noise and Grounding

Since the CS6420 is a mixed-signal integrated circuit, the system designer must pay special attention to layout and decoupling to minimize noise concerns. The three best methods to reduce noise when using the CS6420 are to have good decoupling of power supplies, separation of analog and digital power and ground, and careful board layout.

Figure 6 shows the suggested placement of decoupling capacitors for the power supplies. Note that the trace length from the power pin to the capacitors is minimized. Also note that the smaller valued capacitor is placed closer to the pin than the larger valued capacitor. The smaller capacitor decouples high frequency noise and the larger capacitor attenuates lower frequencies.

The separation of analog and digital power and ground is done in two ways. The power is separated by deriving the digital power for the CS6420 from the analog through a ferrite bead to isolate analog from digital, as shown in Figure 7. The ferrite bead serves as a low-pass filter to remove CS6420 digital switching noise from the analog power supply. The ground is separated by isolating all the digital components of the system board on one ground plane and all the analog and linear components on a different ground plane. The CS6420 should be placed over the analog ground plane. This prevents digital switching noise from the digital components of the board from coupling into the converters and aliasing into the passband.

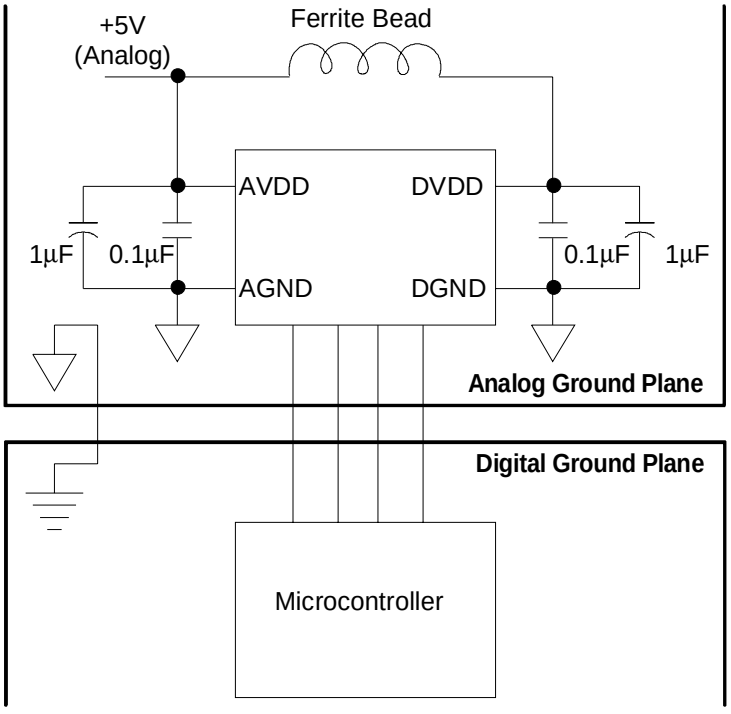


Figure 7. Ground Planes

DESIGN CONSIDERATIONS

When designing the CS6420 into a system, it is important to keep several considerations in mind. These concerns can be loosely grouped into three categories: algorithmic considerations, circuit design considerations, and system design considerations.

Algorithmic Considerations

The CS6420 facilitates full-duplex hands-free communication via many algorithms running on the Digital Signal Processor that is the core of the CS6420. Among these are the algorithms that perform the adaptive filtering, the half-duplex switching, digital volume control, and supplementary echo suppression.

Full-Duplex Mode

Full-duplex hands-free communication is achieved through a technique called adaptive filtering. The basic principle behind adaptive filtering is that the acoustic path between speaker and microphone can be modeled by a transfer function which can be dynamically determined by an adaptive digital filter. This principle assumes good update control and speech/tone detection algorithms to prevent the filter from mistraining.

Theory of Operation

Figure 8 illustrates how the adaptive filter can cancel echo and reduce loop gain. The echo path of the system is between points B and C: the speaker to microphone coupling. A signal injected at A (sometimes called a “training signal”) is sent both to B, the input of the echo path, and to F, the input of the adaptive filter. The signal at B is modified by the transducers and the environment, and received at point C (an “Echo”). Meanwhile, let us assume for argument’s sake that the adaptive filter has exactly the right transfer function to match the echo path BC, and so the signal at point D is approximately equal to the signal at point C. After these are subtracted by the summing element, all that is left is the error signal at point E, which should be very small.

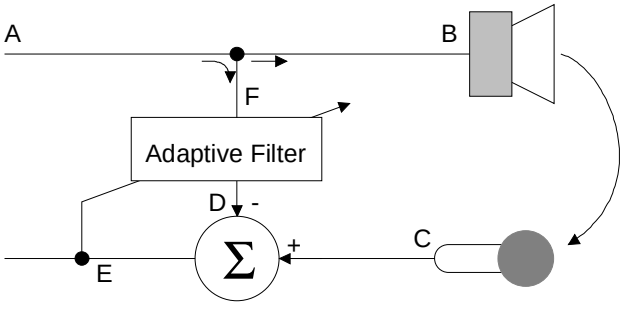


Figure 8. Simplified Acoustic Echo Canceller Block Diagram

If a person were to speak into the microphone at point C, that signal would pass through the summing element unchanged because the adaptive filter had no comparable input to subtract out. In this manner, the person at A and the person at C may simultaneously speak and A will not hear his own echo.

In the real world, the echo path is not static. It will change, for example, when people move in the room, when someone moves the speaker or the microphone, or when someone drops a piece of paper on top of the speaker. So, the filter needs to adapt to modify its transfer function to match that of the environment. It does so by measuring the error signal at point E and trying to minimize it. This signal is fed back to the adaptive filter to measure performance and how best to adapt, or train.

The trouble arises when the person at the near-end (C) speaks: the error signal will be non-zero, but the adaptive filter should not change. If it tries to train to the near-end signal, the adaptive filter has no way to reduce the error signal, because there is no input to the filter, and therefore no output from it. The adaptive filter would mistrain.

To prevent this mistraining, the echo canceller uses double-talk detection algorithms to determine when to update. These update control algorithms

are the heart of most echo canceller implementations.

The worst case situation for the CS6420 is when parties at both ends are speaking and the person at the near-end is moving. In this case, the echo canceller will cease to adapt because of the double-talk, but the echo will not be optimally reduced because of the change in path.

Adaptive Filter

The adaptive filter in the CS6420 uses an algorithm called the "Normalized Least-Mean-Square (NLMS)" update algorithm to learn the echo path transfer function. This Finite Impulse Response (FIR) filter has 508 taps, which can model up to 63.5ms of total path response at a sampling rate of 8kHz. The coverage time is calculated by the following formula:

$$\left(\frac{1}{8kHz}\right) \times 508 = 63.5 \text{ ms.}$$

The CS6420's adaptive filter, like all FIR filters, only models Linear and Time Invariant (LTI) systems. So, any non-linearity in the echo path can not be modeled by the adaptive filter and the resulting signals will not be cancelled. Signal clipping and poor-quality speakers are very common sources of non-linearity and distortion.

A common integration problem for echo cancellers is signal clipping in the echo path. For example, if a speaker driver is driven to its rails, the distortion of the speech may be hard to perceive, but it is very bad for the echo canceller. This technique has been used in half-duplex phones to provide good low-level signal gain at the expense of distortion with high amplitude signals. Since this does not work for the CS6420, an AGC mechanism has been introduced to provide equivalent behavior without clipping. See the section on *AGC* for more details.

Another common problem is speaker quality. A poor quality speaker which is perfectly acceptable for a half-duplex speakerphone, may limit the echo canceller's performance in a full-duplex speakerphone. The distortion elements will not be modeled by the adaptive filter and so limit its effectiveness. Speakers should have better than 2% THD performance to not impede the adaptive filter.

Volume control should be implemented only using the CS6420 Microcontroller Interface. A real-time external change in the gain of the speaker driver, for example, would result in a change in the transfer function of the echo path, and so would force the adaptive filter to readapt. If the volume control is done before the input to the adaptive filter, the echo path does not change, and no retraining is necessary. Another side benefit of the CS6420 volume control is that it transparently provides dynamic range compression.

Pre-Emphasis

The typical training signal for the adaptive filter will be speech, but most adaptive filters work optimally with white noise. Speech has very different spectral characteristics than white noise because of its quasi-periodic nature.

Research at Crystal has shown that quasi-periodic signals cause the formation of spurious non-zero coefficients within the adaptive filter at tap intervals determined by the periodicity of the signal. This results in small changes in period being very destructive to the adaptive filter's performance.

One mechanism the CS6420 uses to prevent this filter corruption with speech is to pre-emphasize the signal sent to the adaptive filter so that much of the low frequency content is removed.

The CS6420 works very well with a speech training signal because of the pre-emphasis filter. White noise training signals, however, will result in sub-optimal performance, so when testing, white noise is not recommended as a training signal.

Graded Beta

The update gain of an adaptive filter, sometimes called the "beta", is the rate at which the filter co-

efficients can change. If beta is too low, the adaptive filter will be slow to adapt. Conversely, if it is too high, the filter will be unstable and will create unwanted noise in the system.

In most echo canceller implementations, the beta is a fixed value for all the filter coefficients. In some situations, though, through knowledge of the characteristics of echo path response, the beta can be varied for groups of coefficients. This preserves stability by allowing the beta to be higher for some coefficients and compensating by reducing beta below nominal for others.

For example, acoustic echo tends to decay exponentially, so the first taps need to be large and the later taps will be small. Having a large beta for the first taps will allow those taps to be adapted faster, while having a small beta for the later taps will keep the filter stable. This has an added benefit of suppressing the spurious taps mentioned in the *Pre-Emphasis Filter* section above.

The Microcontroller Interface allows four settings for graded beta: none, 0.19 dB/ms, 0.38 dB/ms, and 0.75 dB/ms. Use 0.75 dB/ms for acoustically dead rooms or cars, and 0.19 dB/ms or no grading of beta for large, or acoustically live rooms.

Update Control

As mentioned in the *Theory of Operation* section, the update control algorithms are the heart of any useful echo canceller implementation. Aside from telling the adaptive filter when to adapt, they are responsible for correcting performance when the path changes too quickly for the filter. For example, if the adaptive filter is actually adding signal power instead of cancelling, the update control algorithms will reset the adaptive filter to cleared coefficients, forcing it to restart.

Speech Detection

The CS6420 detects speech by using power estimators to track deviations from a background noise power level. The power estimators filter and average the raw incoming samples from the ADC.

A background noise level is established by a register that increases 3 dB at intervals determined by NseRmp (Register 2, bits 7 and 6). When the power estimator level rises, the background noise level will slowly increase to try to match it. When the power estimator level is below the background noise level, the background noise level is quickly reset to match the power estimator level. This method allows significant flexibility in tracking the background noise level.

Speech is detected when the power estimator level rises above the background noise level by a given threshold. The half-duplex receive speech detector threshold is set by RHDet (Register 2, bits 11 and 10), the half-duplex transmit speech detector threshold is set by THDet (Register 3, bits 11 and 10), and the receive suppression speech detector threshold is set by RSThd (Register 2, bits 5 and 4). The transmit speech detectors for both half-duplex and suppression default to 5 dB.

Note that constant power signals which persist for long durations, such as tones from a signal generator, will be detected as speech only as long as the background noise level has not risen to within the speech detection threshold of the signal power. When a tone has persisted for long enough, the background noise level will be equal to the power estimator level, and so the tone will no longer be considered speech. This duration is dependent upon the power difference between the signal and the ambient noise power, as well as NseRmp. It should be noted that the CS6420 has a tone detector to prevent updates when tones are present and allow tones to persist regardless of the speech detectors.

Half-Duplex Mode

In cases where the system relies on the echo canceller for stability, a fail-safe mechanism must be in place for instances when the echo canceller is not

performing adequately. The CS6420 implements a half-duplex mode to guarantee communication even when the echo canceller is disabled.

When the CS6420 is first powered on, or emerges from a reset, the echo canceller coefficients are cleared, and the echo cancellers provide no benefit at this point. The half-duplex mode is on to prevent howling and echo from interfering with communication. Once the CS6420's adaptive filters have adapted sufficiently, the half-duplex mode is automatically disabled, and full-duplex communication can occur.

The half-duplex mode allows three states: transmit, receive, and idle. In the transmit state, the transmit channel is open and the receive channel is muted. The receive state mutes the transmit channel. The idle state is an internal state which is used to enhance switching decision making. The CS6420 must be idle before it will allow a state change between transmit and receive.

The half-duplex controller can be susceptible to echo, so a holdover timer is provided to help prevent false switching. Holdover will force the channel to remain in its current state for a fixed duration after speech has stopped. HDly (Register 2, bits 9 and 8) sets the duration of the holdover. Longer holdover will tend to make interrupting much harder, but will be much more robust to spurious switching caused by echo.

AGC

The CS6420 implements a peak-limiting AGC in both the transmit and receive directions in order to boost low-level signals without compromising performance when high amplitude signals are present. The technique effectively results in dynamic range compression.

The AGC works by setting a reference level based on the value represented by TVol (Register 1, bits 9-5) for the transmit direction and RVol (Register 0, bits 9-5) for the receive direction. If the signal from the input is above this reference, it is attenuated to the reference level with an attack time of 125 µs. This attenuation level decays with a time constant of 30 ms unless another signal greater than the reference level is detected. After the attenuation, a post-scaler scales the reference level to full-scale (the maximum digital code), which amplifies all signals by the difference between the reference level and full-scale.

For example, Figure 9 shows how the AGC works with a reference level of +30 dB (Word = 00000). Any signal greater than 30 dB below full-scale (a), is scaled down to 30 dB (b). This signal is then scaled up +30 dB (the reference level) to provide the final output (c). Note that the combination of attenuation and gain results in less than +30 dB total gain being applied. If the input signal is below 30 dB below full-scale (d), no attenuation is done and the full +30 dB of gain is applied to the signal (e).

When the reference level is set to +0 dB, the AGC is effectively disabled. Volume control is implemented by digital attenuation in 3 dB steps from this point on down. The maximum gain is +30 dB and the minimum is -60 dB in 3 dB steps. The lowest gain setting (11111) mutes the path. The signal scaling takes place in between the two cancellers, and so does not disturb the echo canceller as changing gain in the echo path would (see the *Adaptive Filter* section for more details).

Suppression

Echo cancellation is somewhat of a misnomer in that echo is merely attenuated, not entirely cancelled. Some residual echo still exists after the summing node. This residual echo, though very low, may be audible when the near-end talker is not speaking. Suppression further attenuates the echoed signal.

The CS6420 employs supplementary echo suppression which adds attenuation on top of the cancellation to remove the residual echo. For example, the

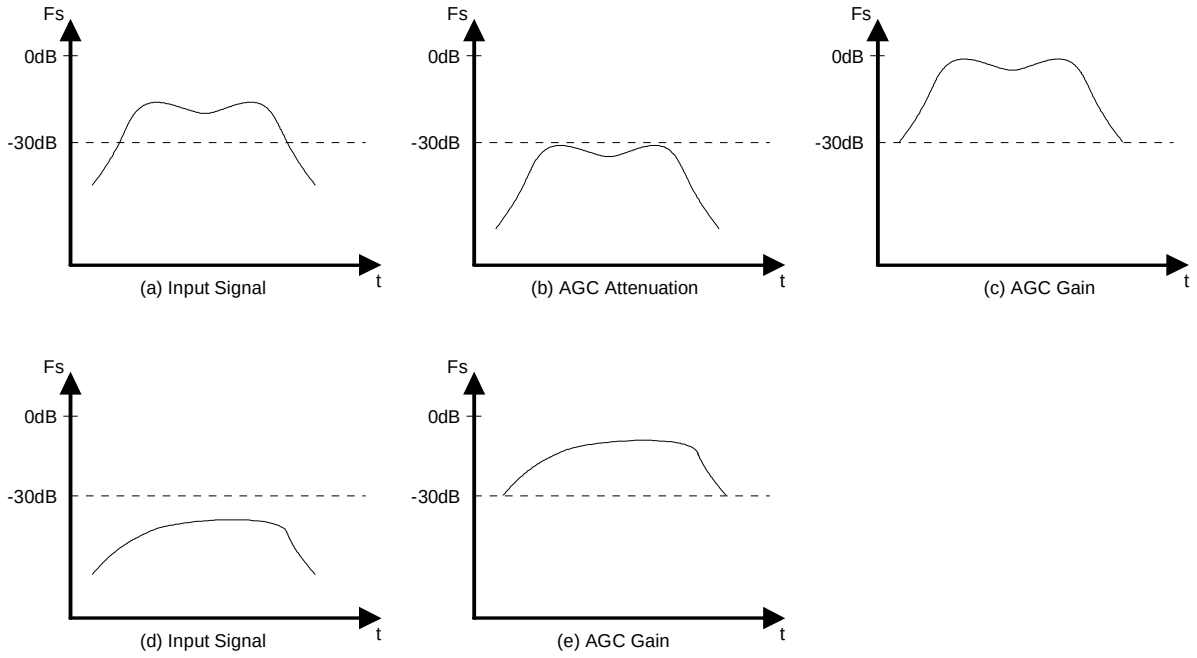


Figure 9. How AGC works (TVol = 00000)

transmit channel will engage extra attenuation whenever only the far-end talker is speaking. However, if the near-end talker starts speaking, the attenuation is removed and the system relies on the near-end talker's speech to mask residual echo.

Suppression causes some modulation of the perceived background noise which may be distracting to some users. As a result, it may be desirable to limit the suppression attenuation to the minimum necessary. The CS6420 provides TSAtt (Register 3, bits 9 and 8) to control the amount of attenuation introduced by suppression in the transmit channel. Receive suppression attenuates by 24 dB.

The suppression in the transmit suppression and that in the receive direction work very differently. The transmit suppression works in a "default off" mode while the receive suppression is "default on."

Transmit Suppression

The transmit suppressor attenuates the transmit path when only far-end speech is present, hence the name "default off." This ensures that the suppression engages only when necessary.

Recall that the purpose of Transmit Suppression is to mask residual echo by inserting additional loss/attenuation in the transmit path in the scenario when only far-end speech is present; the residual echo, if any, in double-talk being masked by near-end speech assuming reasonable levels of ERLE.

There are two controls/tweekable parameters for governing the behavior of Transmit Suppression. The two controls are adjustable through the Microcontroller Interface, and they are TSThd (Register 3, bits 5 and 4) and TSBias (Register 3, bits 7 and 6). TSThd is the primary control and should be adjusted before changing the value of TSBias from its default setting. TSThd sets the ERLE expectation to be used in discriminating between near-end speech and far-end echo. This control setting will by far predominate in affecting the manner in which Transmit Suppression behaves.

TSBias is a secondary control. This is to be adjusted after the system designer is more or less satisfied with the behavior of Transmit Suppression with the TSThd set. It affects the ease with which a near-end talker may disengage Transmit Suppression and

keep it disengaged. We recommend using larger values of TSBias relative to TSThd settings in order to facilitate ease of near-end speech transmission. For example, the default setting for TSThd is 15 dB and 18 dB for TSBias.

In some scenarios, especially when the dynamic range of volume control is significantly large, we also recommend the use of different combinations of TSThd and TSBias setting relative to output volume of the acoustic interface.

Receive Suppression

The "default on" receive suppressor is nominally attenuating unless far-end speech is present. This behavior is more consistent with behavior observed in modern speakerphones, and helps keep noise levels low.

One side effect of this scheme is that a constant power signal, such as noise from a noise generator or a tone, will eventually be attenuated when the background noise level estimate turns off the receive suppression speech detector. See the section on *Speech Detection* from more details.

RSThd (Register 2, bits 5 and 4) sets the speech detection threshold of the suppressor's speech detector. See the *Speech Detection* section for more details.

Circuit Design

The design of the CS6420 interface circuitry plays an important role in achieving optimum performance. The actual circuit design is important, especially the analog interface. Proper grounding and layout will help minimize the noise that might get coupled into the CS6420.

Interface Considerations

Of the CS6420 interfaces, the analog interface and the microcontroller interface are the most important to pay special attention to during circuit design. The analog interface especially will determine how well the echo canceller can perform.

Analog Interface

The Analog Interface feeds information about the echo path to the adaptive filter, so it is critical that this interface be well designed. Using high-quality transducers and circuits that guarantee low-distortion and minimal clipping are essential to the success of any echo canceller based design.

As mentioned in the *Adaptive Filter* section, the adaptive filter assumes that the echo path is linear and time-invariant. As such, poor quality speakers are a common cause of poor echo canceller performance due to their high distortion. Speakers must be selected with their linearity in mind. In general, the speaker should have less than 2% Total Harmonic Distortion. This will result in distortion terms 34 dB below the desired signal, enough headroom for the echo canceller to function adequately.

The other major consideration in the design of the analog interface is that the circuitry that processes the transducer signals not clip or distort it. For example, a common problem is the use of a speaker amplifier with a fixed gain, which clips when driving the speaker. Although the distortion may not be objectionable to the human ear, it will prevent the adaptive filter from modeling the path correctly. That which worked for half-duplex speakerphones will not necessarily work for full-duplex speakerphones. Microphone amplifier circuitry is also suspect when looking for sources of clipping and distortion.

Microcontroller Interface

The Microcontroller Interface is the only asynchronous digital connection to the CS6420, so it is the most likely place for digital noise coupling to be a problem. The interface itself is fairly straightforward and requires only three pins from a microcontroller.

The three pins that comprise the Microcontroller Interface are STROBE, DATA, and $\overline{\text{DRDY}}$. STROBE must not exceed the system clock of the CS6420 in speed. Also, four extra clocks are required after $\overline{\text{DRDY}}$ is brought high in order to latch the data into the CS6420, as is shown in Figure 5.

Grounding Considerations

Proper grounding of the CS6420 is necessary for optimal performance from this mixed-signal device. The CS6420 should be considered an analog device for grounding purposes.

The digital sections of the CS6420 are synchronized with its ADCs and DACs to minimize the effects of digital noise coupling. However, for external digital devices that are asynchronous with respect to the CS6420, precautions should be taken to minimize the chances of digital noise coupling into the CS6420.

A design with the CS6420 should have a separate ground plane for any digital devices. For example, a system microcontroller should be on a digital ground plane with its control lines leading to the CS6420 in the shortest reasonable distance. The CS6420 itself should lie completely on the analog ground plane.

Layout Considerations

The physical layout of the traces and components around the CS6420 will also strongly affect the performance of the device. Special attention must be paid to decoupling capacitors, the crystal oscillator, and the input anti-aliasing filters.

The decoupling capacitors for the power supplies of the CS6420 should be placed as close as possible to the power pins for best performance. There are two capacitors per pin: the 0.1 µF capacitor needs to be closest to the pin to decouple the high frequency components, and the larger cap can be farther away. The MB pin is the most critical as it connects directly to the on-chip voltage reference. AVDD and DVDD are secondary to MB with respect to priority.

The crystal oscillator should be placed as close as possible to reduce the distance that the high frequency signals must travel. If the crystal is placed too far away, the trace inductance may cause problems with oscillator startup.

The next concern with placement is the input anti-aliasing filters for the ADC inputs. NI has an RC low-pass network with a corner frequency of 8 kHz. The capacitor of this low-pass network should be placed very close to the pin so that there is very little exposed trace to pick up noise. If the on-chip microphone amplifier is used, the 0.022 µF capacitor on APO will provide the appropriate cutoff frequency, and so should be placed close to the APO pin. If the on-board preamplifier is not used, APO will have the same RC network as NI, and should be treated similarly.

The connections from the controller to the Microcontroller Interface should be short straight traces, if possible. The traces should not run very close to any digital clocks to avoid cross coupling.

System Design

The CS6420 is ultimately only one part of a bigger full-duplex hands-free system. In order for that system to work well, it needs to be properly balanced. The distribution of the system gains will make or break the echo canceller. In order to judge performance, however, the system integrator must be armed with the means to test the product.

Gain Structure

The distribution of the system gains is an important design consideration to keep in mind. Gain distribution is an intricate balancing act where the system integrator tries to maximize dynamic range while minimizing noise, and at the same time, getting excellent echo canceller performance.

The basic constraint on getting good echo canceller performance is that the maximum output should not clip when coupled to the input. For example, if in a speakerphone, AO provides 1 V_{rms} to a speaker, the reflections reaching the microphone should present no more than 1 V_{rms} to the Acoustic ADC. In fact, it is advisable to allow 6 dB or even 12 dB of margin, such that in the above example, the signal present at the Acoustic ADC is 250 mV_{rms}.

After this coupling level is established, the desired signal gain must be established. To continue from the previous example, the transmit gain must be adjusted to make sure the near-end talker is easy to hear at the far-end. If the signal from the near-end talker clips at the ADC, it is not significant to the echo path because the AEC should not be updating anyway.

In general, to minimize noise, system gain should be concentrated before the ADC. However, this is not practical in all cases, mostly because of the coupling constraint. The CS6420 offers the AGC'd gains provided by TVol and RVol to help provide the desired gain.

The CS6420 offers two different programmable gain sources: TGain/RGain and TVol/RVol. TGain and RGain switch in different size sampling capacitors at the ADC to provide a choice of 0 dB, 6 dB, 9.5 dB, and 12 dB of analog gain. TVol and RVol introduce digital gain and attenuation in 3 dB steps. The difference is significant in that the digital gain will gain up the noise of the ADC as well as the desired signal, whereas the analog gain will not.

Testing Issues

The following tests are suggestions for measuring echo canceller and half-duplex performance.

ERLE

Echo Return-Loss Enhancement (ERLE) is a measure of the attenuation that an echo canceller provides. The number is an expression of the ratio of the level of signal without the echo canceller compared to the level of signal with the echo canceller.

When measuring ERLE, it is important that any potential acoustic loops be broken; so to measure the ERLE of the Acoustic Canceller, the NO output should be disconnected from the rest of the network. This will prevent feedback which could occur when all of the CS6420's failsafes are disabled.

The following example outlines the steps necessary to measure the ERLE of the acoustic echo canceller.

It is important to choose a good test signal for the tests to be valid. As mentioned in the *Adaptive Filter* section, the CS6420 does not work optimally with white noise. The best signal to use would be a repeatable speech signal, like a recording of someone counting or saying "ah."

Use the Microcontroller Interface to disable transmit and receive suppression as well as half-duplex. Allocate all the taps to the Acoustic Canceller in order to allow full-duplex without the Network Canceller being trained. The gains should be set appropriate for good system performance.

The first measurement is a baseline figure of performance with no echo canceller. Use the Microcontroller Interface to clear the acoustic canceller coefficients. Inject the test signal at NI and measure the rms voltage at NO. This measurement gives the baseline coupling level (denominator).

Use the Microcontroller Interface to set the acoustic canceller coefficients to normal which will allow the adaptive filter to adapt. Inject the test signal at NI and allow a few seconds for the filter to adapt. Measure the rms voltage at NO. This measurement gives the cancelled echo level (numerator).

Convert both voltages to decibels and subtract the echo cancelled level from the baseline level to calculate the ERLE. At the factory, with known good components, we typically see 30 dB of ERLE with speech.

Convergence Time

Convergence time is a measure of how quickly the adaptive filter can model the echo path. From cleared coefficients, the training signal is injected into the echo canceller and the time for the ERLE to reach a given threshold value is the convergence time. Different customers will have different threshold levels, so Crystal does not specify convergence time.

The following example will measure convergence time for the acoustic echo canceller:

Set up the system as for the ERLE test. Clear the acoustic canceller coefficients through the Microcontroller Interface. Apply the training signal to NI, set the coefficients to normal, and simultaneously start a timer. Once the measured ERLE reaches the threshold the system designer desires, stop the timer. The elapsed time is the convergence time. A good value for the threshold would be the AErle value from Register 3, since this would be the time for the CS6420 to go from half-duplex mode to full-duplex mode.

A good tool for this measurement is a digital storage oscilloscope set to a slow sweep so that about five seconds of signal is shown on the screen. One channel of the oscilloscope should monitor the ADC input (for an uncancelled reference), and another channel should monitor the echo cancelled output. This technique is especially effective when speech is the training signal.

We see about 2-5 seconds of training time using known good equipment. This time assumes continuous speech as the training signal. Pauses will extend the convergence time.

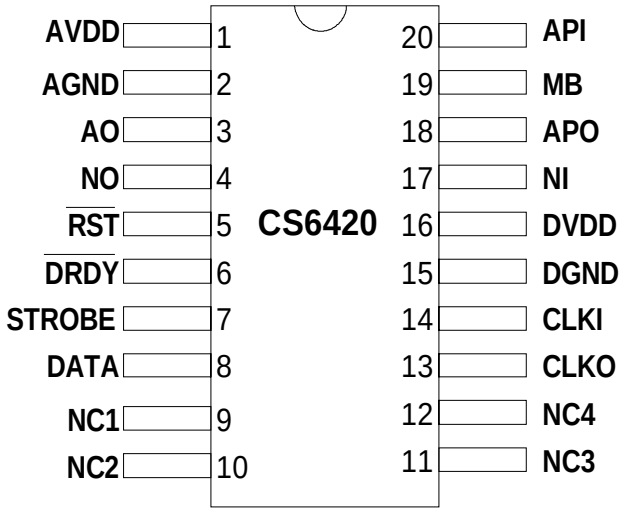
Half-Duplex Switching

Although the CS6420 transitions from half-duplex operation from reset after only a few utterances are passed through the system, the performance of the half-duplex is critical to the end-user in cases where the echo canceller is not adequate. The half-duplex switching characteristics can be subjectively tested with the following procedure:

Set the CS6420 Microcontroller Interface to the nominal register values for the system, but clear the acoustic and network echo canceller coefficients. This will force the CS6420 to remain in half-duplex mode.

The most useful test of practical performance found at Crystal has been the “alternating counting test.” In this test the person at the near-end counts all the odd numbers and the person at the far-end counts all the even numbers. This tests the interruptibility of the half-duplexer. During testing, system parameters for the half-duplex may need to be changed to accommodate the level of performance expected for the product. See the *Half-Duplex* and *Register Definitions* sections for more details.

PIN DESCRIPTIONS



Analog Interface

AO - Acoustic Interface Output, Pin 3

Analog voltage output for the acoustic side (near-end output/receive output). Maximum output signal is 1 V_{rms} (2.8 V_{pp}). This output can drive down to 10 kΩ and is usually followed by a speaker driver. The output is pre-compensated to expect a single-pole RC low pass filter with a corner frequency of 4 kHz.

NO - Network Interface Output, Pin 4

Analog voltage output for the network side (far-end output/transmit output). Maximum output signal is 1 V_{rms} (2.8 V_{pp}). This output can drive down to 10 kΩ. The output is pre-compensated to expect a single-pole RC low pass filter with a corner frequency of 4 kHz.

API - Acoustic Interface Preamplifier Input, Pin 20

Input to the acoustic side microphone preamplifier. Signal source resistance at this pin will reduce the 34 dB gain inherent in the preamplifier. The maximum signal without clipping is 20 mV_{rms} (57 mV_{pp}), assuming default settings.

APO - Acoustic Interface Preamplifier Output, Pin 18

Output of the acoustic side microphone preamplifier and input to the acoustic side analog-to-digital converter (near-end input/transmit input). This input expects a single-pole RC anti-aliasing filter with a corner frequency of 8 kHz. Maximum signal level before clipping at this point is 1 V_{rms} (2.8 V_{pp}), assuming default settings for the Tx Analog Gain.

MB - Microphone Bias Voltage Output, Pin 19

Output of 3.5 VDC provides the internal voltage reference for the CS6420. MB must be decoupled with a 10 µF and 0.1 µF capacitor to prevent noise from affecting the on-chip voltage reference. MB must not be connected to any load.

NI - Network Interface Input, Pin 17

Input to the network side analog-to-digital converter (far-end input/receive input). This input expects a single-pole RC anti-aliasing filter with a corner frequency of 8 kHz. Maximum signal level before clipping at this point is 1 V_{rms} (2.8 V_{pp}), assuming default settings for the Rx Analog Gain.

Microcontroller Interface

$\overline{\text{RST}}$ - Active Low Reset Input, Pin 5

When $\overline{\text{RST}}$ is held low, the CS6420 is put into a low power mode with all functional blocks idle. When $\overline{\text{RST}}$ goes high, the CS6420 is started in a known state.

$\overline{\text{DRDY}}$ - Active Low Microcontroller Interface Data Ready Input, Pin 6

$\overline{\text{DRDY}}$ is a low pulse used to gate valid input data into the Microcontroller Interface.

STROBE - Microcontroller Interface Clock Input, Pin 7

The rising edge of STROBE latches DATA into the Microcontroller Interface while $\overline{\text{DRDY}}$ is low.

DATA - Microcontroller Interface Data Input, Pin 8

DATA is latched into the Microcontroller Interface on the rising edge of STROBE.

Clock

CLKI - Clock Oscillator Input, Pin 14

A 20.480 MHz parallel-resonant crystal should be connected between CLKI and CLKO. Alternatively, CLKI may be driven directly with an 20.480 MHz CMOS level clock.

CLKO - Clock Oscillator Output, Pin 13

A 20.480 MHz parallel-resonant crystal should be connected between CLKI and CLKO. Must be floating if CLKI is driven directly with a CMOS level clock.

Power Supply

AVDD - Analog Supply, Pin 1

+5 Volt analog power supply.

AGND - Analog Ground, Pin 2

Analog ground reference.

DVDD - Digital Supply, Pin 16

+5 Volt digital power supply.

DGND - Digital Ground, Pin 15

Digital ground reference.

Miscellaneous

NC1 - No Connect, Pin 9

Must be floating for normal operation.

NC2 - No Connect, Pin 10

Must be floating for normal operation.

NC3 - No Connect, Pin 11

Must be floating for normal operation.

NC4 - No Connect, Pin 12

Must be floating for normal operation.

GLOSSARY

Echo

A signal that returns to its source after some delay.

Network Echo

Echo resulting from signal reflection due to an impedance mismatch in a 2-to-4 wire converter (hybrid).

Acoustic Echo

Echo created by signal propagation in a room from a speaker to a microphone.

Reverberation

Local information that bounces around the room before it reaches the microphone. An example of reverberation is when your back is to the speakerphone, and your voice bounces off the wall before it reaches the microphone.

Near-End

The location with the acoustic interface (speaker and microphone).

Far-End

The location connected to the network interface.

Transmit Path

The signal path from Near-End input to Far-End output.

Receive Path

The signal path from Far-End input to Near-End output.

Full-Duplex

The state when both Transmit and Receive paths are simultaneously active.

Half-Duplex

The state when either Transmit or Receive path is active.

Supplementary Echo Suppression

Dynamic attenuation placed in the opposite path of the active path to mask residual echo. For example, if the receive path is active, the transmit path is attenuated. When both paths are simultaneously active, the suppression attenuation is removed. See the section on *Suppression* in *Design Considerations* for more details.

Howling

In full-duplex operation, both the microphone and speaker are active at the same time, which, in conjunction with the reflection off the hybrid, creates a closed loop. The signal coupling between the speaker and the microphone can cause feedback oscillation or howling. This happens when the coupling between the speaker and microphone is strong enough to increase the system's closed loop gain above unity.

Acoustic Coupling

The strength of the output signal from the speaker that is received at the microphone input.

Adaptive Filter

A digital FIR filter that adjusts its coefficients to match a transfer function, such as the echo path between the speaker and microphone. The adaptive filter is able to compensate for different and changing conditions, such as someone moving in the room.

Echo Path

The acoustic echo path describes the acoustic coupling between the speaker and the microphone. It describes both the magnitude and delay characteristics of the echoed signal. It is affected by the speaker, microphone, phone housing, room, objects in the room, movement, and the talker. The network echo path is comprised of the transfer function between NO and NI.

Path Change

A change in the transfer function that describes the Echo Path. Changes in the acoustic echo path are most commonly due to motion in the room or gain changes at an external speaker. Network echo path is most easily changed by picking up an extension or hanging up the phone.

AGC

The CS6420 implements a peak-limiting Automatic Gain Control to allow a greater dynamic range without clipping the signal. See the section on *AGC* in the *Design Considerations* section for details on how it works.

Doubletalk

The condition occurring when both Near End and Far End talkers are speaking simultaneously.

ERLE

Echo Return-Loss Enhancement is the amount of attenuation of echo signal an echo canceller provides (not counting Suppression) as measured in dB. ERLE is a measure of the echo canceller's performance. The larger the value for ERLE, the better the echo cancellation.

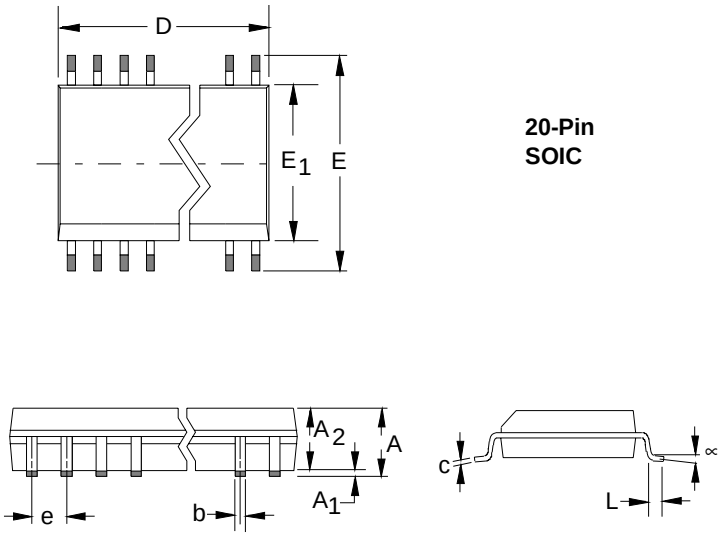
Coverage Time

The CS6420 echo canceller has 508 taps and it can sample an analog signal at an 8 kHz rate. 512 x 1/8kHz = 63.5 ms. Sound travels through air at a rate of around 1 ft/ms. Thus the echo canceller can be used in a room with walls 32 feet away, discounting multiple reflections. But remember that at this distance, most of the echo has been attenuated due to the physical separation. The majority of the acoustic coupling comes from the first arrival, or directly from the speaker to the microphone. The first signal is by far the strongest.

Convergence Time

A high quality echo canceller is continuously modifying its internal model of the echo path characteristics (See Adaptive Filter). When the model is complete, the echo canceller will be able to cancel echo to the extent of its rated capabilities. Convergence time is the duration it takes the echo canceller to train itself, from cleared coefficients, and switch to full-duplex operation, in the presence of speech.

PACKAGE DIMENSIONS



20-Pin SOIC

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.41	2.54	2.67	0.095	0.100	0.105
A_1	0.127	-	0.300	0.005	-	0.012
A_2	2.29	2.41	2.54	0.090	0.095	0.100
b	0.33	0.46	0.51	0.013	0.018	0.020
c	0.203	0.280	0.381	0.008	0.011	0.015
D	12.45	12.70	12.95	0.490	0.500	0.510
E	10.11	10.41	10.67	0.398	0.410	0.420
E_1	7.42	7.49	7.57	0.292	0.295	0.298
e	1.14	1.27	1.40	0.040	0.050	0.055
L	0.41	-	0.89	0.016	-	0.035
∝	0°	-	8°	0°	-	8°

• Notes •

A DIVISION OF CIRRUS LOGIC

CDB6420

CS6420 Evaluation Board

Features

- Small size of important board components eases system integration
- Speaker driver included
- Microphone bias circuitry provided
- Easy connection to PC Parallel Port
- Windows-based control software included
- Analog and Digital Patch Area
- Includes Evaluation Board, 3 1/2" Software Diskette, and 25-Pin D Connection Cable.

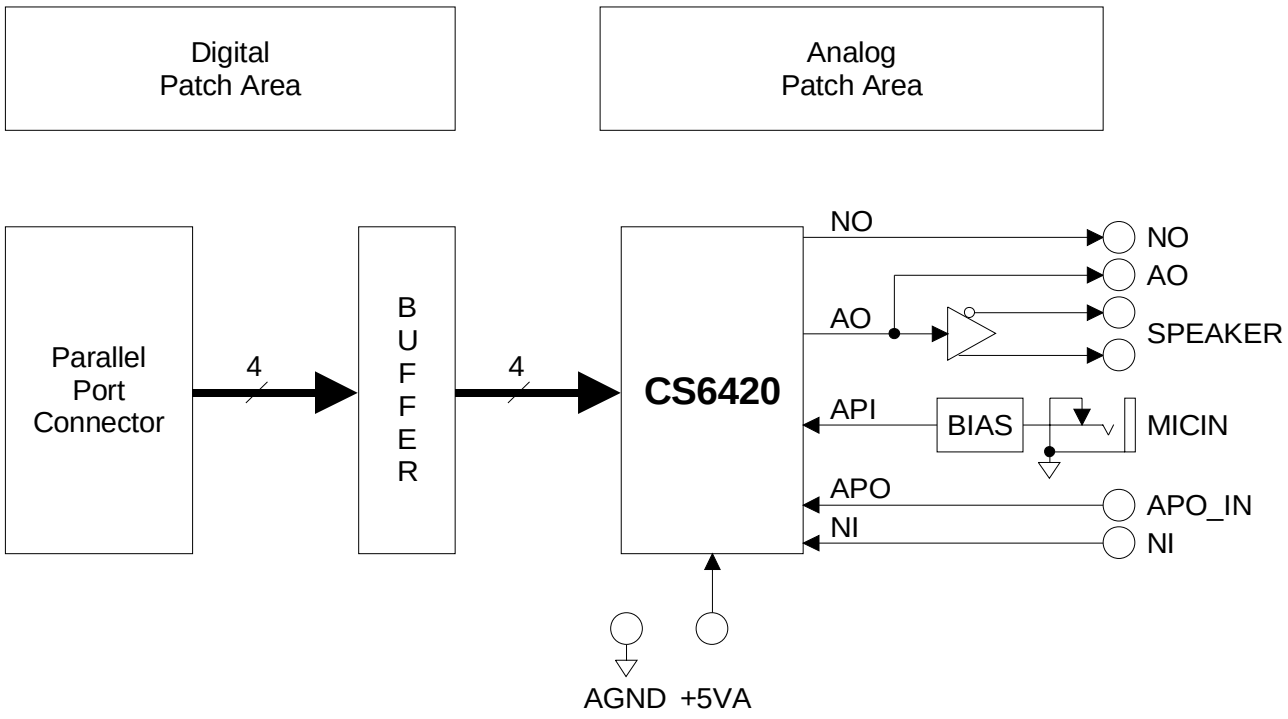
Description

The CDB6420 allows an end-user to quickly and easily integrate the CS6420 Full-Duplex Speakerphone IC into a system and evaluate its performance. The board comes with software which allows the registers of the CS6420 to be manipulated from a personal computer running Windows. Evaluation requires a +5 V power supply. Connections for analog audio sources are provided on the board.

The CDB6420 includes a business card-sized section which contains the CS6420 and all the elements necessary to provide a speakerphone interface. This section is available for direct insertion into a target system, if the target system can provide the signals required by the CS6420 Network Interface.

ORDERING INFORMATION

CDB6420	Evaluation Board



Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (AVDD, DVDD)	+5VA	4.5	5.0	5.5	V
Ambient Operating Temperature	T_{AOp}	0	25	70	°C
Maximum Analog Input Level (APO, NI) Note 1	V_{in}		2.8		V_{pp}
Maximum Analog Output Level (AO, NO)	V_{out}		2.8		V_{pp}
Input and Output Offset Voltage	V_{off}		2.12		VDC
Maximum Speaker Output Voltage	V_{spkr}		6.4		V_{pp}

1. Assumes TGain=RGain= 0 dB.

HARDWARE

Power Supplies

The CDB6420 power supply circuitry is shown in Figure 1. The evaluation board expects a clean +5V DC power supply to be applied to the +5VA binding post. This powers the analog components of the evaluation board. Power for the digital components is derived through a ferrite bead to filter out the high frequency components.

Analog Signal Connections

Figure 2 shows the RCA connectors for the analog signals. These RCA connectors connect directly to the test points with the same names. All the connectors have a nominal maximum input and output voltage of 2.8 V_{pp}. NO and AO present 12 kΩ of output impedance at the connector and have a low-pass corner at 4 kHz. APO_IN and NI both have input anti-aliasing filters with corners at 8 kHz, and an nominal input impedance of 6 kΩ.

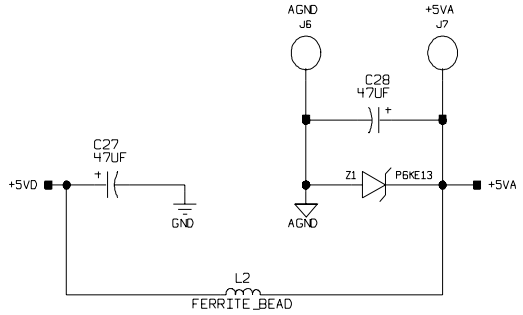


Figure 1. Power Supply

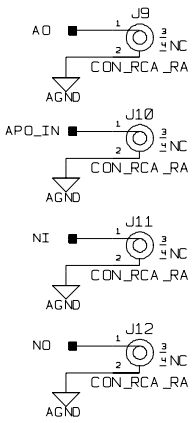


Figure 2. RCA Connections

Microphone Bias

A constant current source providing the necessary bias for electret microphones is shown in Figure 3. A 1/8" stereo microphone jack (J8) is provided for easy connection to microphones with 1/8" plugs. HDR3 provides an easy way to connect a microphone with bare wires. The stereo microphone jack is self-shorting, so when connecting to the test point MICIN or HDR4, make sure that either a plug is in the jack, or the trace from the jack has been cut (HDR4 is a convenient place to do this).

Speaker Driver

A speaker driver circuit, implemented with a Motorola MC34119, is shown in Figure 4. This circuit provides 6.4 V_{pp} differentially to the SPEAKER terminals (J1 and J2). This circuit can drive down to an 8 Ω load. When using the speaker driver, the speaker driver must be connected to AO by HDR3. This will connect the speaker driver to AO, but in doing so will create a voltage divider at the AO test point resulting in a 1.4 V_{pp} full-scale swing at the AO test point and connector. The CDB6420 is shipped with the speaker driver enabled by default.

In order to disable the speaker driver, remove the jumper shorting HDR3. This will result in the connection between AO and the speaker driver input being broken and allowing the signal at the AO test point and connector to swing to its full extreme of 2.8 V_{pp} full-scale.

CS6420

The heart of the CDB6420, the CS6420 Full-Duplex Speakerphone Chip, is shown in Figure 5. The outputs AO and NO are shown with the output low-pass filters that remove the high frequency components from the delta-sigma DACs. The inputs APO_IN and NI are shown with the anti-aliasing network they require.

When using APO as the input, the CS6420 does not use the on-chip 34 dB preamplifier. HDR1 must be changed to the PREAMP OFF (1-2) position when

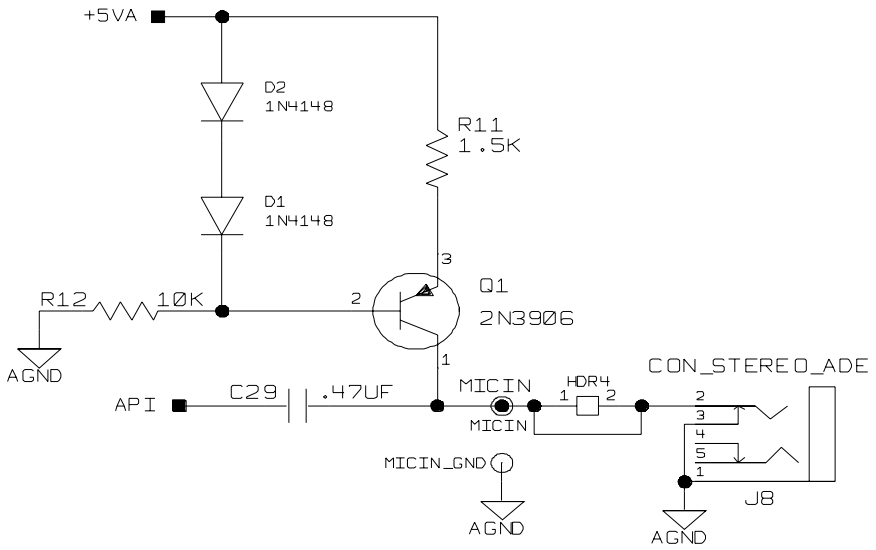


Figure 3. Microphone Input Circuit

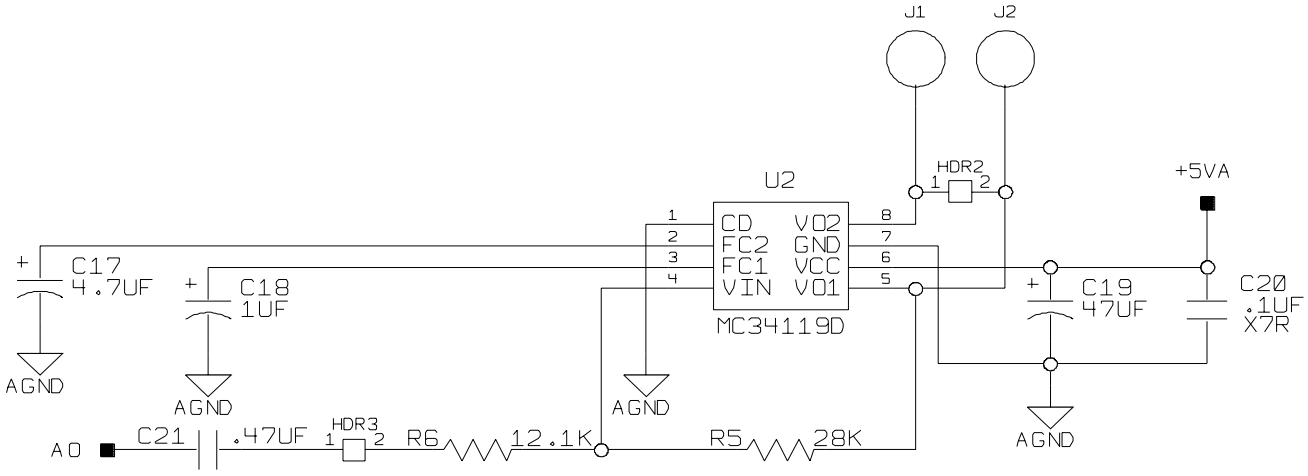


Figure 4. Speaker Output Circuit

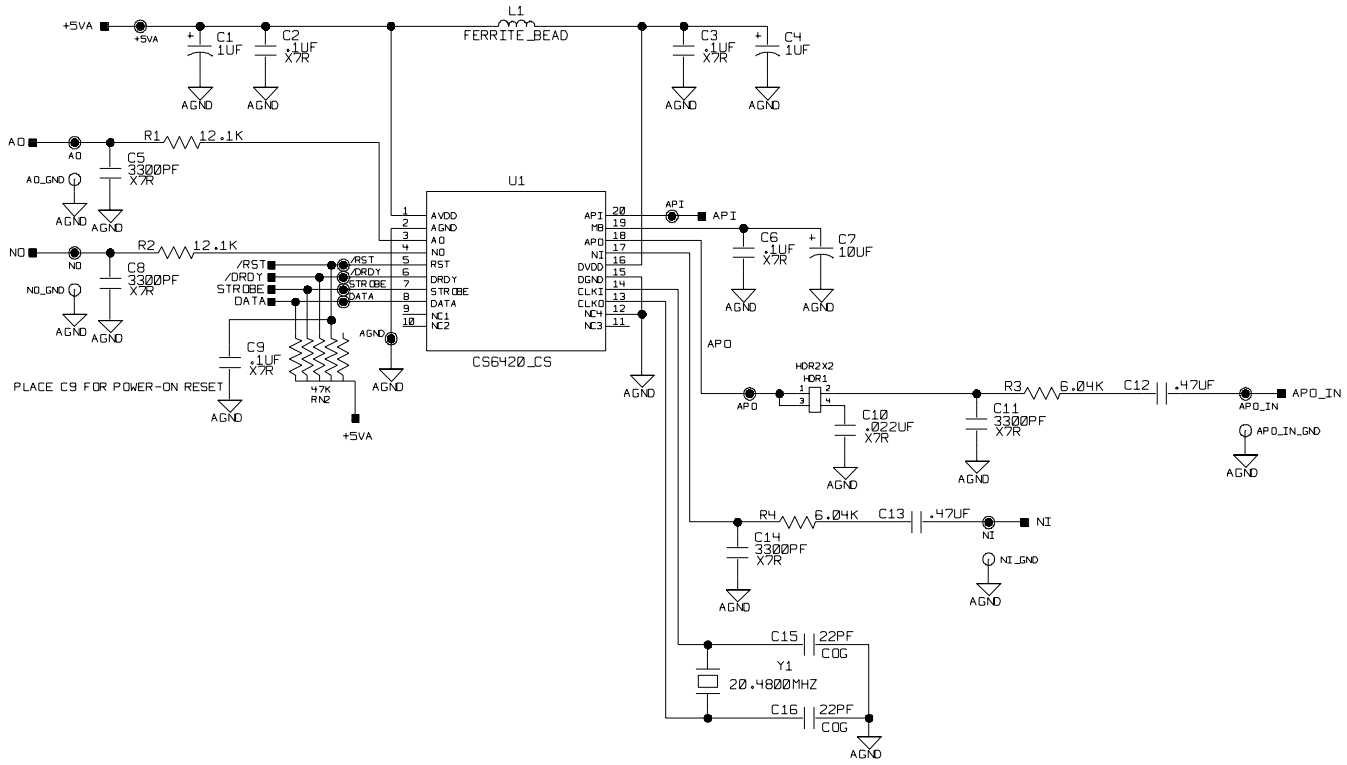


Figure 5. CS6420 Connection Diagram

using APO_IN as an input. This connects the signal path appropriately. The control bit in the software (Mic) must be set to APO as well. When using MICIN as the acoustic side input source, HDR1 must be in the PREAMP ON (3-4) position, and the Mic bit in the software should be set to API.

The test loops labeled API and APO are provided to allow easy probing of the pins of the same name. The maximum signal present at APO should be 2.8 V_{pp} with TGain (see the *Software* section) set to 0 dB.

Parallel Port Interface

Figure 6 shows the parallel port interface of the CDB6420 that connects to a PC's parallel port. The 74HCT541 buffer serves to protect the CS6420 from any damaging surges. The buffer is socketed for easy replacement. Four of the parallel port data lines are used to control the microcontroller interface pins of the CS6420. The RC network serves to minimize the ringing common to HCT devices. Test loops are provided for easy oscilloscope access.

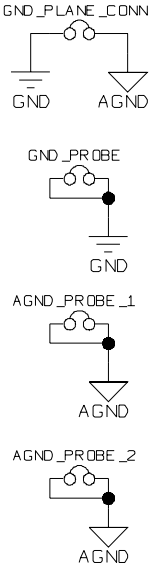


Figure 7. Grounds

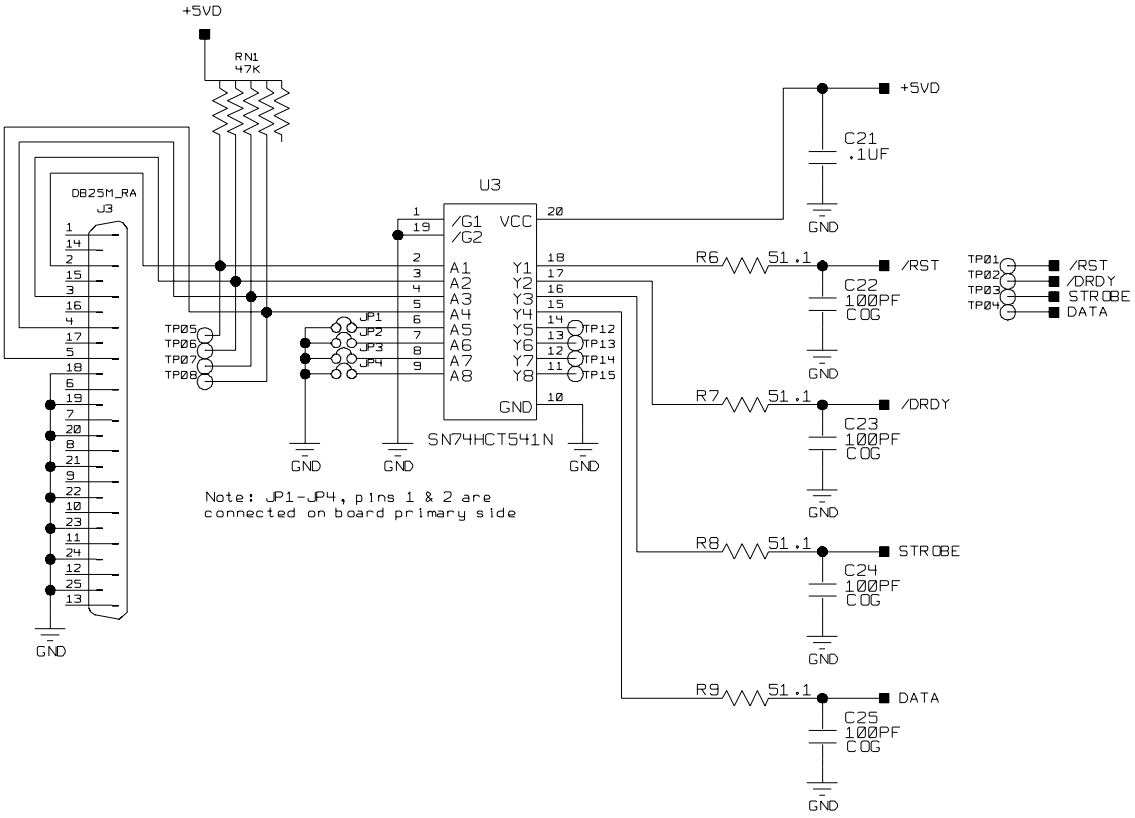


Figure 6. Parallel Port

SOFTWARE

Requirements

Windows 3.1 or better
available LPT port
100KB Hard Disk space

Selecting an LPT Address

When starting the program for the first time, an LPT address must be specified to communicate with the CDB6420. This address is usually available from the BIOS information displayed at system boot or from the PC's CMOS setup program. This address is necessary for the CDB6420 program to manipulate the registers on the board.

Select the LPT address by choosing the appropriate address in the "Control | LPT Address..." menuitem. A good way to tell if you have selected the correct address is to change the Reset Option to Powerdown (see the Reset Options section), and press the Current Reset Option button. If you have an ammeter on the power supply to the CDB6420, you will see a dramatic decrease in current consumption. Alternatively, you can probe the $\overline{\text{RST}}$ line and you should see it go low when you press the button.

Reset Options

A dialog box which supports the various CS6420 reset options is shown in Figure 8. This dialog box is invoked by selecting the menuitem "Control | Reset Options...".

The "Exit Timer" edit box allows the system integrator to test the effects of an early exit from reset. An integer from 0 to 100 may be entered here to specify how long after $\overline{\text{RST}}$ goes high the control word to terminate the reset timer early will be sent. See the CS6420 datasheet for more details.

The CS6420 is capable of either a cold reset or a warm reset. A cold reset resets all registers and

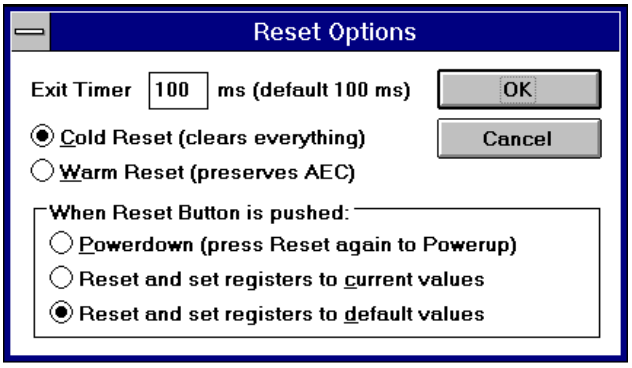


Figure 8. Reset Options

variables to their default values. A warm reset saves certain key variables to allow the CS6420 to adapt to the echo path more quickly.

The function of the reset button in the main window are controlled by the radio buttons in the group "When Reset Button is pushed:". The first option will force the CS6420 into a low power mode by holding $\overline{RST}$ low until the button is pushed again (the text on the button will change to reflect this). The second option will send the current settings of the four registers to the CS6420 immediately after performing the reset. The last option will restore the default values of the registers to the CS6420, which is the mode selected when the program is initially started. Note that this option also changes the register settings in the main window. Also note that once this type of reset is invoked, the reset type will automatically be changed to restore current register values.

Main Window

Figure 9 shows the main window of the CDB6420 Control Program. The main window is a block diagram representation of the internals of the CS6420 with all the registers placed in their appropriate locations in the signal flow. The right side of the screen is the Near End (or Acoustic Interface), and the left side is the Far End (or Network Interface. See figure 9). The upper path is the Receive Path, and the lower path is the Transmit Path. The hexadecimal values of the registers given the current settings of the controls is given in the lower left corner. These values are sent to the CS6420 over the microcontroller interface.

The Controls

There are 27 controls in the CDB6420 Control Program main window. These controls map to the four registers in the CS6420 whose register values can be seen in hexadecimal format in the lower left of the main window. The controls can be easily navigated by using the "Tab" key to traverse the controls from left to right, and "Shift-Tab" to reverse the direction. Furthermore, the four most commonly used controls have hotkeys which will take you to them: RVol (Ctrl+1), TVol (Ctrl+2), NCC (Ctrl+3), and ACC (Ctrl+4). These are also accessible from the “Control” menu.

Drop-down Box Hints

Once familiar with the values in the drop-down boxes, one can easily choose specific values by typing the first letter of the selection, or using the up and down arrow keys. Typing the first letter of the selection can help avoid lots of scrolling and unnecessary writes to the microcontroller interface. For example, if RVol is currently selected, its value can be changed to 30 dB by pressing 3 once and to 3 dB by pressing it again. 0 dB is selected by pressing 0, and pressing "m" will select mute. Alternatively, if the value is 0 dB, pressing the down arrow will set the register to -3 dB, and pressing the up arrow will set the value to 3 dB.

As another example, when manipulating the Acoustic Coefficient Controls (ACC) drop-down box, the desired setting of the three available selections ("Normal", "Clear", and "Freeze") can be chosen with the keys "n", "c", and "f". If using the arrow keys, going to Freeze from Normal would always result in a Clear, which may not be desired, so pressing "f" would be preferable. You can always use the mouse to select the value.

Button Hints

The four checkboxes (RSD, HHold, HD, and TSD) can be toggled by pressing the spacebar when the checkbox is selected. The radio button for Mic (choosing between API and APO for the ADC input source) is changed by using the up or down arrow. The Reset Button (at the bottom of the main window) can be pressed when selected by pressing the spacebar, or at anytime by pressing the enter key. As above, you can always use the mouse to select the value.

Controls in Detail

The controls are discussed in detail below. Each description has the register name, the available choices, and the consequence of each choice summarized. The following descriptions are only meant as a supplement to the CS6420 datasheet. Please carefully read the Register section of that document for full details.

RGain - Receive ADC Analog Gain

0 dB, 6 dB, 9.5 dB, 12 dB:
set gain of the ADC at NI

RSD - Receive Suppression Disable

checked: disable receive suppression
unchecked: enable receive suppression

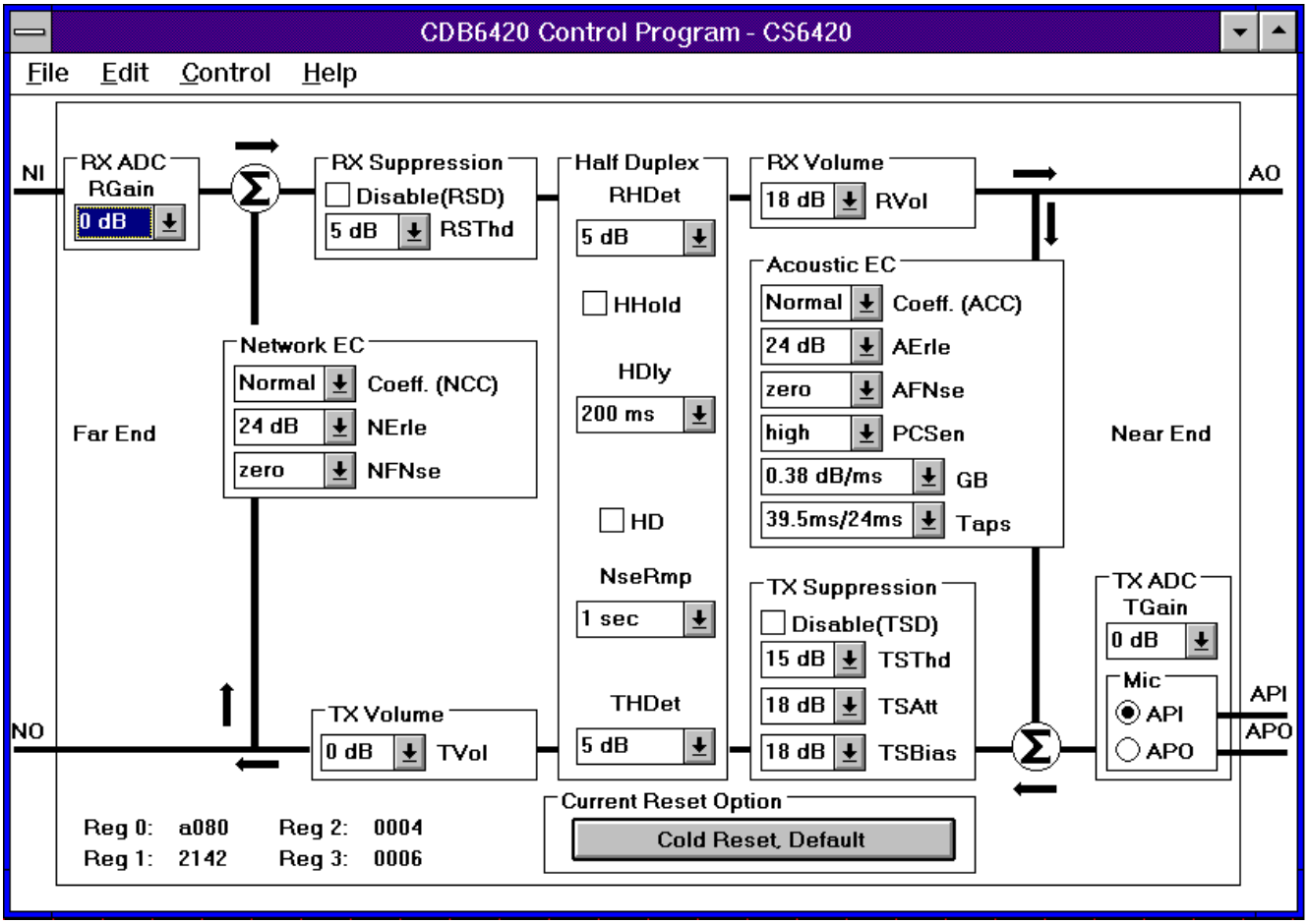


Figure 9. Main Control Panel

RSThd - Receive Suppression speech-detection Threshold

5 dB: default

3 dB: make disengaging receive suppression easier (sensitive to bursty far end noise)

6 dB: make receive suppression harder to disengage (less sensitive to far end noise).

NCC - Network (echo canceller) Coefficient Control

Normal: coefficients adapt to echo path

Clear: coefficients held to zero (no cancellation)

Freeze: coefficients held to current values and adaptation halted

NErle - Network ERLE threshold

24 dB: default

18 dB: network echo canceller tends to go to full-duplex more easily (faster)

30 dB: network echo canceller requires good performance to go to full-duplex (slower)

NFNse - Network Full-duplex Noise threshold

zero: use NErle as sole criterion to transition to full-duplex.

-42 dB: echo path may not exist, so go to full-duplex when noise level is below -42 dB (easy) and internal determination of path/no path is complete

-54 dB: echo path may not exist, so go to full-duplex when noise level is below -54 dB (hard) and internal determination of path/no path is complete

TVol - Transmit Volume

30 dB, 27 dB, ... , -57 dB, -60 dB, mute:

digital volume control, positive numbers are AGC'd.

RHDet - Receive Half-duplex Detect threshold

5 dB: default

3 dB: half-duplex detects far end speech more easily (more sensitive to far end noise)

6 dB: half-duplex less sensitive to far end speech (less sensitive to far end noise)

HHold - Half-duplex Hold on howl

checked: after howl, CS6420 remains in half-duplex

unchecked: after howl, CS6420 readapts

HDly - Half-duplex holdover Delay

200 ms: default

100 ms: very easy to break in, but may falsely switch

150 ms: somewhat easy to break in, but may falsely switch

HD - Half-duplex Disable

checked: CS6420 will never be in half-duplex.

unchecked: CS6420 can be in half-duplex as needed.

NseRmp - Noise estimator Ramp rate

1 sec: noise estimator increases noise level by 3 dB/ 1 sec

0.5 sec: estimated noise level increases by 3 dB/ 0.5 sec (improves tracking of dynamic noise levels)

2 sec: estimated noise level increases by 3 dB/ 2 sec (improves detection of long bursts of speech)

THDet - Transmit Half-duplex Detect threshold

5 dB: default

3 dB: half-duplex tends to detect transmit speech more easily (more sensitive to near end noise)

6 dB: half-duplex is less sensitive to transmit speech (less sensitive to near end noise)

RVol - Receive Volume

30 dB, 27 dB, ... , -57 dB, -60 dB, mute:

digital volume control where positive numbers are AGC'd

ACC - Acoustic (echo canceller) Coefficient Control

Normal: coefficients adapt to echo path

Clear: coefficients held to zero (no cancellation)

Freeze: coefficients held to current values and adaptation halted

AErle - Acoustic ERLE threshold

24 dB: default

18 dB: acoustic echo canceller tends to go to full-duplex more easily (faster)

30 dB: acoustic echo canceller requires good performance to go to full-duplex (slower)

AFNse - Acoustic Full-duplex Noise threshold

zero: use AErle as sole criterion to transition to full-duplex.

-42 dB: echo path may not exist, so go to full-duplex when noise level is below -42 dB (easy) and internal determination of path/no path is complete

-54 dB: echo path may not exist, so go to full-duplex when noise level is below -54 dB (hard) and internal determination of path/no path is complete

PCSen - Path-Change Sensitivity

high: more sensitive to near end path changes (on rare occasions may briefly drop into half-duplex during doubletalk)

low: less sensitive to path changes and more robust to doubletalk

GB - Graded Beta

0.00 dB/ms: use to disable beta grading

0.75 dB/ms: use for acoustically dead rooms (e.g. inside a car)

0.38 dB/ms: use for "typical" rooms

0.19 dB/ms: use for very acoustically live rooms (e.g. glass or tile walls, no carpet, etc.)

Taps - allocation of filter Taps

55.5ms/---: allocate all taps to Acoustic canceller (disables Network canceller)

47.5ms/16ms:use for short Network path echo durations or for longer Acoustic path

38.5ms/24ms:use for typical Network path echo durations

31.5ms/32ms:use for long Network path echo durations (note that Acoustic performance may suffer)

TSD - Transmit Suppression Disable

checked: disable transmit suppression

unchecked enable transmit suppression

TSThd - Transmit Suppression Threshold

15 dB: need 15 dB ERLE at acoustic canceller to discriminate between speech and echo

12 dB: less sensitive to near end speech (more prone to suppressing near-end speech)

9 dB: least sensitive to near end speech (most prone to suppressing near-end speech)

TSAtt - Transmit Suppression Attenuation level

18 dB: default

12 dB: use if noise modulation caused by suppression is annoying and residual echo is not perceptible

24 dB: use if residual echo after suppression is perceptible

TSBias - Transmit Suppression Bias

18 dB: default

15 dB: harder for near end to break in. See CS6420 datasheet for details

21 dB: easier for near end to break in. See CS6420 datasheet for details

TGain - Transmit ADC analog Gain

0 dB, 6 dB, 9.5 dB, 12 dB:

set gain of the ADC at API/APO

Mic - Microphone preamplifier select

API: ADC input is taken from API/MICIN through 34 dB amplifier (HDR1 on board must be set to PREAMP ON)

APO: ADC input is taken from APO/APO_IN (HDR1 on board must be set to PREAMP OFF)

Reset Button

Cold Reset, Default:

cold reset to default register values

Warm Reset, Default:

warm reset to default register values

Cold Reset, Current:

cold reset to register values indicated by controls

Warm Reset, Current:

warm reset to register values indicated by controls

Power Down:

hold CS6420 $\overline{\text{RST}}$ low to force low power mode

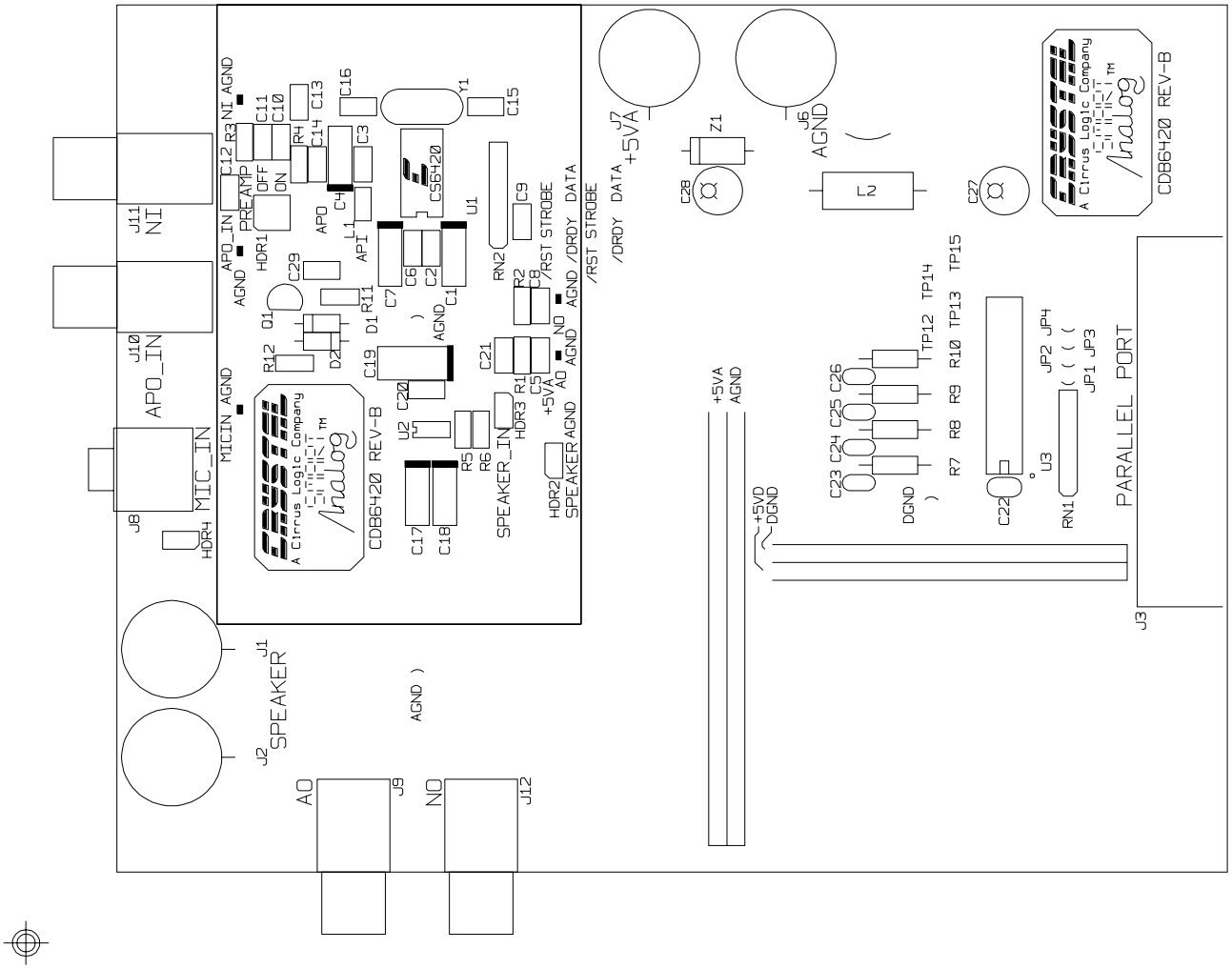
Power Up, Cold Reset, Current:

bring CS6420 $\overline{\text{RST}}$ high; restore register values indicated by controls

Power Up, Warm Reset, Current:

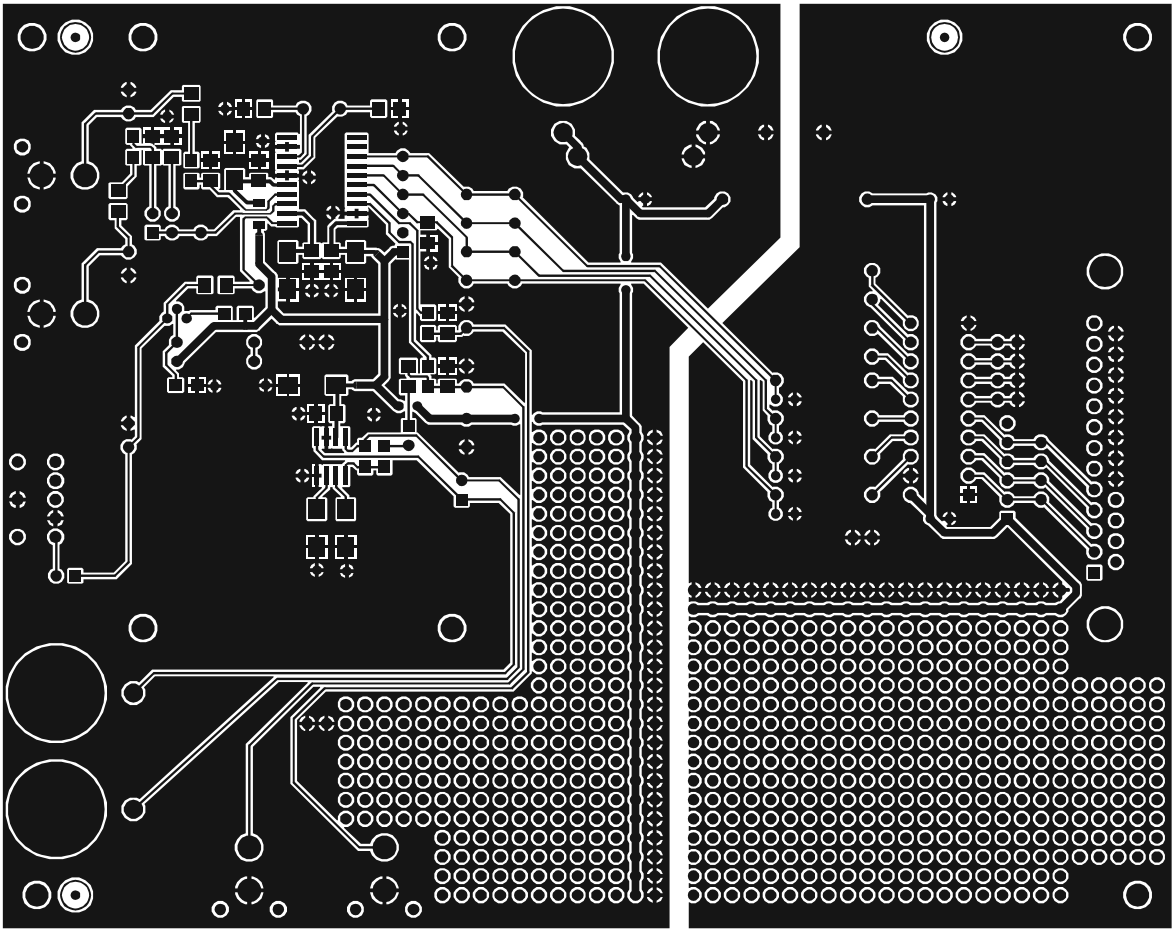
bring CS6420 $\overline{\text{RST}}$ high; warm reset and restore register values indicated by controls

CS6420 CUSTOMER DEMO BD
CDB6420 REV-B



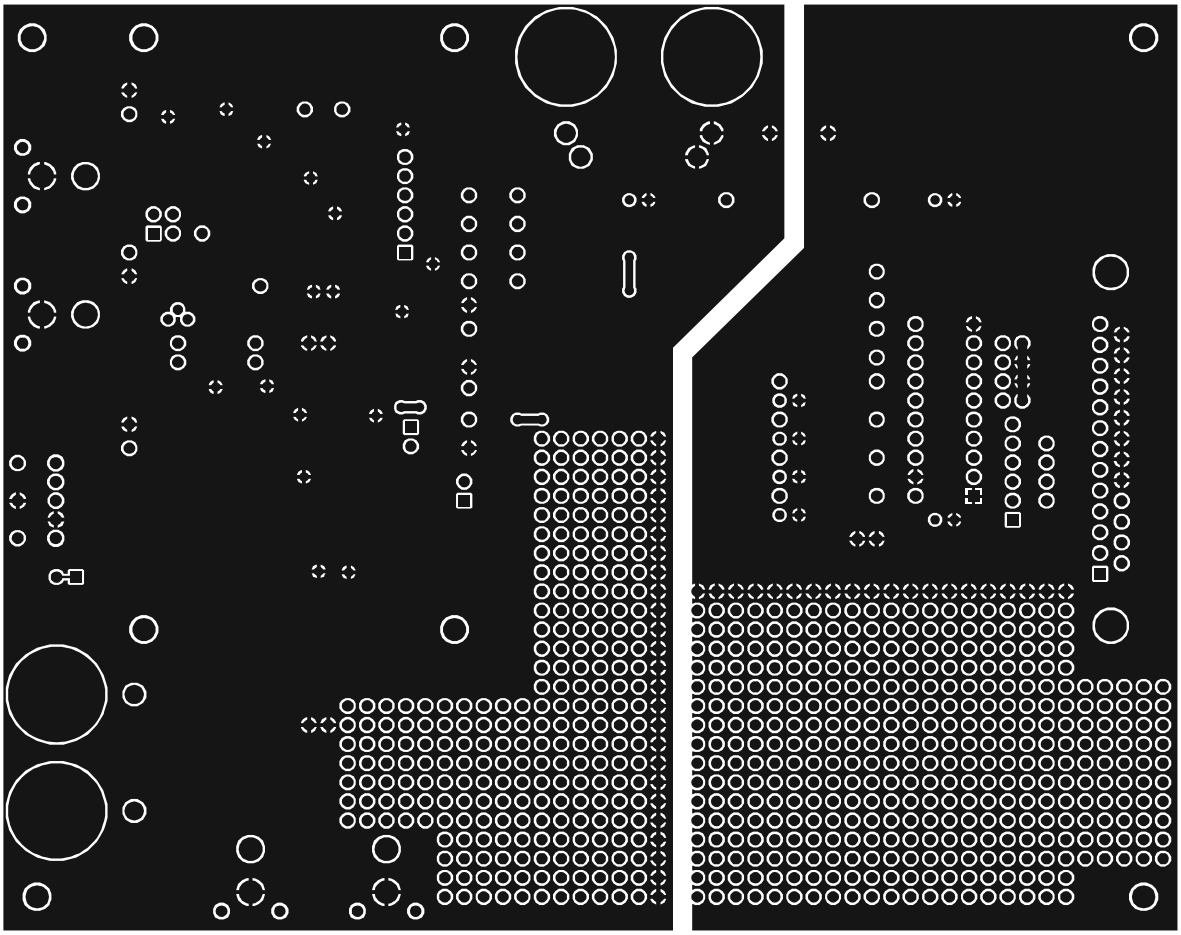
SILKSCREEN - TOP

CS6420 CUSTOMER DEMO BD
CDB6420 REV-B



TOP SIDE

CS6420 CUSTOMER DEMO BD
CDB6420 REV-B



BOTTOM SIDE


SMART
Analog
™