DENSITRON DISPLAYS

OLED DISPLAY MODULE

Application Notes

PRODUCT NUMBER	DD-6448BE-2A with EVK board

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REVISION RECORD

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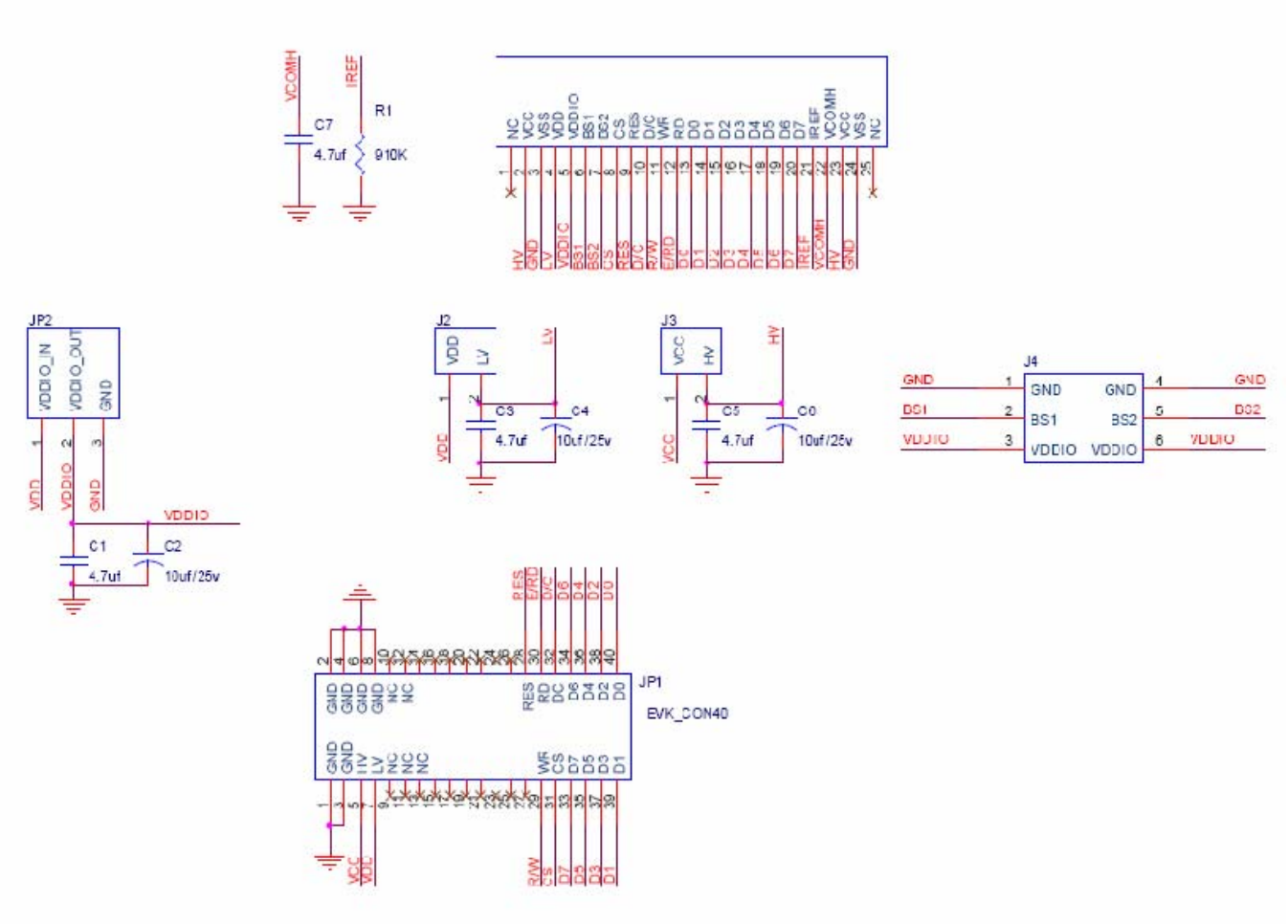
1 EVK Schematic



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2 Symbol Definition

VCC : Power supply for panel driving voltage.

VSS：This is ground pin.

VDD：Power supply for core logic operation.

VDDIO：Power supply for interface logic level.

BS0~BS2：MUC bus interface selection pin(BS0 pulled LOW in internal).

CS：This pin is chip select input(active LOW).

RES：This pin is reset signal input(active LOW).

D/C：This is DATA/COMMAND control pin. When it is Pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address select.

R/W：This is read/write control input pin connecting to the MCU interface. When interface to a 6800-series microprocessor , Read mode will be carried out when this pin is pulled HIGH and write mode when low . When interface to an 8080-microprocessor , this pin when be the data Write input. When serial interface is selected, this pin must be connected to Vss.

E/RD：When interface to a 6800-series microprocessor , this pin will be used as the Enable(E) signal. When interface to an 8080-microprocessor , this pin receives the Read(RD#)signal.

D0~D7：These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D0(SCLK) will be the serial clock input,D1(SDIN) will be the serial data input,D2 should be left opened. When I2C mode is selected,D1(SDAin) AND D2(SDAout) should be tied together,D0(SCL) is the I2Cclock input

IREF：This is segment output current reference pin.

VCOMH：This pin for COM signal deselected level voltage.

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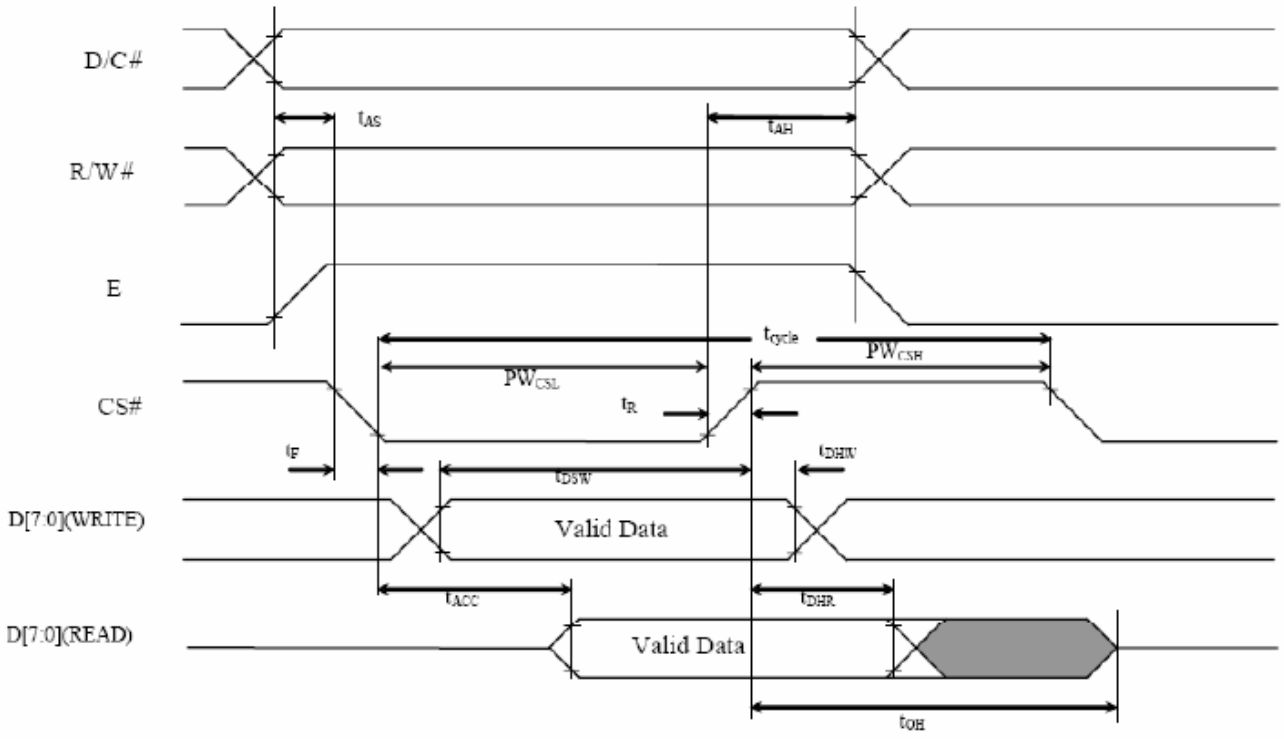
3 Timing characteristics

3.1.1 6800 Interfacing description and timing characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



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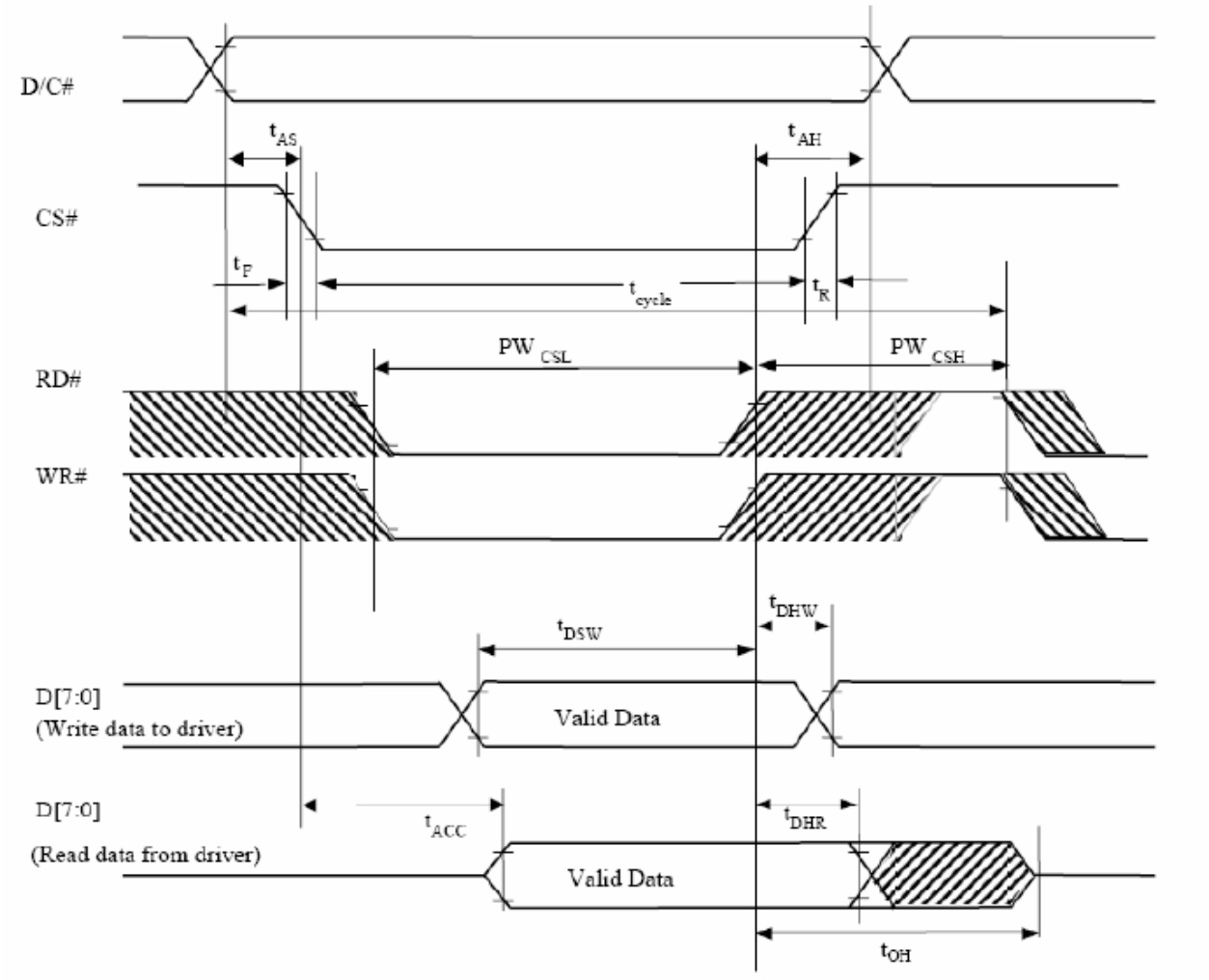
3.1.2 8080 Interfacing descriptions and timing characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time			140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



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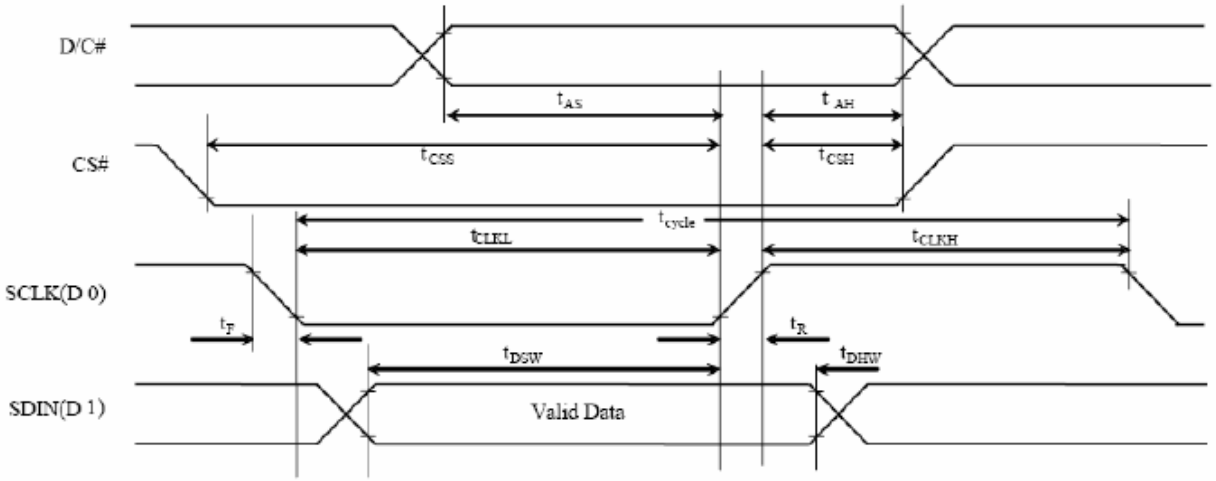
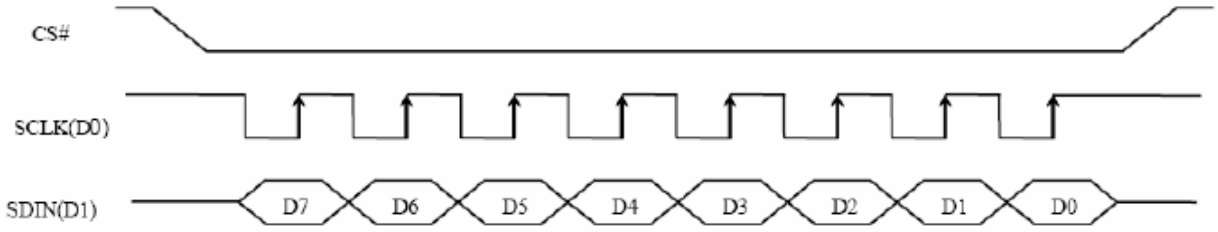
3.1.3 SPI Interfacing and Descriptions Characteristics

(V_{DD} - V_{SS} = 2.4V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





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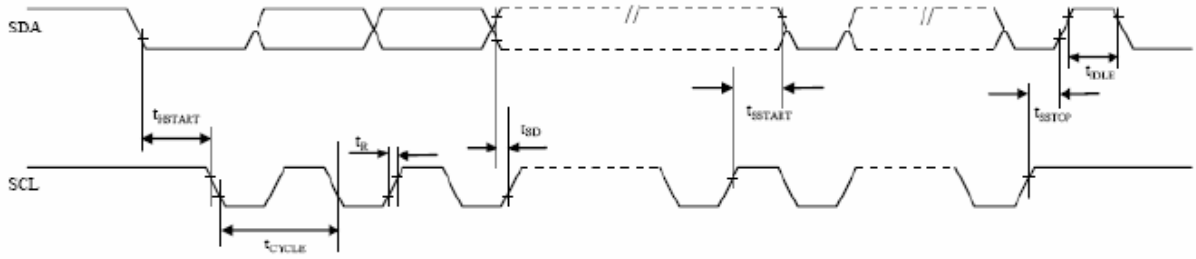
3.1.4 I2C Interfacing and Descriptions Characteristics

(VDD - VSS = 2.4 to 3.5,TA = 25° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



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Connection Between OLED and EVK

Figure 1 EVK PCB and DD-6448BE-2A Module

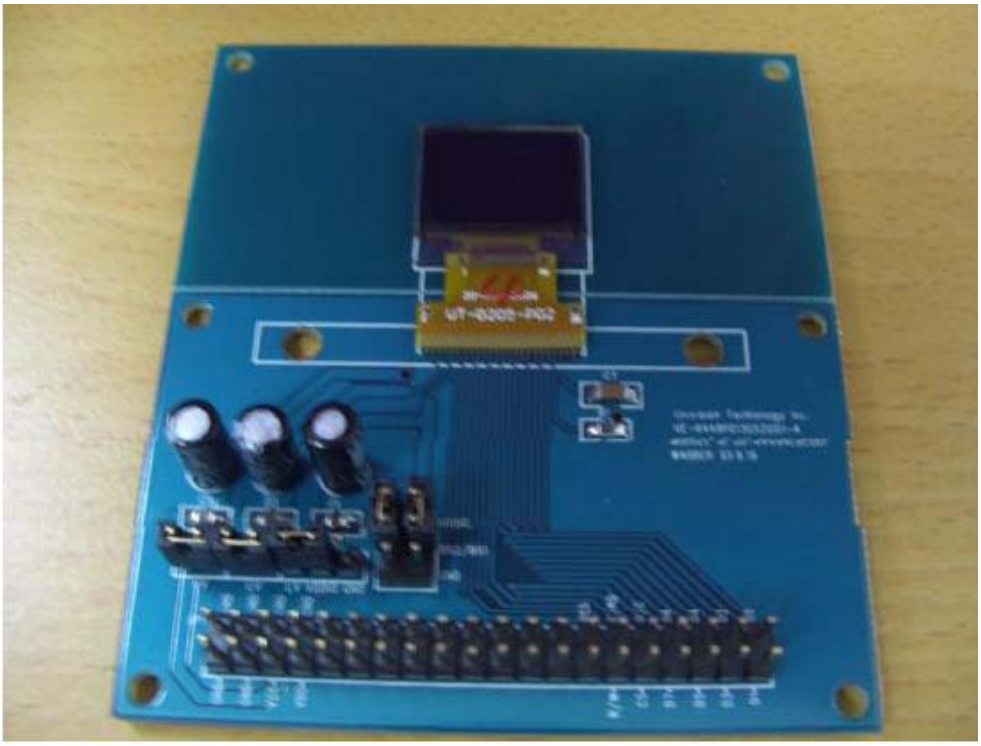

Figure 2 the DD-6448BE-2A and EVK assembled (Top view)

The SSD1305Z is a COG type package, that the connect pads are on top of the module connector. When assembled the module and EVK push the locking pad to lock the module.

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See Figure 1 and 2. The user can use the leading wire to connect EVK with the customers application. The example is shown in Figure 3.

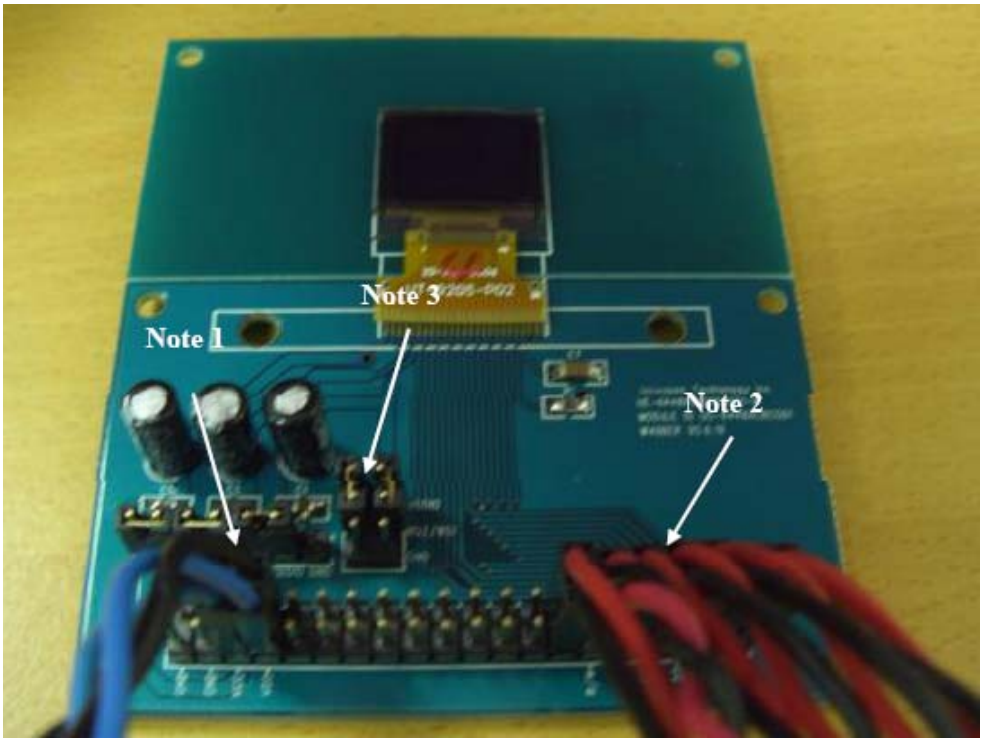

Figure 3 EVK with test platform.

Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.

Note 2: The leading wire has 13 pins totally in this case.
(D0~D7 – E/RD – R/W – D/C – RES – CS)

Note 3: Select Mode (8080 – 6800 – SPI – I2C)

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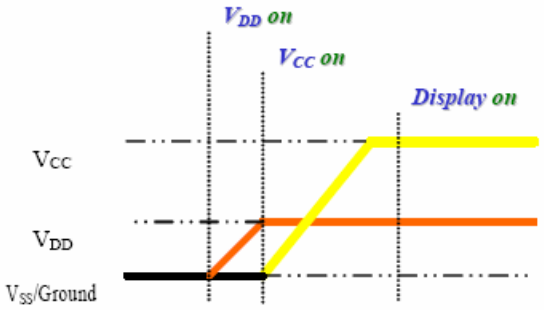
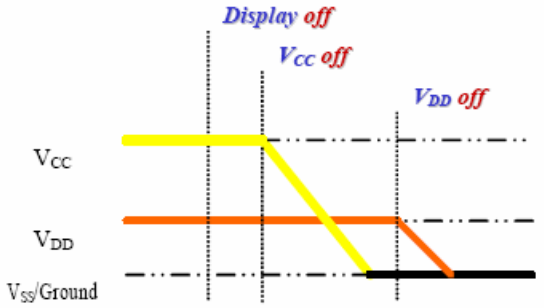
4 How to use the SSD1305Z

4.1.1 Power down and Power up Sequence

To protect the OLED panel and extend the panel life time the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn off. Such that the panel has enough time to charge up or discharge before/after operation.

Power up Sequence: 1. Power up V_{DD} 2. Send Display off command 3. Driver IC Initial Setting 4. Clear Screen 5. Power up V_{DDH} 6. Delay 100ms (when V_{DD} is stable) 7. Send Display on command	
Power down Sequence: 1. Send Display off command 2. Power down V_{DDH} 3. Delay 100ms (when V_{DDH} is reach 0 and panel is completely discharges) 4. Power down V_{DD}	

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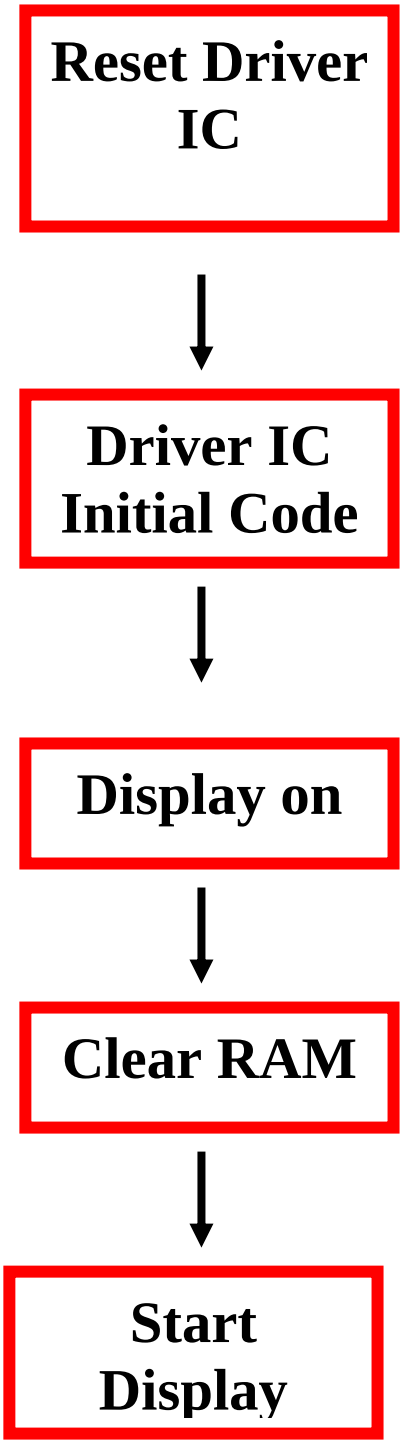
5 How to use the DD-6448BE-2A



RES#=0; Delay 10ms; RES#=1

Suggest all registers set again

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5.1 Recommended Initial code

```
void initial()

{
write_command(0x02);//set low column address

write_command(0x12);//set high column address

write_command(0x40);//(display start set)

write_command(0x2e);//(stop horzontal scroll)

write_command(0x81);//(set contrast control register)
write_command(0x32);

write_command(0x82);//(brightness for color banks)
write_command(0x80);//(display on)

write_command(0xa1);//(set segment re-map)

write_command(0xa6);//(set normal/inverse display)

write_command(0xa8);//(set multiplex ratio)
write_command(0x2F);

write_command(0xd3);//(set display offset)
write_command(0x40);

write_command(0xad);//(set dc-dc on/off)
write_command(0x8E);//

write_command(0xc8);//(set com output scan direction)

write_command(0xd5);//(set display clock divide ratio/oscillator/frequency)
write_command(0xf0);//

write_command(0xd8);//(set area color mode on/off & low power display mode )
write_command(0x05);//

write_command(0xd9);//(set pre-charge period)
write_command(0xF1);

write_command(0xda);//(set com pins hardware configuration)
write_command(0x12);


write_command(0xdb);//(set vcom deselect level)
```


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```
write_command(0x34);

write_command(0x91);//(set look up table for area color)
write_command(0x3f);
write_command(0x3f);
write_command(0x3f);
write_command(0x3f);

write_command(0xaf);//(display on)

write_command(0xa4);//(display on)

}
```


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6 WRITE DATA & COMMAND SUB FUNCTION

```
void write_command(unsigned char aa)

{

IOCLR = 0x000000ff;
IOSET = RD_IN;//RD=1

IOCLR = DC_IN;//RS=0
IOCLR = CS_IN;//CS=0
IOCLR = WR_IN;//W_R=0

IOSET = aa;//--------input command

IOSET = WR_IN;//W=1
IOSET = CS_IN;//CS=1
IOCLR = RD_IN;

}

void write_data(unsigned char bb)

{

IOCLR = 0x000000ff;

IOSET = RD_IN;//RD=1
IOSET = DC_IN;//RS=1
IOCLR = CS_IN;//CS=0
IOCLR = WR_IN;//W_R=0

IOSET = bb; //--------input data

IOSET = WR_IN;//W_R=1
IOSET = CS_IN;//CS_1=1

}
```

NOTE: RD recommended initial code and sub function for 8080 series CPU interface

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