CLOCK OSCILLATORS "HP" series (non-PLL based PECL)





"HP" series use fundamental mode (inverted mesa) crystal to achieve stable and clean 10KH or 100KH differential PEC signals. No multiplier, no overtone and no phase lock loop technique is used. Jitter is as low as 1ps for the 155.520 MHz for SONET/SDH applications. The inherent advantage of differential PECL signal transmission provides improved noise immunity and makes the system less susceptible to ground noise.

PRODUCT SUMMARY:

Package code	Frequency Range	Assembly Technique	Package Size (mm)			
PECL	Trequency mange	Assembly reclinique	[inches]. H: Seat height.			
Thru-Hole Types						
4 PIN MODE	LS					
HP14	19.440 ~ 250 MHz	4 pin DIL full size. Hermetically sealed. Can height = 7.5 mm. Sealed crystal inside.	12.8 x 20.2 x 8.3H [0.504 x 0.795 x 0.327]			
5 PIN MODELS						
HP514	19.440 ~250 MHz	5 pin DIL full size. Hermetically sealed. Can height = 7.5 mm. Sealed crystal inside.	12.8 x 20.2 x 8.3H [0.504 x 0.795 x 0.327]			
6 PIN MODE	LS					
HP614	19.440 ~250 MHz	6 pin DIL full size. Hermetically sealed. Can height = 7.5 mm. Sealed crystal inside.	12.8 x 20.2 x 8.3H [0.504 x 0.795 x 0.327]			
Surface Mount Types	– Gull Wing					
4 PIN MODE	LS					
HP24	19.440 ~250 MHz	4 pin DIL full size. Hermetically sealed. Can height = 7.5 mm. Sealed crystal inside.	12.8 x 20.2 x 9.3H [0.504 x 0.795 x 0.366]			
5 PIN MODE	ĹS					
HP524	19.440 ~250 MHz	5 pin DIL full size. Hermetically sealed. Can height = 7.5 mm. Sealed crystal inside.	12.8 x 20.2 x 9.3H [0.504 x 0.795 x 0.366]			
6 PIN MODELS						
HP624	19.440 ~250 MHz	6 pin DIL full size. Hermetically sealed. Can height = 7.5 mm. Sealed crystal inside.	12.8 x 20.2 x 9.3H [0.504 x 0.795 x 0.366]			
Surface Mount Types	- Leadless					
HP62	19.440 ~250 MHz	6 pad Leadless.	9.6 x 11.4 x 2.5H [0.378 x 0.449 x 0.098]			
HP64	19.440 ~250 MHz	6 pad Leadless.	9.6 x 11.4 x 4.7H [0.378 x 0.449 x 0.185]			

MERCURY www.mercury-crystal.com

Taiwan: TEL (886)-2-2695-7099, FAX (886)-2-2695-7473, e-mail: <u>sales-tw@mercury.com</u> U.S.A.: TEL (1)-909-466-0427, FAX (1)-909-466-0762, e-mail: <u>sales-us@mercury.com</u>

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CLOCK OSCILLATORS "HP" series (non-PLL based PECL)

Logic: PECL square wave



General Specification for "HP" series (low jitter)

 T_A = +25°C, Inclusive of 25°C calibration tolerance, operating temperature range, Input voltage variation, load change, aging, shock and vibration.

Output Wave Form		P E C L 100K square wave			
		Non-PLL based, fundamental mode inverted n	nesa crystal used.		
Frequency Ra	inge	19.440 ∼ 250 MHz			
Standard Frequencies		38.880, 44.736, 50.000, 77.760, 100.000, 10207.360, 212.500 MHz (partial list)	06.250, 125.000, 155.520, 166.6286, 200.0,		
Frequency Sta	ability emp. range (code " C ")	"A": ±25 ppm over 0°C to +70°C "C": ±100 ppm over 0°C to +70°C For non-standard please give desired frequency stability after the "C".			
	, , ,	For example "C20" is ± 20 ppm over 0 to $+7$			
Frequency Sta Industrial temp	ability o. range (code "I")	"D":±25 ppm over -40°C to +85° (not available on all packages) "E":±50 ppm over -40°C to +85°C			
Frequency S	tability	vs Supply voltage ±5% change: ±3 ppm max. vs Load ±10% change: ±2 ppm max.			
Input Voltage	Vcc	$+3.3 \text{ V} \pm 5\% \text{ (LVPECL)}$	$+5.0 \text{ V} \pm 5\% \text{ (PECL)}$		
Output Voltag (Relative to gre	e HIGH "1", V_{OH} ound)	2.25 V min.	3.95 V min. 4.05 typical 4.15 V max		
Output Voltag (Relative to gre	e LOW "0", V_{OL} ound)	1.65 V max.	3.15 min; 3.25 typical; 3.35 V max.		
Current Cons (measured wi	umption th terminating resistors)	58 mA typical at 155.520 MHz 54 mA typical at 77.760 MHz 73 mA typical at 77.760 MHz			
Load		50 ohms into Vcc-2V or Thevenin equivalent. (terminating resistors required on all outputs)			
Rise Time (Tr) and Fall Time (Tf)		1.5 nano sec. max (20% ↔ 80% Vcc)			
Duty Cycle at 50% output swing		$50\pm2\%$ typical; $50\%\pm5\%$ max. both outputs			
Jitter	155.520 MHz, 5V as example	Over 1 Hz to 1 MHz band width: 20 pico seconds RMS max. Over 10 Hz to 1 MHz band width: 1.8 pico seconds RMS max. Over 100 Hz to 1 MHz band width: 0.2 pico seconds RMS max. Over 12 kHz to 20 MHz band width: 1 pico seconds RMS max. Over 10 Hz to 20 MHz band width: 5 pico seconds RMS max.			
SSB Phase	155.520 MHz, 5V	-50 dBc at 10 Hz offset, -80 dBc at 100 Hz offset, -110 dBc at 1 kHz offset,			
Noise Start-up Time	as example	-135 dBc at 10 kHz offset, -145 dBc at 100 kHz offset, -145 dBc at 1 MHz offset			
•		10 m sec. max.			
Aging Storage Temp	noraturo	±2 ppm / year max.			
Storage Temperature Tri-state option		-55°C to +100°C PECL output is disabled and complimentary output remains high when Tri-state pin is "HIGH". Both PECL and complimentary PECL outputs are high when Tri-state pin is "LOW".			

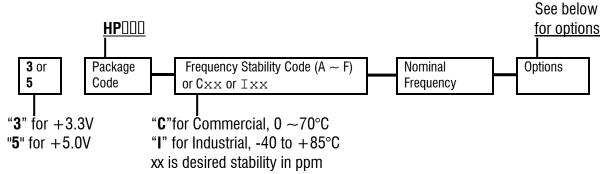
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CLOCK OSCILLATORS "HP" series (non-PLL based PECL)





PART NUMBER FORMAT AND EXAMPLES:



5HP14-A-125.0

represents +5.0 V non-PLL based PECL clock oscillator, 125.0 MHz in 4 pin DIP full size, frequency stability is ± 25 ppm over 0 to $+70^{\circ}$ C. note: 125 MHz fundamental mode inverted mesa crystal used.

3HP614-C20-155.520-3T

represents +3.3 V clock oscillator with non-PLL based PECL output 155.520 MHz in 6 pin full size DIL, frequency stability is ± 20 ppm over 0 to $+70^{\circ}$ C (commercial), with Tri-state option on pin 3. note: 155.520 MHz fundamental mode inverted mesa crystal used.

MODELS WITH OPTIONS

4 pin thru-hole and gull wing models.

Part number suffix	Pin 1	Pin 7	Pin 8	Pin 14
blank	No Connection	Case ground	PECL Output	Supply Voltage
-1C	Complimentary PECL Output	Case ground	PECL Output	Supply Voltage
-1T	Tri-State	Case ground	PECL Output	Supply Voltage

5 pin thru-hole and gull wing models

	Option			Option	
Part number suffix	Pin 1	Pin 7	Pin 8	Pin 9	Pin 14
blank	No Connection	Case ground	PECL Output	Complimentary PECL Output	Supply Voltage
- 1T	Tri-State	Case ground	PECL Output	Complimentary PECL Output	Supply Voltage

6 pin thru-hole and gull wing models

_		Option			option	
Suffix	Pin 1	Pin 3	Pin 7	Pin 8	Pin 12	Pin 14
- 1T	Tri-State	No connection	Case ground	PECL Output	Complimentary PECL output	Supply Voltage
- 3T	No Connection	Tri-State	Case ground	PECL Output	Complimentary PECL output	Supply Voltage

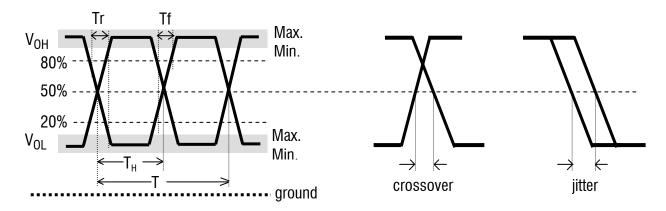
6 pad leadless surface mount models : No option available. See package drawing for pin connect

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Logic: PECL square wave

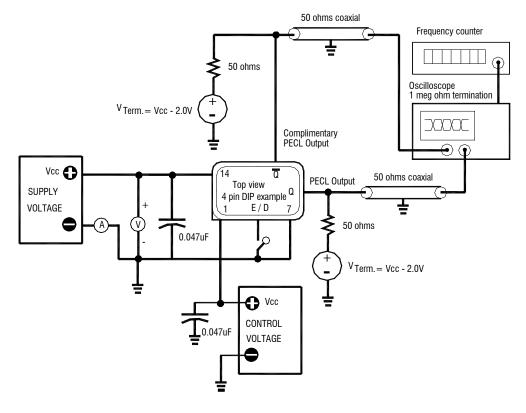


OUTPUT WAVEFORMS:



Duty cycle= $(T_H/T)*100$

TEST CIRCUIT Apply to all models and options. Both PECL and complimentary PECL outputs shown.



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