

# Farnell Order Code: 1538956

**FOX MODEL: FXO-LC735R-200**

**FOX Part Number: 771-200-25**

**LVDS, CERAMIC, SMD, OSCILLATOR**

**Specifications**

| Parameters                                     |                           |
|--|---------------------------|
| Frequency                                      | 200 MHz                   |
| Frequency Stability <sup>1</sup>               | ±50 PPM                   |
| Temperature Range                              |                           |
| Operating (T <sub>OPR</sub> )                  | -40°C ~ +85°C             |
| Storage (T <sub>STG</sub> )                    | -55°C ~ +125°C            |
| Supply Voltage (V <sub>DD</sub> )              | 3.3V ± 5%                 |
| Input Current (I <sub>DD</sub> )               | 100 mA Max                |
| Differential Output Voltage (V <sub>OD</sub> ) | 0.250V ~ 0.450V           |
| Output Offset Voltage (V <sub>OS</sub> )       | 1.125V Typ                |
| Differential Output Swing (V <sub>P-P</sub> )  | 0.250V <sub>P-P</sub> Min |
| Output Symmetry (50% V <sub>P-P</sub> Level)   | 45% ~ 55%                 |
| Rise Time (20% ~ 80% V <sub>P-P</sub> ) (TR)   | 400 pS Max                |
| Fall Time (80% ~ 20% V <sub>P-P</sub> ) (TF)   | 400 pS Max                |
| Output Load (Recommended Circuit below)        | 100 ohms                  |
| Startup Time (T <sub>S</sub> )                 | 10 ms Max                 |
| Output Enable / Disable Time <sup>2</sup>      | 100 nS Max                |
| Phase Jitter (12kHz ~ 20MHz)                   | 0.9 pS Typ.               |
| Maximum Soldering Temp / Time                  | 260°C / 10 Seconds        |
| Moisture Sensitivity Level (MSL)               | 1                         |
| Termination Finish                             | Au                        |

<sup>1</sup> Inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock, and vibration.

<sup>2</sup> An internal pullup resistor from pin 1 to pin 6 allows active output if pin 1 is left open.

| ENABLE/DISABLE FUNCTION <sup>2</sup>           |                   |
|--|-------------------|
| Pin 1  | OUTPUT (Pin 4, 5) |
| OPEN <sup>2</sup>                              | ACTIVE            |
| '1' Level V <sub>IH</sub> ≥ 70%V <sub>DD</sub> | ACTIVE            |
| '0' Level V <sub>IL</sub> ≤ 30%V <sub>DD</sub> | High Z            |

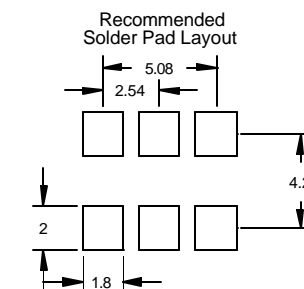
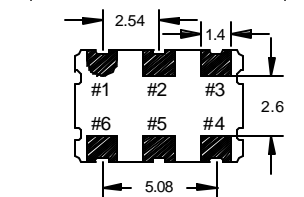
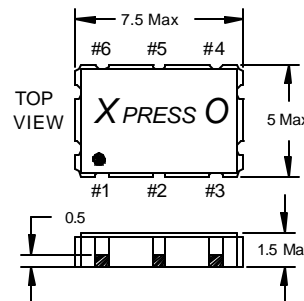
**NOTE** A 0.01µF bypass capacitor should be placed between V<sub>DD</sub> (Pin6) and GND (Pin 3) to minimize power supply line noise.

**RoHS Compliance Status: Compliant**



Drawing is for reference to critical specifications defined by size measurements. Certain non-critical visual attributes, such as side castellations, reference pin shape, etc. may vary

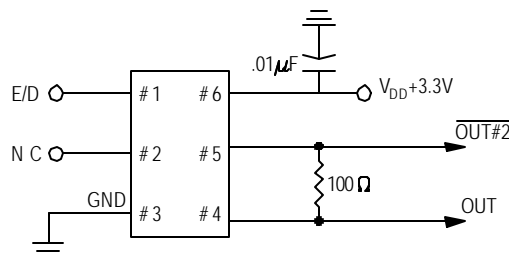
**Mechanical / Dimensions (millimeters):**



**Pin Connections**

- #1 E/D      #4 Output 1
- #2 NC      #5 Output 2
- #3 GND    #6 V<sub>DD</sub>

**A. Recommended Circuit**



**NOTE** The above specifications, having been carefully prepared and checked, is believed to be accurate at the time of publication; however, no responsibility is assumed by Fox Electronics for inaccuracies.

| Reference / Comments | Title / Description: Product Specifications |              |                  |
|----------------------|---|--------------|------------------|
|                      | Drawing Number: DWG-4551-4                  | Rev: 1       | Size: A          |
|                      | Part Number: 771-200-25                     |              | Cage: 61429      |
|                      | Draftsperson: AR                            | Approved: BN | Date: 01/15/2008 |