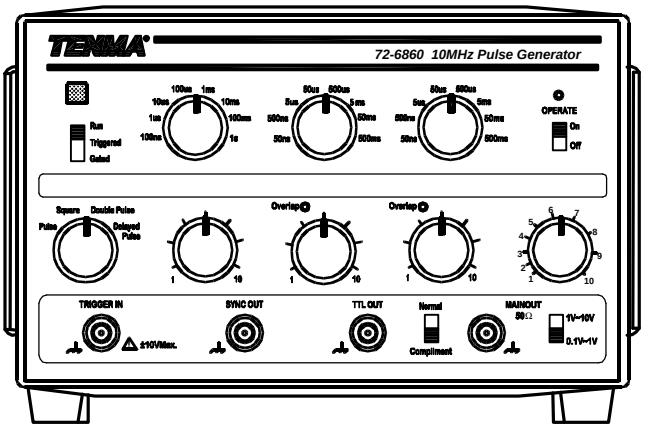
REVISIONS			DOC. NO. SPC-F004 * Effective: 12/21/98 * DCP No: 680					
DCP #	REV	DESCRIPTION	DRAWN	DATE	CHECKD	DATE	APPRVD	DATE
430	A	RELEASED	JWM	3/14/01	JC	9/4/01	DJC	9/21/01



Specifications

Period, Pulse Width, Delay

Each parameter is variable within 8 overlapping decade ranges with a vernier providing continuously variable control within each range.

Period

Range: 100nsec to 10sec (10MHz to 1Hz)
Jitter: <0.1%

Pulse Width

Range: 50nsec to 5sec
Jitter: <0.1%

Delay:

Range: 50nsec to 5sec

Trigger, Gate

Run

Normal operational mode in which pulses are generated continuously at 0.1Hz to 10MHz.

Triggered

DC to 10MHz pulse train in synchronism with external trigger pulses; pulse width determined by pulse width controls. Trigger can be generated manually from front panel button.

Gated

0.1Hz to 10MHz pulse train, parameters set by period and pulse width controls, starts synchronously with leading edge of gate input. Last pulse is completed at the end of gating period. Gating signal can be generated manually from front panel button.

Pulse Modes

Normal Pulse

One pulse is generated each period. The delay setting is ignored.

Square wave

0.1Hz to 10MHz squarewave, frequency set by the period controls. Pulse width and delay settings ignored.
Mark: Space Ratio: 1:1±10 %

Double Pulse

A second pulse is generated after a delay set by the delay controls; the delay is related to the leading edge of the first pulse.

Delayed Pulse

A pulse is generated after a delay set by the delay controls; the delay is related to the rising edge of the trigger signal.

Inputs

Gate/Trig Input

Frequency Range: DC~10MHz
Signal Range: TTL threshold; max. input ±10V
Min. pulse width: >30nsec
Input Impedance: Typically 10k Ω

Outputs

50Ω Output
Amplitude: Two switch selectable ranges of 0.1V~1.0V and 1V~10V from 50 Ω. (50mV to 500mV and 500mV to 5V into 50Ω) Adjustable within ranges by a single turn vernier.
Rise/Fall Times: Typically 10nsec into 50 Ω load.
Maximum 15ns
Aberrations: Typically <5 % for output set at >20 % of range max. into 50 Ω

Aux. Output

Duplicates 50 Ω output but at a fixed CMOS/TTL level

Sync Output

Amplitude: a positive going pulse at CMOS/TTL level.
Timing: Leading edge starts >20nsec before the TTL/50 Ω output transition.
Duration: Typically 30nsec

Complement Switch

Inverts the AUX and 50 Ω outputs

General
Power: 115V AC nominal 50/60Hz, adjustable internally; operating range ±14 % of nominal; 20VA max.
Size: 140mm(H) x 220mm(W) x 230mm(D)
Weight: 1.6kg (3.5lb)
Operating Range: +5°C to 40°C; 20 %~80% R.H.
Storage Range: -40°C to 70°C
Safety: Complies with EN61010-1
EMC: Complies with EN5508-1 and EN50082-1

SPC-F004.DWG

TENMA®

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE FOR REFERENCE PURPOSES ONLY.

DRAWN BY:	DATE:
Jeff McVicker	3/14/01
CHECKED BY:	DATE:
JOHN COLE	9/4/01
APPROVED BY:	DATE:
Daniel Carey	9/21/01

DRAWING TITLE: 10MHz Pulse Generator with Delay

SIZE	DWG. NO.	ELECTRONIC FILE	REV
A	72-6860	19C7734.dwg	A

SCALE: NTS | U.O.M.: INCHES [mm] | SHEET: 1 OF 1