

# **Specification for Approval**

PRODUCT NAME: PRODUCT NO.: Part Number: RGS11128032BW000 9913601000 PMO13601

	CUSTOMER	
	APPROVED BY	
DATE:		

RITDISPLAY CORP. APPROVED





# **REVISION RECORD**

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2005. 10. 03	
X02	<ul> <li>Add the information of module weight</li> <li>Add the operating conditions for different luminance</li> <li>Add the panel electrical specification</li> <li>Modify external dimension – add TAB bending view</li> </ul>	2005. 10. 25	Page 5, 6, 7, 8 & 16
A01	<ul> <li>Transfer from X version</li> <li>Add the packing specification</li> </ul>	2005. 11. 08	Page 17





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## <u>1. SCOPE</u>

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

## 2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## 3. FEATURES

- Small Molecular Passive Organic Light Emission Diode.
- Color : Blue
- Panel matrix : 128x32
- Driver IC : SSD1303
- Excellent Quick response time : 10µs
- Extremely thin thickness for best mechanism design : 1.65mm
- High contrast : 500:1
- Wide viewing angle : 160°
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -20 to 70 °C

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## 4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 32 (H)	dot
2	Dot Size	0.195 (W) x 0.195 (H)	mm <sup>2</sup>
3	Dot Pitch	0.215 (W) x 0.215 (H)	mm <sup>2</sup>
4	Aperture Rate	82	%
5	Active Area	27.5 (W) x 6.86 (H)	mm <sup>2</sup>
6	Panel Size	32.7 (W) x 14.5 (H)	mm <sup>2</sup>
7	Panel Thickness	1.65	mm
8	Module Size	32.7 (W) x 29 (H) x 1.65 (T)	mm <sup>3</sup>
9	Diagonal A/A size	1.1	inch
10	Module Weight	1.63 ± 10%	gram





## **5. MAXIMUM RATINGS**

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V <sub>DD</sub> )	-0.3	3.5	V	Ta = 25°C	
Supply Voltage(Vcc)	8	16	V	Ta = 25°C	
Operating Temp.	-20	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Operating Life Time	2,200	-	Hrs	80 cd/m <sup>2</sup> , 50% checkerboard	Note (1)
Operating Life Time	3,000		Hrs	60 cd/m <sup>2</sup> , 50% checkerboard	Note (2)
Operating Life Time	7,000	-	Hrs	40 cd/m <sup>2</sup> , 50% checkerboard	Note (3)
Storage Life Time	20,000	-	Hrs	Ta=25°C, 50% RH	

Note:

(A) Under Vcc = 10 Volts, Ta =  $25^{\circ}$ C, 50% RH.

- (B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.
- (1) Setting of  $80cd/m^2$  :
  - Contrast setting : 0x52
  - Frame rate : 85Hz
  - Duty setting : 1/32
- (2) Setting of  $60cd/m^2$  :
  - Contrast setting : 0x3A
  - Frame rate : 85Hz
  - Duty setting : 1/32

(3) Setting of 40cd/m<sup>2</sup> :

- Contrast setting : 0x22
- Frame rate : 85Hz
- Duty setting : 1/32

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## 6. ELECTRICAL CHARACTERISTICS

#### **6.1 D.C ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
Vcc	Analog power supply (for OLED panel)	Ta=-20 °C to +70°C	9.5	10	10.5	V
V <sub>DD</sub>	Digital power supply	Ta=-20 °C to +70°C	2.4	2.7	3.5	V
I <sub>DD</sub>	Operating current for $V_{DD}$ $V_{DD} = 2.7V$ , $V_{CC} = 12V$ , IREF = 10uA No loading, All Display ON	Contrast=FF	-	190	-	uA
I <sub>CC</sub>	Operating current for $V_{CC}$ $V_{DD} = 2.7V$ , $V_{CC} = 12V$ , IREF = 10uA All Display ON	Contrast=FF	-	550	-	uA
VIH	Hi logic input level		0.8* V <sub>DD</sub>	-	V <sub>DD</sub>	V
V <sub>IL</sub>	Low logic input level		0	-	0.2* V <sub>DD</sub>	V
V <sub>он</sub>	Hi logic output level		0.9* V <sub>DD</sub>	-	V <sub>DD</sub>	V
Vol	Low logic output level		0	-	0.1* V <sub>DD</sub>	V
	Segment on output current	Contrast=FF	285	320	355	uA
	V <sub>DD</sub> =2.7V, V <sub>CC</sub> =12V, IREF=10uA, Display on,	Contrast=AF	-	220	-	uA
I <sub>SEG</sub>	Segment pin under test is	Contrast=5F	-	120	-	uA
	connected with a 20K resistive load to $V_{SS}$	Contrast=0F	-	20	-	uA





#### 6.2 ELECTRO-OPTICAL CHARACTERISTICS

#### PANEL ELECTRICAL SPECIFICATIONS

	NAINI				
PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		6	8	mA	All pixels on (1)
Standby mode			~		Standby mode
current		1	2	mA	10% pixels on (2)
Normal mode power		60	80	mW	All pixels on (1)
consumption		60	00	THVV	All pixels on (1)
Standby mode power		10	20	mW	Standby mode
consumption		10	20	THVV	10% pixels on (2)
Normal mode	45	60		cd/m <sup>2</sup>	Diaplay Avarage
Luminance	45	60		Cu/m	Display Average
Standby mode		10		cd/m <sup>2</sup>	Display Average
Luminance		10		Cu/III	Display Average
CIEx (Blue)	0.11	0.15	0.19		V V (CIE 1021)
CIEy (Blue)	0.22	0.27	0.32		x, y (CIE 1931)
Dark Room Contrast	500:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 10V
- Contrast setting : 0x3F
- Frame rate : 85Hz
- Duty setting : 1/32

(2) Standby mode condition :

- Driving Voltage : 10V
- Contrast setting : 0x00
- Frame rate : 85Hz
- Duty setting : 1/32

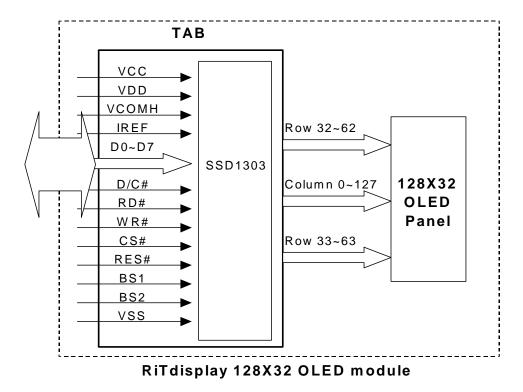
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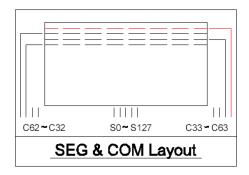


## 7. INTERFACE

#### 7.1 FUNCTION BLOCK DIAGRAM



#### 7.2 PANEL LAYOUT DIAGRAM



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#### 7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO.	TYPE	DESCRIPTION
NC	1	-	No connection
V <sub>SS</sub>	2	-	This is a ground pin.
Test 0	3	-	Reserved pin; No connection and left float
Test 1	4	-	Reserved pin; No connection and left float
Test 2	5	-	Reserved pin; No connection and left float
Test 3	6	-	Reserved pin; No connection and left float
Test 4	7	-	Reserved pin; No connection and left float
NC	8	-	No connection
NC	9	-	No connection
NC	10	-	No connection
V <sub>DD</sub>	11	I	Voltage power supply for logic
BS1	12	Ι	MCU interface selection input
BS2	13	Ι	MCU interface selection input
NC	14	-	No connection
CS#	15	-	This is a chip select control pin.
RES#	16	Ι	Hardware reset signal
D/C#	17	I	This is a Data/Command control pin.
WR#	18	I	This pin is used to receive the Write Data signal.
RD#	19	_	This pin is used to receive the Read Data signal.
D0	20	I/O	This pin is bi-direction data signal
D1	21	I/O	This pin is bi-direction data signal
D2	22	I/O	This pin is bi-direction data signal
D3	23	I/O	This pin is bi-direction data signal
D4	24	I/O	This pin is bi-direction data signal
D5	25	I/O	This pin is bi-direction data signal
D6	26	I/O	This pin is bi-direction data signal
D7	27	I/O	This pin is bi-direction data signal
I <sub>REF</sub>	28	I	A resistor should be connected between this pin and $V_{\text{SS}}$
V <sub>COMH</sub>	29	Ι	A capacitor should be connect between this pin and $V_{\text{SS}}$
V <sub>CC</sub>	30	Ι	Positive high voltage power supply
NC	31	-	No connection





#### 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

					_	_	_						-	_		_
				н	0	1	32	33	4	5	99	57	28	29	30	31
				OUT	SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	 SEG128	SEG129	SEG130	SEG131
					•,	•,	•,	•,	•,	•,	•,	•,	S	S	S	S
				-												
				Address Remap='1	0x83h	0x82h	0x81h	0x80h	0x7Fh	0×7Eh	0×7Dh	0x7Ch	0x03h	0×02h	0x01h	0x00h
				dres ma	θxθ	0xε	3x0	θXΘ	0×7	0×7	0×7	0×7	ŏ	0X0	0XC	ŏ
				Add Re												
				Column Address nap='0' Remap:												
				Column Remap='0'	h	1h	2h	Зh	4h	Бh	вh	7h	Ч	Чh	2h	ЗЬ
	Row A	ddress		en C	0x00h	0x01h	0x02h	охозh	0x04h	0x05h	0x06h	0x07h	0x80h	0x81h	0x82h	0x83h
OUT	Direction='1'	Direction='0'		Ŗ	)	)	0	)	0	)	0	0	Ŭ	0	)	Ŭ
COM0	0x3Fh	0x00h		D0												
COM1	0x3Eh	0x01h		D1												
COM2	0x3Dh	0x02h		D2												
COM3	0x3Ch	0x03h		D3												
COM4	0x3Bh	0x04h	PAGE 0	D4												
COM5	0x3Ah	0x05h		D5												
COM6	0x39h	0x06h		D6												
COM7	0x38h	0x07h		D7												
COM8	0x37h	0x08h		D0												
COM9	0x36h	0x09h		D1												
COM10	0x35h	0x0Ah		D2												
COM11	0x34h	0x0Bh	PAGE 1	D3												
COM12	0x33h	0x0Ch	T/IOE I	D4												
COM13	0x32h	0x0Dh		D5												
COM14	0x31h	0x0Eh		D6												
COM15	0x30h	0x0Fh		D7												
COM16	0x2Fh	0x10h		D0												
COM17	0x2Eh	0x11h		D1												-
COM18	0x2Dh	0x12h		D2												<b>—</b>
COM19	0x2Ch	0x13h	PAGE 2	D3												
COM20 COM21	0x2Bh 0x2Ah	0x14h 0x15h		D4 D5										_		<b>—</b>
COM21	0x29h	0x15h		D5	-									_	-	-
COM23	0x2911 0x28h	0x1011		D7												-
	0/12011	0x1111														
:																
COM48	0x0Fh	0x30h		D0												
COM49	0x0Eh	0x31h		D1									L			L
COM50	0x0Dh	0x32h		D2												<u> </u>
COM51	0x0Ch	0x33h	PAGE 6	D3									L			L
COM52	0x0Bh	0x34h		D4												L
COM53	0x0Ah	0x35h		D5												i
COM54	0x09h	0x36h		D6								_				
COM55	0x08h	0x37h		D7									<u> </u>			—
COM56	0x07h 0x06h	0x38h		<u>D0</u> D1			$\vdash$									<b> </b>
COM57 COM58	0x06h 0x05h	0x39h 0x3Ah		D1 D2									┣──			-
COM59	0x05h 0x04h	0x3An 0x3Bh		D2 D3										$\vdash$		-
COM60	0x0411 0x03h	0x3Ch	PAGE 7	D3									<u> </u>			<u> </u>
COM61	0x03h	0x3Dh		D4 D5												-
COM62	0x02h 0x01h	0x3Eh		D6									<u> </u>			<u> </u>
COM63	0x00h	0x3Fh		D7												<u> </u>
	0/0001		•		•											

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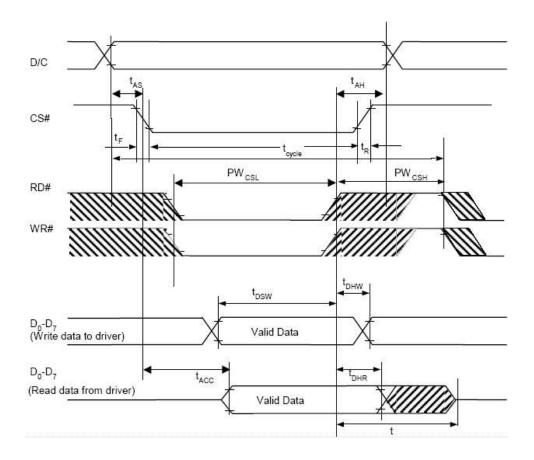




#### 7.5 INTERFACE TIMING CHART

#### $(V_{DD} - V_{SS} = 2.4 \text{ to } 3.5\text{V}, T_A = 25^{\circ}\text{C})$

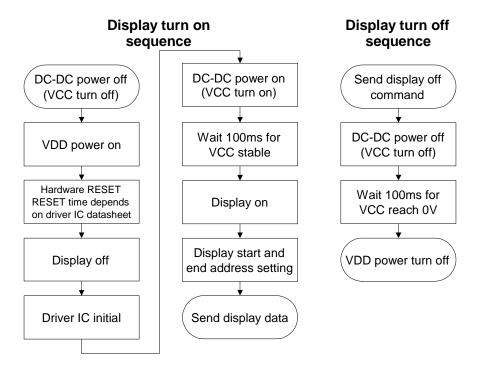
Symbol	Parameter	Min	Тур	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	300	-	-	ns
t <sub>AS</sub>	Address Setup Time	0	-	-	ns
t <sub>ah</sub>	Address Hold Time	0	-	-	ns
t <sub>osw</sub>	Write Data Setup Time	40	-	-	ns
t <sub>DHW</sub>	Write Data Hold Time	7	-	-	ns
t <sub>DHR</sub>	Read Data Hold Time	20	-	-	ns
t <sub>он</sub>	Output Disable Time	-	-	70	ns
t <sub>ACC</sub>	Access Time	-	-	140	ns
PW <sub>CSL</sub>	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60			
PW <sub>CSH</sub>	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60			
t <sub>R</sub>	Rise Time	-	-	15	ns
t <sub>F</sub>	Fall Time	-	-	15	ns





### 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

#### 8.1 POWER ON / OFF SEQUENCE



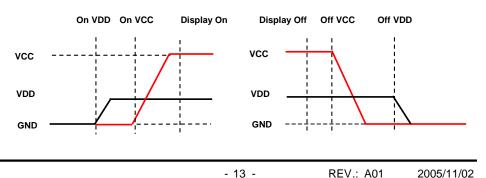
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

Power up Sequence:

- 1. Power up VDD
- 2. Hardware RESET
- 3. Send display off command
- 4. Power up VCC
- 5. Delay 100ms (when VCC is stable)
- 6. Send Display on command

Power down Sequence:

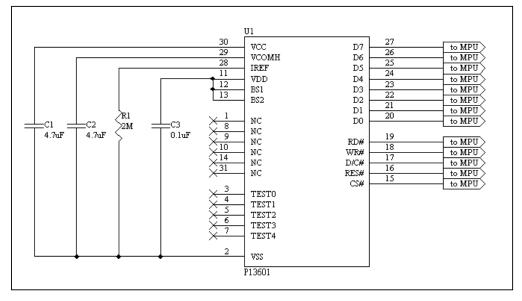
- 1. Send Display off command
- 2. Power down VCC
- 3. Delay 100ms (When VCC is reach 0 and panel is completely discharges)
- 4. Power down VDD







#### **8.2 APPLICATION CIRCUIT**



This circuit is designed for 8080 interface

#### 8.3 COMMAND TABLE

Refer to SSD1303 IC Spec.





## 9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	3
2	Low temp. (Non-operation)	-40°C, 240hrs	2
3	High temp. (Operation)	70°C, 120hrs	3
4	Low temp. (Operation)	-20°C, 120hrs	2
5	High temp. / High humidity (Non-operation)	85°C, 85%RH, 120hrs	5
6	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
7	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	2
8	OLB Peel strength (Non-operation)	500g/cm (Speed~ 50mm/min)	5
9	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
10	Drop	Height: 120cm Sequence : 1 angle  3 edges and 6 faces Cycles: 1	1 Carton
11	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

#### Test and measurement conditions

- 1. All measurements shall not be started until the specimens attain to temperature stability.
- 2. All-pixels-on is used as operation test pattern.
- 3. The degradation of Polarizer are ignored for item 1, 5 & 6.

#### **Evaluation criteria**

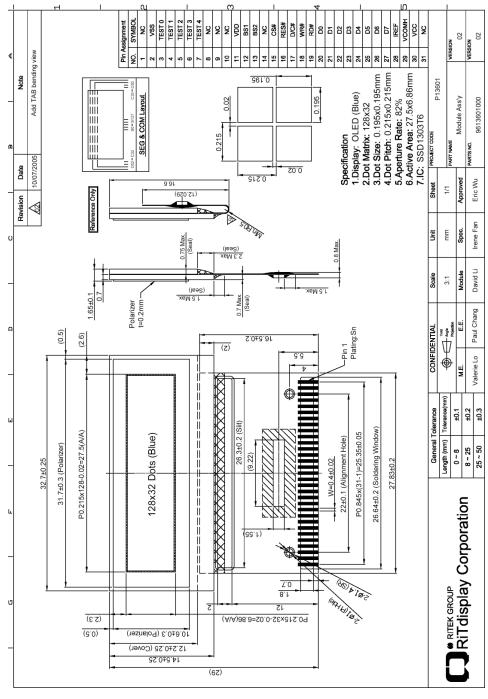
- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: > 50% of initial value.
- 4. Current consumption: within  $\pm$  50% of initial value.

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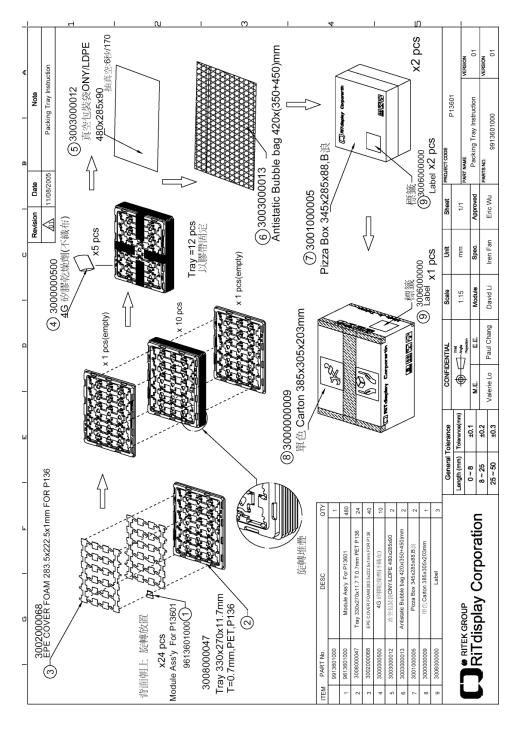
## **10. EXTERNAL DIMENSION**







## **11. PACKING SPECIFICATION**



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## **12. APPENDIXES**

#### **APPENDIX 1: DEFINITIONS**

#### A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

#### **B. DEFINITION OF CONTRAST RATIO**

The contrast ratio is defined as the following formula:

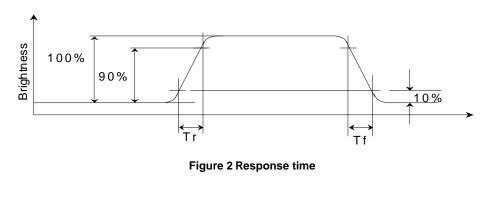
Luminance of all pixels on measurement

Contrast Ratio =

Luminance of all pixels off measurement

#### C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.





#### D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

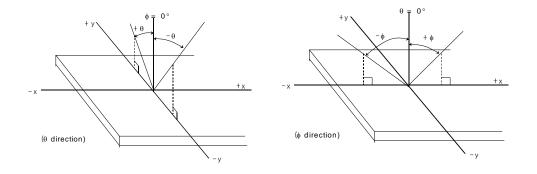


Figure 3 Viewing angle



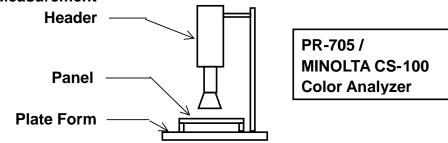


#### **APPENDIX 2: MEASUREMENT APPARATUS**

#### A. LUMINANCE/COLOR COORDINATE

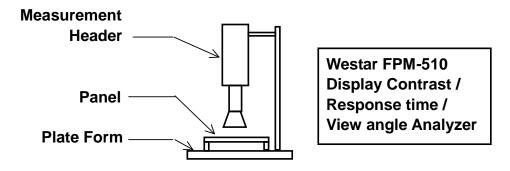
PHOTO RESEARCH PR-705, MINOLTA CS-100





#### B. CONTRAST / RESPONSE TIME / VIEW ANGLE

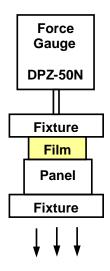
WESTAR CORPORATION FPM-510



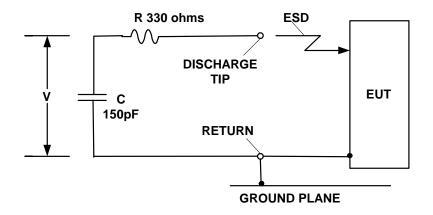




#### **C. PEEL STRENGTH**



#### D. ESD ON AIR DISCHARGE MODE







#### **APPENDIX 3: PRECAUTIONS**

#### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.