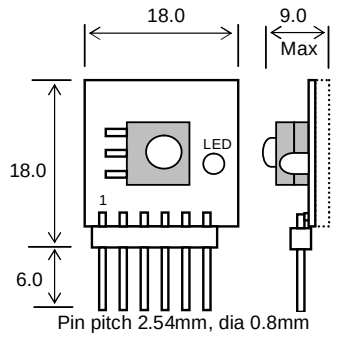
IR Receiver Module KBR38A-1 / KBR38A-2



Pin pitch 2.54mm, dia 0.8mm

SPI Master/Slave / I2C <1MHz clock
Async CMOS / RS232 / RS485
9600, 19200 and 38400 baud.
Single 5V supply at 13mA
LED shows Caps Lock & key press
User setup stored in EEPROM
ASCII / Raw data output modes.

The KBC38A-1 has SPI, Async CMOS, RS232, RS485 and Port toggle interfaces. The KBC38A-2 has SPI, I2C and Port toggle interfaces. Use the KBC56A keyboard to set up the operating mode of the KBR38A or send the equivalent RC5 Raw data codes.

Electrical Parameter	Symbol	Value	Condition
Power Supply Voltage	V_{DD}	5.0VDC +/- 5%	G_{ND}=0V
Power Supply Current	I_{DD} (typ)	13mA + LED 2mA	V_{DD}=5VDC
Logic Input (not /RESET)	V_{IL} / V_{IH}	0.8VDC max / 2.0VDC min	V_{DD}=5VDC
Logic Output	V_{OL} / V_{OH}	0.5VDC max / 2.4VDC min	I_{OH}=-2mA

The /RESET input halts the CPU below 1/3 VDD and initializes above 2/3 VDD.

Environmental Parameter	Value
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +85°C
Operating Humidity	20 to 85% RH @ 25°C non condensing

OUTPUT MODES - Press CTRL then ALT then SHIFT then *Key*	KBRVer	Key
Asynchronous serial 9600 baud – idle high – CMOS	1	A
Asynchronous serial 19200 baud – idle high – CMOS [1]	1	B
Asynchronous serial 38400 baud – idle high – CMOS	1	C
Asynchronous serial 9600 baud – idle low – pseudo RS232	1	D
Asynchronous serial 19200 baud – idle low – pseudo RS232	1	E
Asynchronous serial 38400 baud – idle low – pseudo RS232	1	F
SPI synchronous slave clk input with data clocked on rising edge [2]	1 & 2	G
SPI synchronous slave clk input with data clocked on falling edge	1 & 2	H
I2C with address 71H	2	I
Asynchronous serial 9600 baud – differential – RS485	1	J
Asynchronous serial 19200 baud – differential – RS485	1	K
Asynchronous serial 38400 baud – differential – RS485	1	L
SPI synchronous master clk output with data clocked on rising edge	1 & 2	M
SPI synchronous master clk output with data clocked on falling edge	1 & 2	N
3 Port Toggle – After power ON or /Reset ports are set to low output	1 & 2	O
Enable host busy handshaking or set /SS in SPI master	1 & 2	P
Disable host busy handshaking or set /STRB in SPI master (default)	1 & 2	Q

[1] default mode for KBC38A-1. [2] default mode for KBC38A-2.

DECODE OPTIONS - Press CTRL then ALT then SHIFT then *Key*	KBRVer	Key
No decoding – outputs Raw RC5 command (00h – 38h)	1 & 2	R
No decoding – outputs Raw RC5 system (00h – 1Fh)	1 & 2	S
KBC56A keyboard ASCII decoding (default)	1 & 2	T
KBC56A offset RAW code SHIFT=+40h, ALT=+80h, CTRL=+C0h	1 & 2	U

CTRL, ALT and SHIFT are pressed before a single alternate character. CTRL then ALT or CTRL then SHIFT enable ALT or SHIFT Lock which is cancelled using CTRL. When lock is on, ALT or SHIFT can be used to input a related alternate character. A 16 byte buffer allows the host system to poll the receiver every 2 seconds or to use the IRQ generated by a key press when using I2C or hardware controlled asynchronous modes. When the buffer is empty the data read is FFH in slave SPI or I2C modes and this can be modified using SIN after the first byte in slave SPI mode. Data bytes are 8 bits with asynchronous data adding 1 stop bit and no parity bit.

Data Decode Table (Hex)						
Key	Std	Shift	Lock	ALT	CTRL	Raw
ESC	1B	01	1B	02	80	00
TAB	03	04	03	05	81	01
INS	06	0E	06	0F	83	03
DEL	7F	10	7F	11	82	02
▲ PUp	0B	12	0B	13	84	04
◄HME	08	14	08	15	85	05
► END	09	16	09	17	86	06
▼ PDn	0A	18	0A	19	87	07
? ¥ /	3F	9C	3F	2F	88	08
* € \	2A	9D	2A	5C	89	09
(£ [	28	9B	28	5B	8A	0A
) $]	29	24	29	5D	8B	0B
1 @	31	40	31	Hex	8C	0C
2 &	32	26	32	Hex	8D	0D
3 <	33	3C	33	Hex	8E	0E
4 >	34	3E	34	Hex	8F	0F
5 %	35	25	35	Hex	90	10
6 +	36	2B	36	Hex	91	11
7 -	37	2D	37	Hex	92	12
8 =	38	3D	38	Hex	93	13
9 ~	39	7E	39	Hex	94	14
0 #	30	23	30	Hex	95	15
a A	61	41	41	Hex	96	16
b B	62	42	42	Hex	97	17
c C	63	43	43	Hex	98	18
d D	64	44	44	Hex	99	19
e E	65	45	45	Hex	9A	1A
f F	66	46	46	Hex	9B	1B
g G	67	47	47	1C	9C	1C
h H	68	48	48	1D	9D	1D
i I	69	49	49	1E	9F	1F
j J	6A	4A	4A	1F	A0	20
k K	6B	4B	4B	E0	A1	21
l L	6C	4C	4C	E1	A2	22
m M	6D	4D	4D	E2	A3	23
n N	6E	4E	4E	E3	A4	24
o O	6F	4F	4F	E4	A5	25
p P	70	50	50	E5	A6	26
q Q	71	51	51	E6	A7	27
r R	72	52	52	E7	A8	28
s S	73	53	53	F0	A9	29
t T	74	54	54	F1	AA	2A
u U	75	55	55	F2	AB	2B
v V	76	56	56	F3	AC	2C
w W	77	57	57	F4	AD	2D
x X	78	58	58	F5	AE	2E
y Y	79	59	59	F6	AF	2F
z Z	7A	5A	5A	F7	B0	30
' ! "	27	21	27	22	B1	31
, ; |	2C	3B	2C	B2	B2	32
. : °	2E	3A	2E	F8	B3	33
Space	20	5F	20	07	B4	34
Ctrl	See application page 2 for specific functionality when these keys are pressed.					35
Alt						36
Shift						37
Enter	0D	0D	0C	00	B8	38

In Master SPI mode the /SS is low during data out and /STRB is toggled low for 1us after data is clocked out. The KBR38A-2 slave I2C interface comprises a start condition, fixed address 71H, 8 bit data and stop condition.
Please see the KBR38A application notes on page 2 for timing and circuit ideas.

PIN	Async	RS232*	RS485	SPI Slave	SPI Master	TogON	TogOFF	I2C
1	VDD	VDD	VDD	VDD	VDD	VDD		VDD
2	TOUT	TXD	+A	CLK IN	CLK OUT	Key I	Key Q	SCL
3	0V	0V	0V	0V	0V	0V		0V
4	HostBsy	/HostBsy	-B	SOUT	DOUT	Key H	Key P	/IRQ
5	/RESET	/RESET	/RESET	/RESET	/RESET	/RESET		/RESET
6	/IRQ	IRQ	IRQ	SIN	/SS-/STRB	Key G	Key O	SDA

*The RS232 interface operates between 0V and 5V. Do not connect pins 2, 4 and 6 to RS232 signals which exceed these values.

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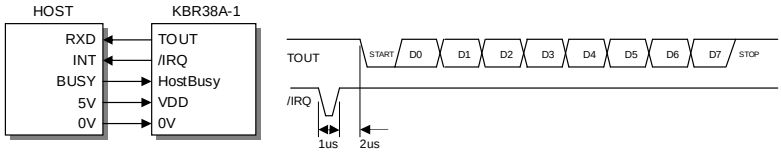
Functions of CTRL, ALT and SHIFT keys when in decode option T (KBC56A decoding – default mode)
In all decode modes if the CTRL, ALT and SHIFT keys are pressed in sequence the next key (A-U) sets, and stores in EEPROM, output mode / decode options. All other functions of these keys are described in the following table.

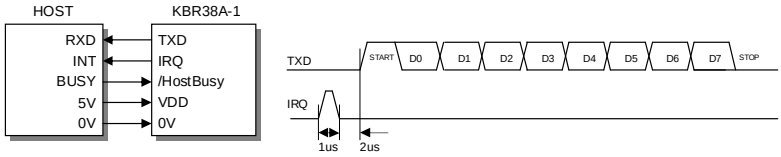
Existing State	New Key Press			
	Normal	**CTRL**	**ALT**	**SHIFT**
Normal	Keyboard character	CTRL on	ALT on	SHIFT on
CTRL	Raw RC5 + 80h (once only)	CTRL off	ALT Lock	SHIFT Lock
ALT	Blue characters / HEX entry	ALT off	No action	ALT off, SHIFT on
SHIFT	Red characters / upper case	SHIFT off	SHIFT off, ALT on	No action
ALT Lock	ALT continuous	ALT Lock off	Normal (once only)	SHIFT once
SHIFT Lock	SHIFT continuous	SHIFT Lock off	ALT once	Normal (once only)

In KBC56A decode mode, HEX entry can be used to send any value from 00h to FFh by pressing the ALT key followed by the 2 HEX digits. In all output and decode modes a key starts to auto repeat after holding it down for 1 second. A 16 byte FIFO buffer holds unread key presses. If Host Busy is enabled (output option P) in async CMOS or RS232 output modes and Host Busy is high (low in RS232), key presses are stored in the buffer but not sent. IRQ still activates to indicate key presses. When this buffer is full, further key presses are discarded. In raw decode modes (R and S), the CTRL, ALT and SHIFT keys have no special function except to change mode.

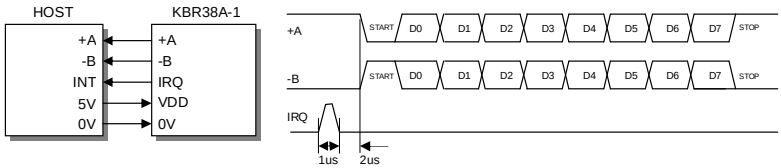
Async serial (CMOS, idle high) – A, B, C
Data is sent asynchronously from TOUT. Baud rate is 9600, 19200 or 38400. Before the start bit is transmitted /IRQ goes low for approximately 1us. Host Busy must be low to enable transmission.



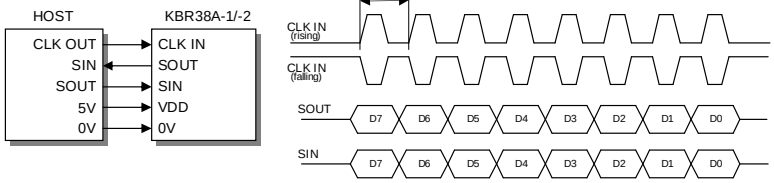
Async serial (pseudo RS232, idle low) – D, E, F
Data is sent asynchronously from TXD. Baud rate is 9600, 19200 or 38400. Before the start bit is transmitted IRQ goes high for approximately 1us. Host Busy must be high to enable transmission. Do not connect to a serial port where higher output voltages than 5V or lower than 0V are present.



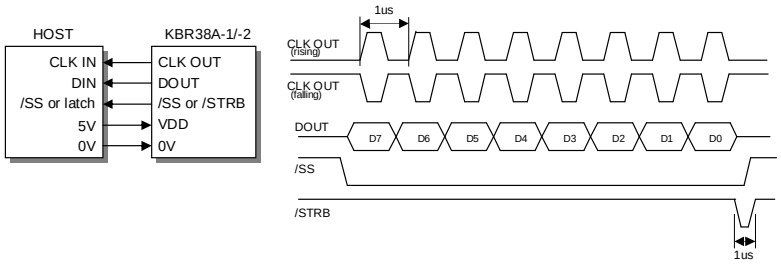
Asynchronous serial (RS485, differential) – J, K, L
Data is sent asynchronously from +A and -B. Baud rate is 9600, 19200 or 38400. Before the start bit is transmitted IRQ goes high for approximately 1us.



SPI slave – G, H
The host must drive CLK IN to shift data out of SOUT. If there is no data in the buffer the value returned will match the value clocked in on SIN (if this is left disconnected FFh will be returned). Data is sent MSB first.



SPI master – M, N
Data is clocked out on the rising or falling edge of CLK OUT. Data is sent MSB first. If /SS is enabled (P), the /SS-/STRB line will be idle high and go low while clocking data. If /STRB is enabled (Q), the /SS-/STRB line will idle high and will go low for approximately 1us after the byte is clocked out. It is recommended to reset the host system after changing SPI mode as an extra clock pulse can be generated.



I2C slave – I (KBR38A-2)
Data is clocked out in slave transmit mode. The host must start the transfer with a start condition. Then the fixed address of 71h is sent with R/W set high. The KBR38A-2 then responds with an ACK/NACK bit. The host must then issue 8 further clocks to clock data out. The host must then send an ACK on the 9th bit. Finally a stop condition is sent.