

Specification for BTHQ 128064AVD-SRE-06-COG

Version July 2003

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**Specification
of
LCD Module Type
Model No.: COG-BTD12864-01**

1. General Description

- ☞ 128 x 64 Dots STN Positive Yellow Reflective Dot Matrix LCD Module.
- ☞ Viewing Angle: 12 o'clock direction.
- ☞ Driving duty: 1/65 Duty, 1/7 bias.
- ☞ 'Epson' S1D10605D04B (COG) Dot Matrix LCD Driver or equivalent.
- ☞ FPC

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

| Parameter | Specifications | Unit |
|--------------------|---|-------|
| Outline dimensions | 55.6(W) x 70.2(H) x 1.095(D) (Included FPC) | mm |
| Viewing area | 50.60(W) x 31.0(H) | mm |
| Active area | 46.577(W) x 27.697(H) | mm |
| Display format | 128(W) x 64(H) | dots |
| Dot size | 0.349(W) x 0.418(H) | mm |
| Dot spacing | 0.015(W) x 0.015(H) | mm |
| Dot pitch | 0.364(W) x 0.433(H) | mm |
| Weight | Approx. 9 | grams |

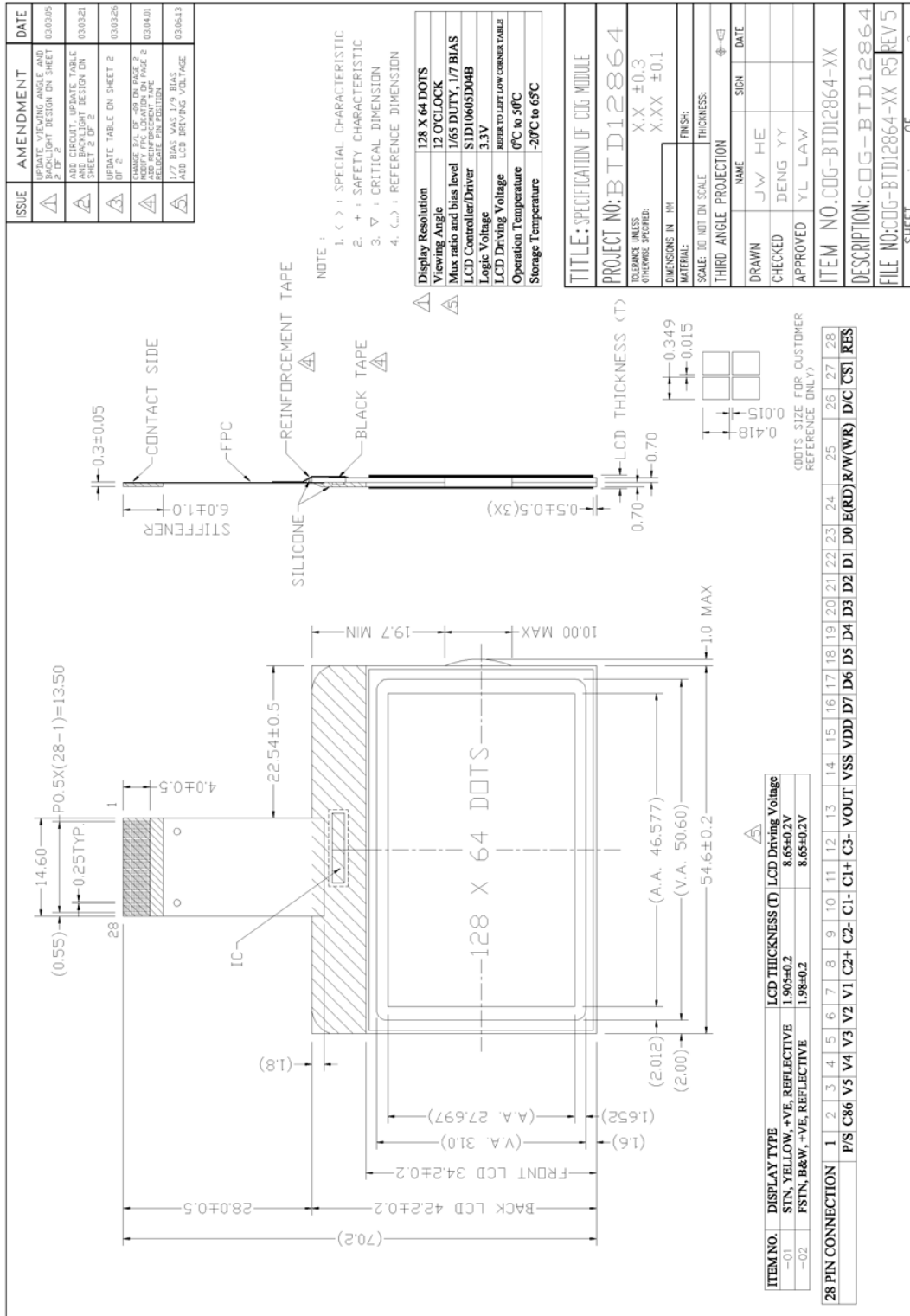


Figure 1: Outline Drawing 1

Downloaded from Elcodis.com electronic components distributor

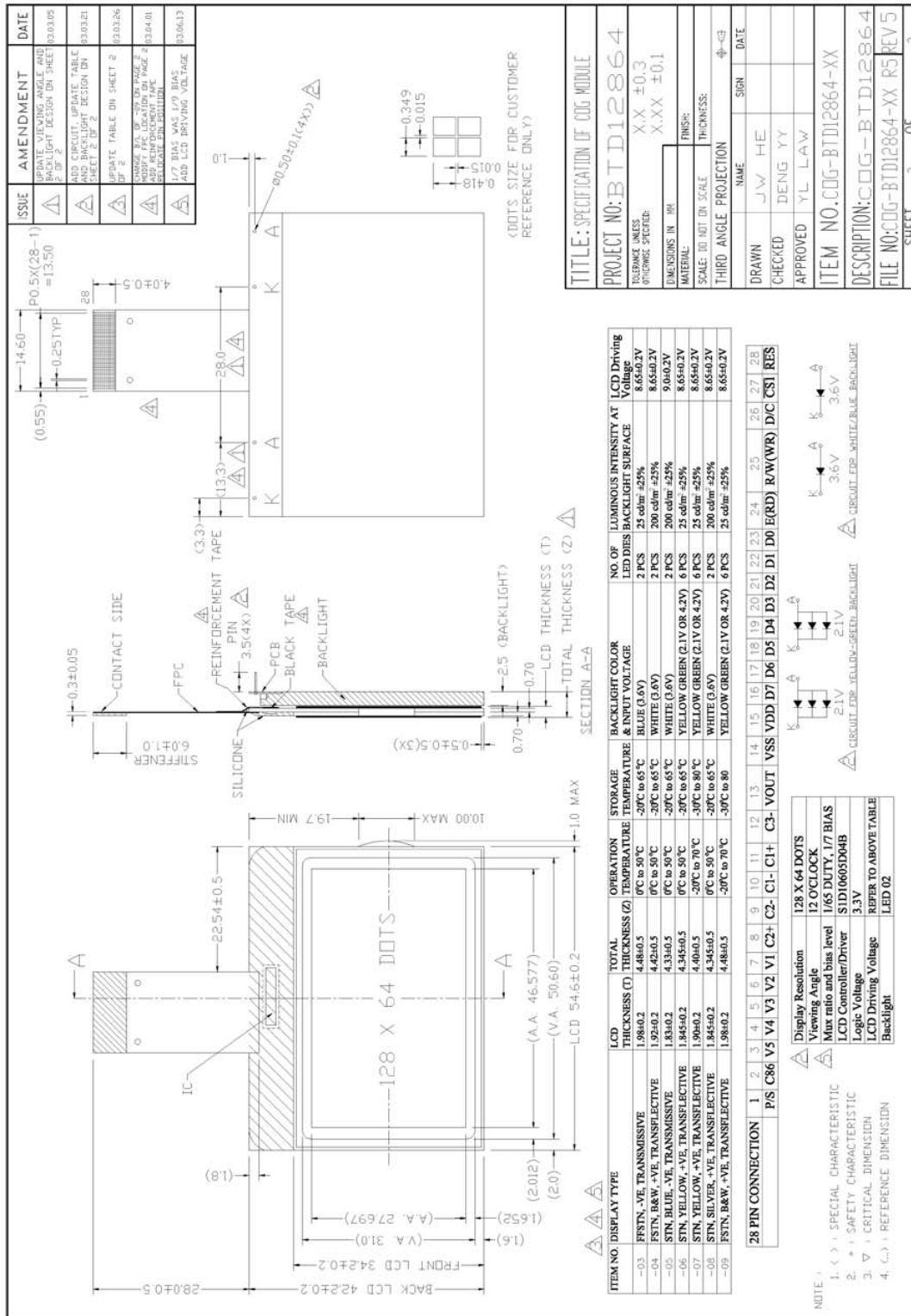


Figure 2: Outline Drawing 2

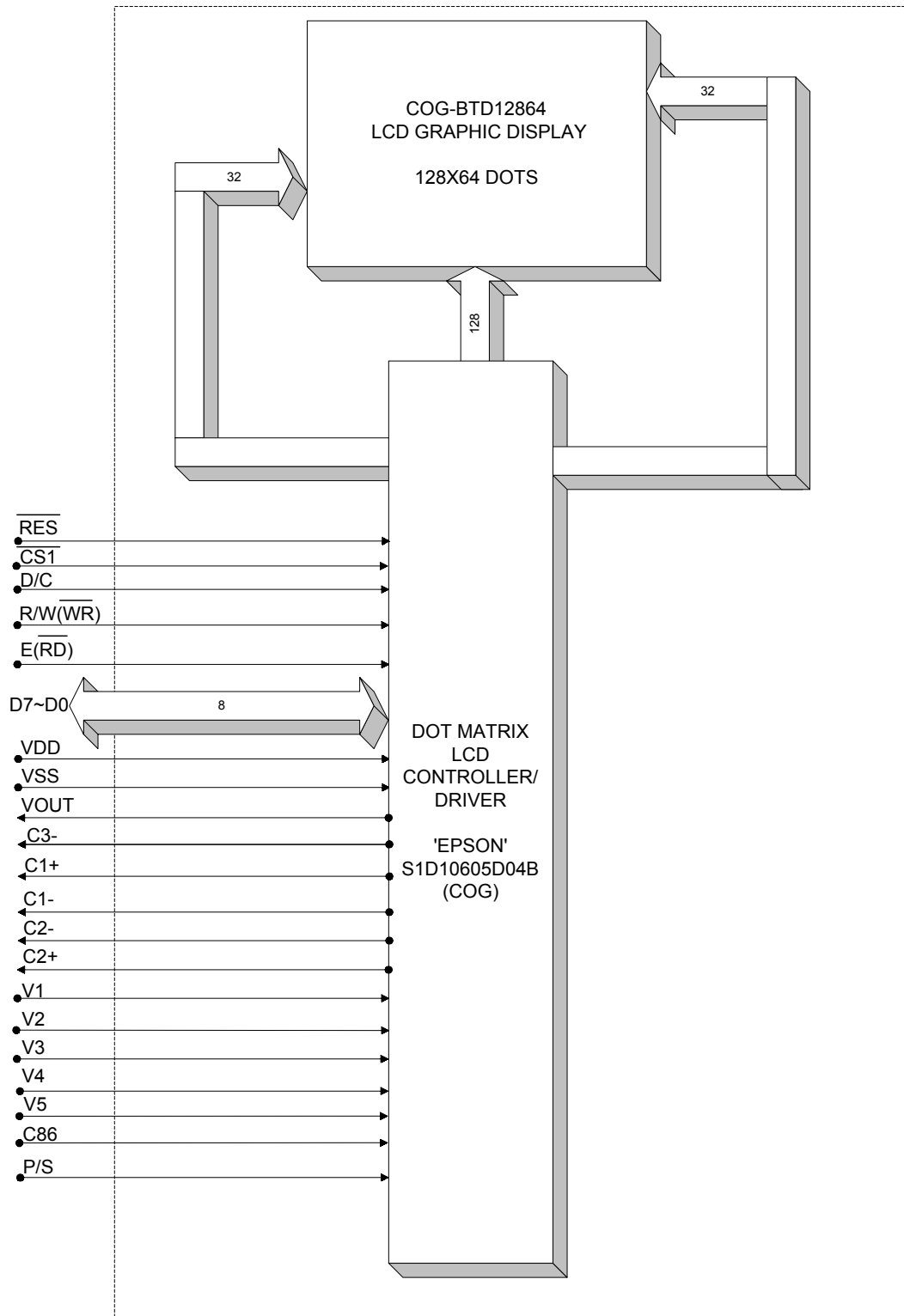


Figure 3: Block Diagram.

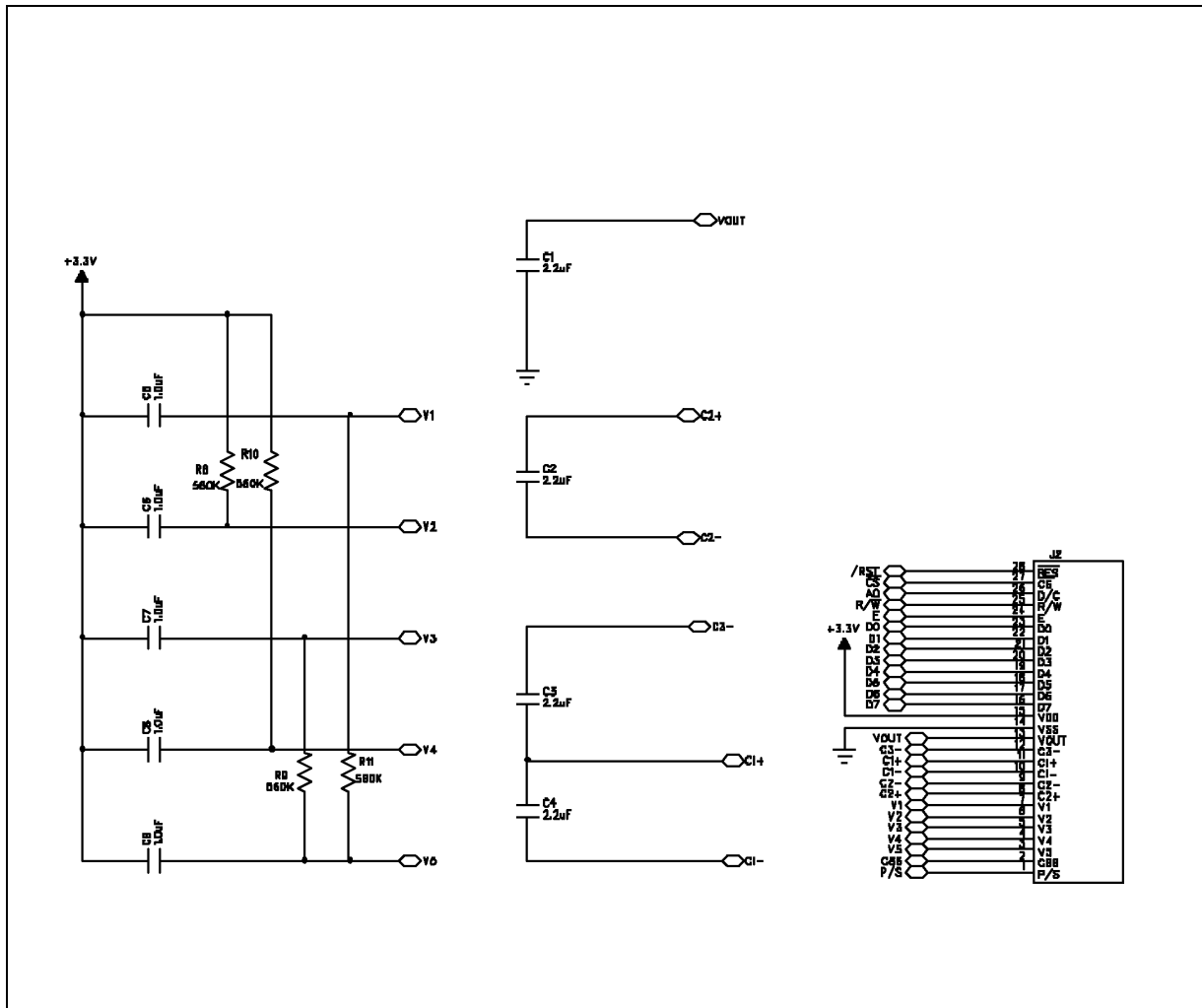


Figure 4: Reference Circuit

3. Interface signals

Table 2(a): Pin Assignment

| Pin No. | Symbol | Description | | | | | | | | | | | | | | | |
|---------|--------------|--|----------------------|--------------|------|------------|--------------|------|---------|----------|----------------------|--|-----|---------|---------|------------|----------|
| 1 | P/S | <p>This is the parallel data input/serial data input switch terminal. P/S = HIGH: Parallel data input. P/S = LOW: Serial data input.</p> <p>The following applies depending on the P/S status:</p> <table border="1"> <thead> <tr> <th>P/S</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>HIGH</td> <td>D/C(A0)</td> <td>D0 to D7</td> <td>\overline{RD}, WR</td> <td></td> </tr> <tr> <td>LOW</td> <td>D/C(A0)</td> <td>SI (D7)</td> <td>Write only</td> <td>SCL (D6)</td> </tr> </tbody> </table> <p>When P/S = <u>LOW</u>, D0 to D5 are HZ. D0 to D5 may be HIGH, LOW or Open. RD(E) and WR(R/W) are fixed to either HIGH or LOW. With serial data input, RAM display data reading is not supported.</p> | P/S | Data/Command | Data | Read/Write | Serial Clock | HIGH | D/C(A0) | D0 to D7 | \overline{RD} , WR | | LOW | D/C(A0) | SI (D7) | Write only | SCL (D6) |
| P/S | Data/Command | Data | Read/Write | Serial Clock | | | | | | | | | | | | | |
| HIGH | D/C(A0) | D0 to D7 | \overline{RD} , WR | | | | | | | | | | | | | | |
| LOW | D/C(A0) | SI (D7) | Write only | SCL (D6) | | | | | | | | | | | | | |
| 2 | C86 | <p>This is the MPU interface switch terminal. C86=HIGH: 6800 Series MPU interface. C86=LOW: 8080 MPU interface.</p> | | | | | | | | | | | | | | | |
| 3 | V5 | This is multi-level power supply for liquid crystal drive. | | | | | | | | | | | | | | | |
| 4 | V4 | <p>Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. VDD (=V0) \geq V1 \geq V2 \geq V3 \geq V4 \geq V5</p> | | | | | | | | | | | | | | | |
| 5 | V3 | | | | | | | | | | | | | | | | |
| 6 | V2 | | | | | | | | | | | | | | | | |
| 7 | V1 | | | | | | | | | | | | | | | | |
| | | <p>Master operation When the power supply turns ON, the internal power supply circuits produce V1 to V4 voltages shown below. The voltage setting are selected using the LCD bias set command.</p> <p>For 1/7 bias: V1=(1/7)xV5, V2=(2/7)xV5, V3=(5/7)xV5, V4=(6/7)xV5.</p> | | | | | | | | | | | | | | | |
| 8 | C2+ | DC/DC voltage converter. Connects a capacitor between this terminal and C2- terminal. | | | | | | | | | | | | | | | |
| 9 | C2- | DC/DC voltage converter. Connects a capacitor between this terminal and C2+ terminal. | | | | | | | | | | | | | | | |
| 10 | C1- | DC/DC voltage converter. Connects a capacitor between this terminal and C1+ terminal. | | | | | | | | | | | | | | | |
| 11 | C1+ | DC/DC voltage converter. Connects a capacitor between this terminal and C1- terminal. | | | | | | | | | | | | | | | |
| 12 | C3- | DC/DC voltage converter. Connects a capacitor between this terminal and C1+ terminal. | | | | | | | | | | | | | | | |
| 13 | VOUT | DC/DC voltage converter. Connects a capacitor between this terminal and VSS. | | | | | | | | | | | | | | | |
| 14 | VSS | 0 V pin connected to the system ground (GND) and this is also the reference power supply for the step-up voltage circuit for the liquid crystal drive. | | | | | | | | | | | | | | | |
| 15 | VDD | Power supply for logic(+3.3V). | | | | | | | | | | | | | | | |

Table 2(b): Pin Assignment

| Pin No. | Symbol | Description |
|---------|---------------------------------|---|
| 16 | D7 | <p>This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus.</p> <p>When the serial interface is selected (P/S = LOW), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.</p> <p>When the chip select is inactive, D0 to D7 are set to high impedance.</p> |
| 17 | D6 | |
| 18 | D5 | |
| 19 | D4 | |
| 20 | D3 | |
| 21 | D2 | |
| 22 | D1 | |
| 23 | D0 | |
| 24 | $\overline{E}(\overline{RD})$ | <p>When connected to an 8080 MPU, this is active LOW. This pin is connected to the \overline{RD} signal of the 8080 MPU, and the S1D15605 series data bus is in an output status when this signal is LOW.</p> <p>When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.</p> |
| 25 | $R/\overline{W}(\overline{WR})$ | <p>When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU \overline{WR} signal. The signals on the data bus are latched at the rising edge of the \overline{WR} signal.</p> <p>When connected to an 6800 Series MPU: This is the read/write control signal input terminal. When R/\overline{W} = HIGH: Read. When R/\overline{W} = LOW: Write.</p> |
| 26 | D/C | <p>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.</p> <p>D/C(A0)="High": Indicates that D0 to D7 are display data. D/C(A0)="Low": Indicates that D0 to D7 are control data.</p> |
| 27 | $\overline{CS1}$ | <p>This is the chip select signal for first chip.</p> <p>When $\overline{CS1}$=LOW and $\overline{CS2}$=HIGH, then the chip select becomes active and the data/commands I/O is enabled.</p> |
| 28 | \overline{RES} | <p>When \overline{RES} is set to LOW, the settings are initialized.</p> <p>The reset operation is performed by the \overline{RES} signal level.</p> |

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 °C)

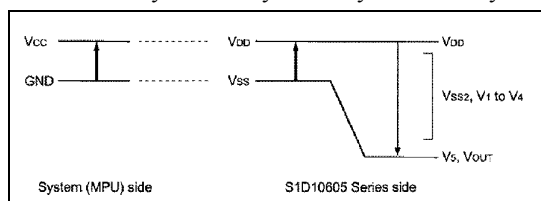
Table 3

| Parameter | Symbol | Min. | Max. | Unit |
|---|-------------|-------|---------|------|
| Power Supply voltage (Logic) | VDD-VSS | -0.3 | +6.0 | V |
| Power Supply voltage(VSS2)(VDD standard) | VSS2 | -4.0 | +0.3 | V |
| Power Supply voltage(V5,VOUT)(VDD standard) | V5,VOUT | -18.0 | +0.3 | V |
| Power Supply voltage(V1,V2,V3,V4)(VDD standard) | V1,V2,V3,V4 | V5 | +0.3 | V |
| Input voltage | Vin | -0.3 | VDD+0.3 | V |

Note: 1.)The VSS2, V1 to V5 and VOUT are relative to the VDD=0V reference.

2.)The V1, V2, V3, and V4 voltages must always satisfy the condition of $VDD \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$.

3.)The modules may be destroyed if they are used beyond the absolute maximum ratings.



4.2 Environmental Condition

Table 4

| Item | Operating Temperature (Topr) | | Storage Temperature (Tstg) | | Remark |
|--|---|-------|----------------------------|-------|-----------------|
| | Min. | Max. | Min. | Max. | |
| Ambient Temperature | 0°C | +50°C | -20°C | +65°C | Dry |
| Humidity | 95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C | | | | no condensation |
| Vibration (IEC 68-2-6) cells must be mounted on a suitable connector | Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction. | | | | 3 directions |
| Shock (IEC 68-2-27) Half-sine pulse shape | Pulse duration : 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes. | | | | 3 directions |

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At $T_a = +25\text{ }^\circ\text{C}$, $V_{DD} = +3.3\pm 5\%$, $V_{SS} = 0\text{V}$.

Table 5

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|--------------------------|--|---------------------|------|---------------------|------|
| Supply voltage (Logic) | V_{DD-VSS} | | 3.14 | 3.3 | 3.47 | V |
| Supply voltage (LCD) (built-in) | $V_{LCD} = V_{DD} - V_5$ | $T_a = 0\text{ }^\circ\text{C}$, Character mode $V_{DD} = +3.3\text{V}$, Note 1 | - | 8.80 | - | V |
| | | $T_a = 25\text{ }^\circ\text{C}$, Character mode $V_{DD} = +3.3\text{V}$, Note 1 | 8.45 | 8.65 | 8.85 | V |
| | | $T_a = 50\text{ }^\circ\text{C}$, Character mode $V_{DD} = +3.3\text{V}$, Note 1 | - | 7.95 | - | V |
| Low-level input signal voltage | V_{ILC} | Note 2 | V_{SS} | - | $0.2 \times V_{DD}$ | V |
| High-level input signal voltage | V_{IHC} | Note 2 | $0.8 \times V_{DD}$ | - | V_{DD} | V |
| Supply Current (Logic & LCD) | IDD | $V_{DD} = +3.3\text{V}$, Note 1, Character mode | - | 0.3 | 0.45 | mA |
| | | $V_{DD} = +3.3\text{V}$, Note 1, Checker board mode | - | 0.5 | 0.75 | mA |

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note 2: A0, D0 to D5, D6(SCL), D7(SI), $\overline{E(RD)}$, $\overline{R(WR)}$, CS1, C86, P/S, \overline{RES} terminals.

5.2 Timing Specifications

System Bus read/Write Characteristics 1 (For the 8080 Series MPU)

At $T_a = 0\text{ }^{\circ}\text{C}$ to $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +3.3\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 6

| Item | Signal | Symbol | Condition | Rating | | Units |
|----------------------------------|-----------------|--------------------|-------------|--------|------|-------|
| | | | | Min. | Max. | |
| Address hold time | A0 | t _{AH8} | | 0 | — | ns |
| Address setup time | A0 | t _{AW8} | | 0 | — | ns |
| System cycle time 1 | A0 | t _{CYCL8} | | 300 | — | ns |
| System cycle time 2 | A0 | t _{CYCH8} | | 300 | — | ns |
| Control LOW pulse width (Write) | \overline{WR} | t _{CCLW} | | 60 | — | ns |
| Control LOW pulse width (Read) | \overline{RD} | t _{CCLR} | | 120 | — | ns |
| Control HIGH pulse width (Write) | \overline{WR} | t _{CCHW} | | 60 | — | ns |
| Control HIGH pulse width (Read) | \overline{RD} | t _{CCHR} | | 60 | — | ns |
| Data setup time | D0 to D7 | t _{DS8} | | 40 | — | ns |
| Data hold time | | t _{DH8} | | 15 | — | ns |
| RD access time | | t _{ACC8} | CL = 100 pF | — | 140 | ns |
| Output disable time | | t _{OH8} | | 10 | 100 | ns |

*1 The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYCL(H)8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leq (t_{CYCL(H)8} - t_{CCLR} - t_{CCHR})$ are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being LOW ($CS2=HIGH$) and \overline{WR} and \overline{RD} being at the LOW level.

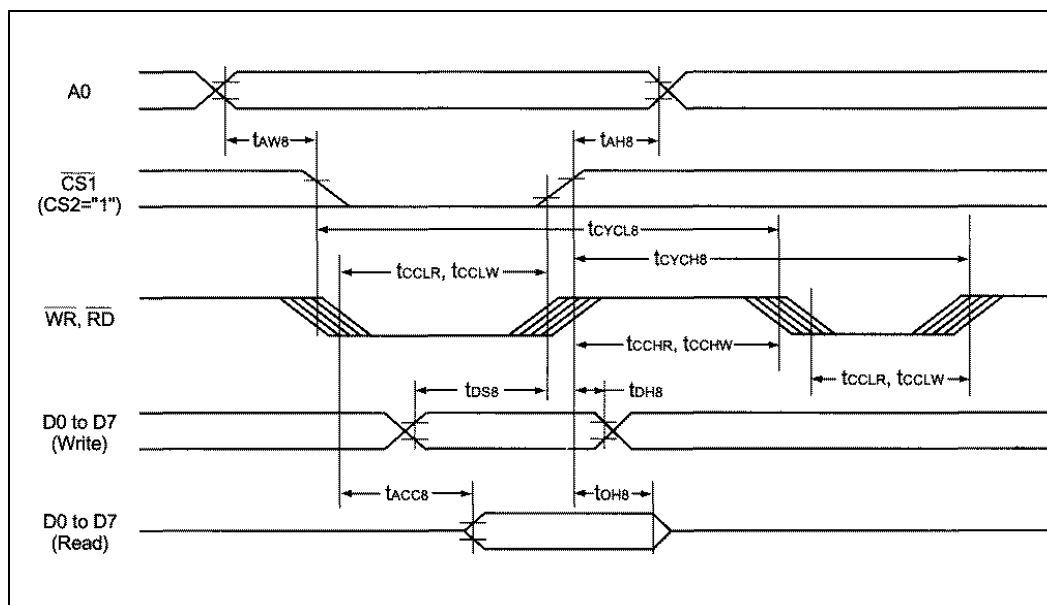


Figure 5: The timing diagram of system bus read/write (For the 8080 Series MPU)

System Bus read/Write Characteristics 2 (For the 6800 Series MPU)

At $T_a = 0\text{ }^{\circ}\text{C}$ to $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +3.3\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 7

| Item | Signal | Symbol | Condition | Rating | | Units |
|------------------------|----------|--------------------|-------------------|--------|------|-------|
| | | | | Min. | Max. | |
| Address hold time | A0 | t _{AH6} | | 0 | — | ns |
| Address setup time | A0 | t _{AW6} | | 0 | — | ns |
| System cycle time 1 | A0 | t _{CYCH6} | | 300 | — | ns |
| System cycle time 2 | A0 | t _{CYCL6} | | 300 | — | ns |
| Data setup time | D0 to D7 | t _{DS6} | CL = 100 pF | 40 | — | ns |
| Data hold time | | t _{DH6} | | 15 | — | ns |
| Access time | | t _{ACC6} | | — | 140 | ns |
| Output disable time | | t _{OH6} | | 10 | 100 | ns |
| Enable HIGH pulse time | Read | E | t _{EWHR} | 120 | — | ns |
| | Write | E | t _{EWHW} | 60 | — | ns |
| Enable LOW pulse time | Read | E | t _{EWLR} | 60 | — | ns |
| | Write | E | t _{EWLW} | 60 | — | ns |

*1 The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leq (t_{CYCH(L)6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leq (t_{CYCH(L)6} - t_{EWLR} - t_{EWHR})$ are specified.

*2 All timing is specified using 20% and 80% for V_{DD} as the reference.

*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being LOW ($CS2=HIGH$) and E.

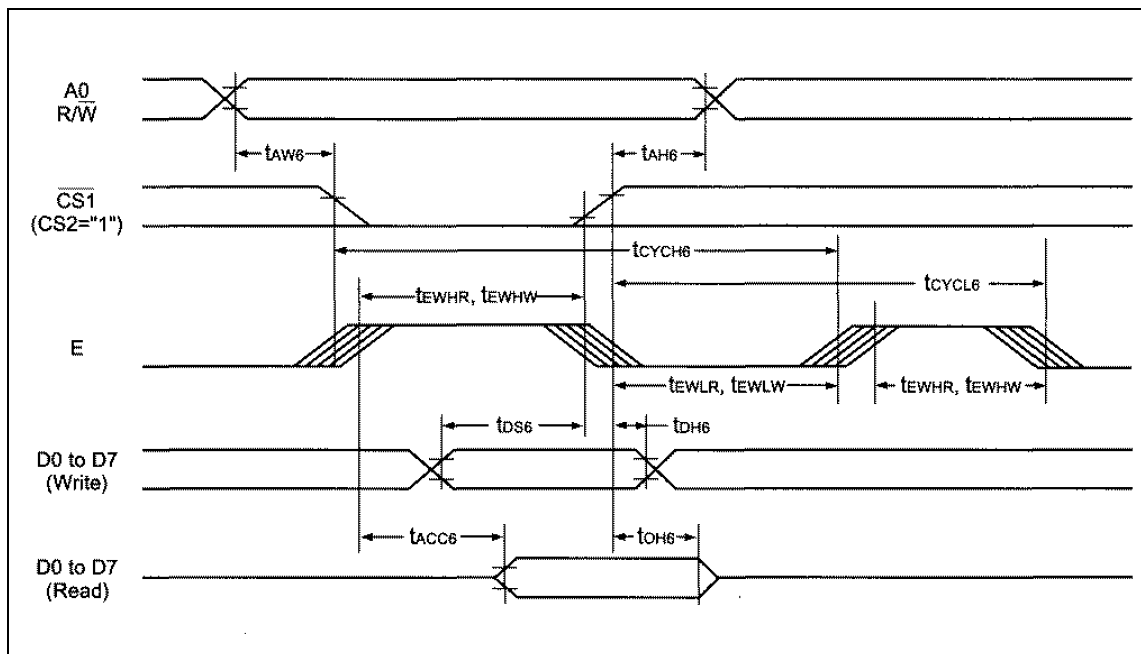


Figure 6: The timing diagram of system bus read/write (For the 6800 Series MPU)

The serial interface

At $T_a = 0\text{ }^{\circ}\text{C}$ to $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +3.3\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 8

| Item | Signal | Symbol | Condition | Rating | | Units |
|----------------------|--------|-------------------|-----------|--------|------|-------|
| | | | | Min. | Max. | |
| Serial Clock Period | SCL | t _{SCYC} | | 250 | — | ns |
| SCL HIGH pulse width | | t _{SHW} | | 100 | — | ns |
| SCL LOW pulse width | | t _{SLW} | | 100 | — | ns |
| Address setup time | A0 | t _{SAS} | | 150 | — | ns |
| Address hold time | | t _{SAH} | | 150 | — | ns |
| Data setup time | SI | t _{SDS} | | 100 | — | ns |
| Data hold time | | t _{SDH} | | 100 | — | ns |
| CS-SCL time | CS | t _{CSS} | | 150 | — | ns |
| | | t _{CSH} | | 150 | — | ns |

Note 1: The input signal rise and fall (tr, tf) are specified at 15ns or less.

Note 2: All timing is specified using 20% and 80% of VDD as the standard.

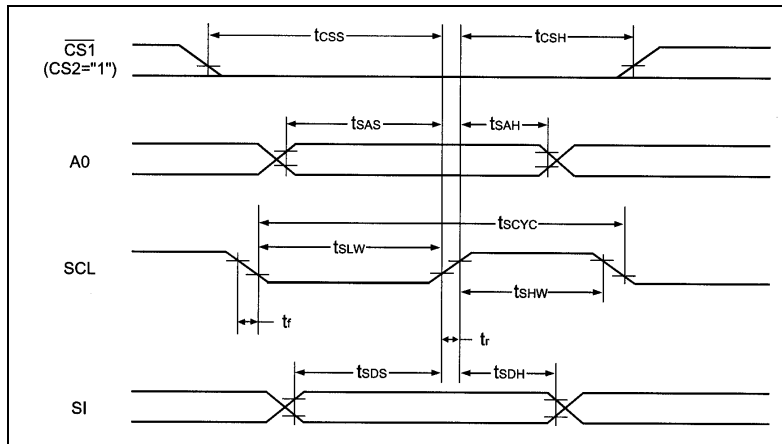


Figure 7: The timing diagram of serial interface

Reset Timing

At $T_a = 0\text{ }^{\circ}\text{C}$ to $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +3.3\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 9

| Item | Signal | Symbol | Condition | Rating | | | Units |
|-----------------------|--------|-----------------|-----------|--------|------|------|-------|
| | | | | Min. | Typ. | Max. | |
| Reset time | | t _R | | — | — | 1 | μs |
| Reset LOW pulse width | RES | t _{rw} | | 1 | — | — | μs |

Note : All timing is specified with 20% and 80% of VDD as the standard.

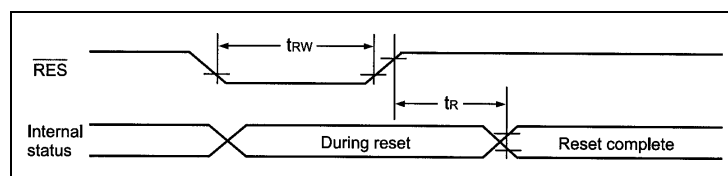


Figure 8: Reset Timing

6. Command Table

Table 10

| Command | Command Code | | | | | | | | | | Function | |
|---|--------------|----|----|------------|----|-------------------------|----|----------------------------------|----------------|----|----------|---|
| | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | D0 |
| (1) Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | LCD display ON/OFF 0: OFF, 1: ON |
| (2) Display start line set | 0 | 1 | 0 | 0 | 1 | Display start address | | | | | 1 | Sets the display RAM display start line address |
| (3) Page address set | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Page address | | | | Sets the display RAM page address |
| (4) Column address set upper bit | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Most significant column address | | | | Sets the most significant 4 bits of the display RAM column address. |
| Column address set lower bit | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Least significant column address | | | | Sets the least significant 4 bits of the display RAM column address. |
| (5) Status read | 0 | 0 | 1 | Status | | | | 0 | 0 | 0 | 0 | Reads the status data |
| (6) Display data write | 1 | 1 | 0 | Write data | | | | | | | 1 | Writes to the display RAM |
| (7) Display data read | 1 | 0 | 1 | Read data | | | | | | | 1 | Reads from the display RAM |
| (8) ADC select | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Sets the display RAM address SEG output correspondence 0: normal, 1: reverse |
| (9) Display normal/reverse | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | Sets the LCD display normal/reverse 0: normal, 1: reverse |
| (10) Display all points ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | Display all points 0: normal display 1: all points ON |
| (11) LCD bias set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Sets the LCD drive voltage bias ratio S1D10605***** 0: 1/9, 1: 1/7 S1D10606***** /S1D10608***** /S1D10609***** ... 0: 1/8, 1: 1/6 S1D10607***** 0: 1/6, 1: 1/5 |
| (12) Read/modify/write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Column address increment At write: +1 At read: 0 |
| (13) End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Clear read/modify/write |
| (14) Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Internal reset |
| (15) Common output mode select | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | * | * | * | Select COM output scan direction 0: normal direction, 1: reverse direction |
| (16) Power control set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Operating mode | | | Select internal power supply operating mode |
| (17) Vs voltage regulator internal resistor ratio set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Resistor ratio | | | Select internal resistor ratio (Rb/Ra) mode |
| (18) Electronic volume mode set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Set the Vs output voltage electronic volume register |
| Electronic volume register set | 0 | 1 | 0 | * | * | Electronic volume value | | | | | | |
| (19) Static indicator ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0: OFF, 1: ON |
| Static indicator register set | 0 | 1 | 0 | * | * | * | * | * | * | * | 1 | Mode Set the flashing mode |
| (20) Power saver | | | | | | | | | | | | Display OFF and display all points ON compound command |
| (21) NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Command for non-operation |
| (22) Test | 0 | 1 | 0 | 1 | 1 | 1 | 1 | * | * | * | * | Command for IC test. Do not use this command |

(Note) *: disabled data