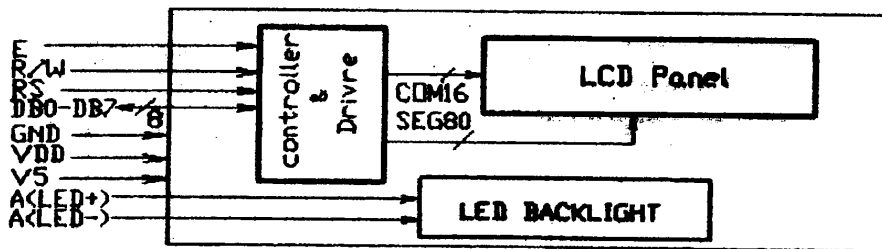


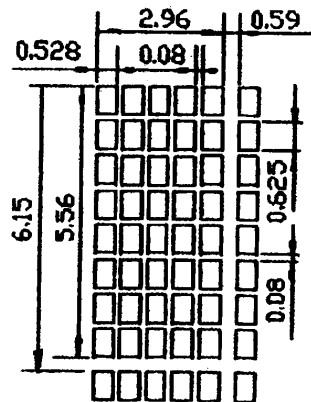
● Block Diagram & DD RAM Address

● Display Pattern



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Line2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

RAM area : 00H — 27H and 40H — 67H
 Note : Please select 2 line display



● Interface Pin Function

Pin No.	Symbol	Level	Function
1	Vss	---	Power Supply 0V +5V for Liquid Crystal driving
2	Vdd	---	
3	Vee	---	
4	Rs	H/L	Register select Hi>Data Input Li:Instruction Input
5	R/W	H/L	Read/Write select Hi>Data Read(Module → MPU) Li>Data Write(Module → MPU)
6	E	H.H-L	Operation start signal for data read/write
7	DB0	H/L	Lower order 4 line data bus with bidirectional three--state. Used for data transfer between the MPU and the module. These four are not used during 4-bit operation.
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	Higher order 4 lines data bus with bidirectional three--state. Used for data transfer between the MPU and the module. DB7 can be used as a BUSY flag
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
*15	A(LED+)	---	Supply Voltage for LED Backlighting
*16	K(LED-)	---	0V(GND)

Note : * marked pin are only for LED backlighting type