

# **Specification for BTHQ 22005VSS-SMN-LED WHITE**

**Version October 2002**

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**Specification  
of  
LCD Module Type  
Item No.: BTHQ 22005VSS-07**

**1. General Description**

- 20 characters (5x8 dots) x 2 lines STN Negative Blue Transmissive Dot Matrix LCD module.
- Viewing Angle: 6 O'clock direction.
- Driving scheme: 1/16 Duty, 1/5 bias.
- 'SAMSUNG' KS0070BP-00CC (Die form) LCD Controller & Driver or equivalent.
- 'SAMSUNG' KS0065B-PCC (Die form) LCD Segment Driver or equivalent.
- White LED05 backlight.

**2. Mechanical Specifications**

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	116.0(W) x 37.0(H) x 14.0 MAX.(D)	mm
Effective viewing area	83.0(W) x 18.6(H)	mm
Display format	20 characters x 2 lines	-
Character size	3.20(W) x 5.55(H) (5 x 8 dots)	mm
Character spacing	0.50(W) x 0.40(H)	mm
Character pitch	3.70(W) x 5.95(H)	mm
Dot size	0.628(W) x 0.681(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.643(W) x 0.696(H)	mm
Weight:	TBD	grams

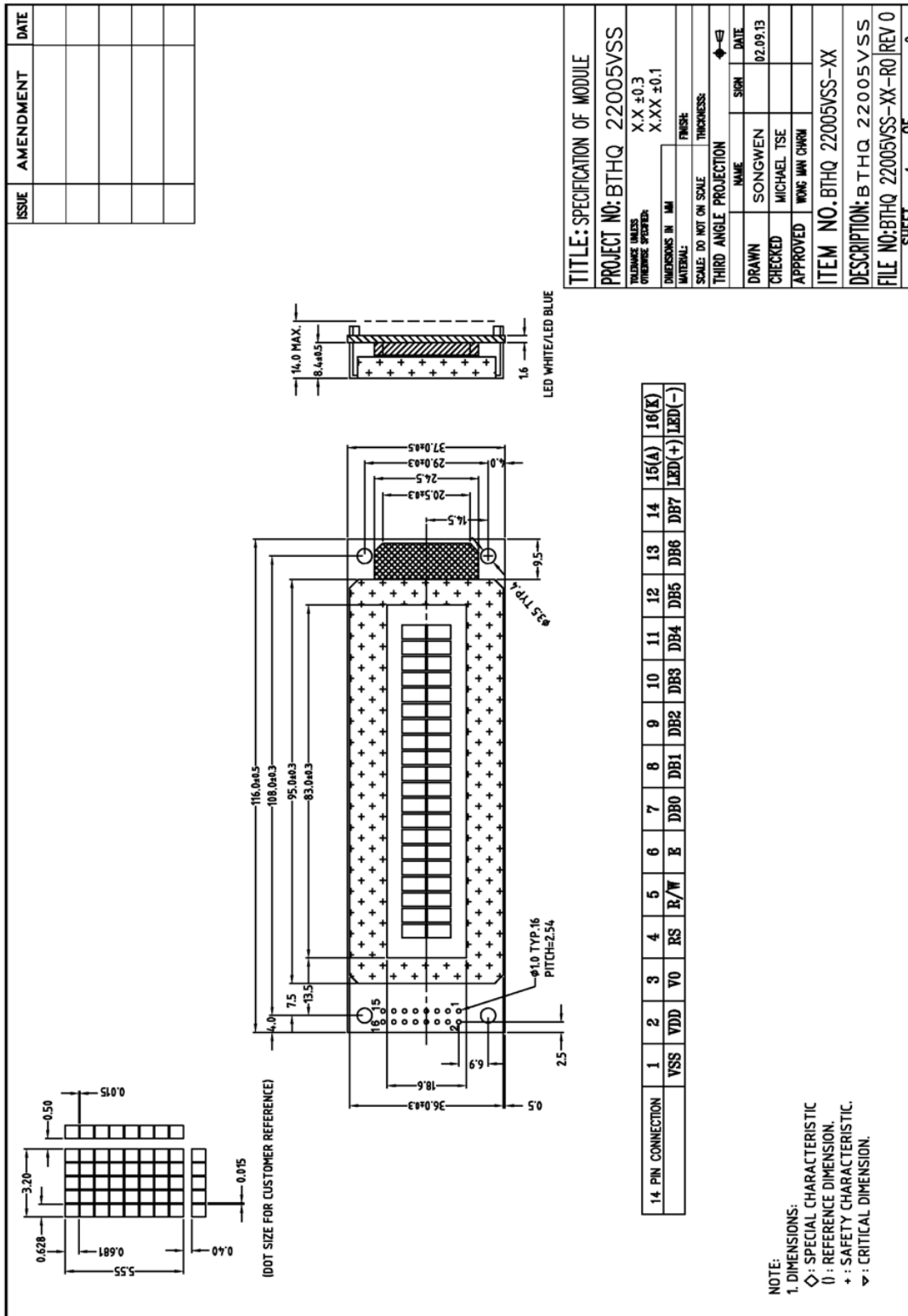


Figure 1: Outline Drawing 1

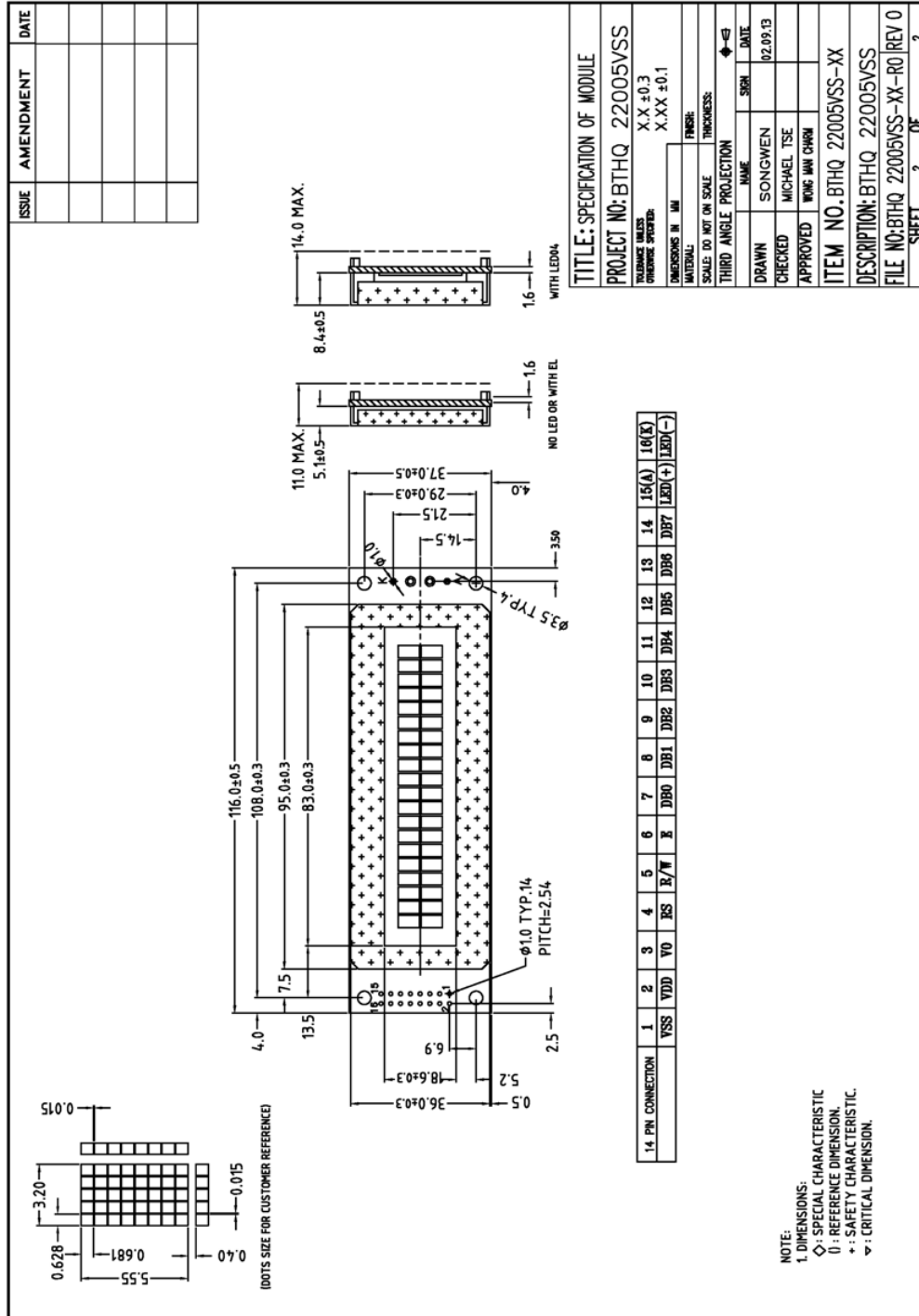


Figure 2: Outline Drawing 2

**3. Interface signals**Table 2

Pin No.	Symbol	Description
1	VSS	Ground(0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: "High" for Data register (for read and write) "Low" for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: " High" for Read mode. "Low" for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15(A)	LED(+)	Anode of LED backlight
16(K)	LED(-)	Cathode of LED backlight

#### 4. Absolute Maximum Ratings

##### 4.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+15.0	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

##### 4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s <sup>2</sup> = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions



## 5. Electrical Specifications

### 5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD =5.0V, Note1.	4.2	4.5	4.8	V
Input signal voltage for E,DB0-DB7,R/W,RS.	V <sub>IH</sub>	"H" level	2.2	-	VDD	V
	V <sub>IL</sub>	"L" level	-0.3	-	0.6	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.0	1.5	mA
		Checker board mode, Note 1	-	1.2	1.8	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.3	0.5	mA
		Checker board mode, Note 1	-	0.3	0.5	mA
Supply voltage of white LED05 backlight	VLED	Forward current =40 mA  Number of LED dies =1x2 =2.	3.2	3.6	4.0	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

## 5.2 Timing Specifications

At  $T_a = 0\text{ }^{\circ}\text{C}$  To  $+50\text{ }^{\circ}\text{C}$  ,  $V_{DD} = +5\text{V} \pm 5\%$  ,  $V_{SS} = 0\text{V}$ .

Refer to Fig. 3, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	$t_C$	500	-	ns	E
E rise time	$t_R$	-	25	ns	E
E fall time	$t_F$	-	25	ns	E
E pulse width (High, Low)	$t_W$	220	-	ns	E
R/W and RS set-up time	$t_{SU1}$	40	-	ns	R/W,RS
R/W and RS hold time	$t_{H1}$	10	-	ns	R/W, RS
Data set-up time	$t_{SU2}$	60	-	ns	DB0-DB7
Data hold time	$t_{H2}$	10	-	ns	DB0-DB7

Refer to Fig. 4, the bus timing diagram for read mode .

Table 7

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	$t_C$	500	-	ns	E
E rise time	$t_R$	-	25	ns	E
E fall time	$t_F$	-	25	ns	E
E pulse width	$t_W$	220	-	ns	E
R/W and RS set-up time	$t_{SU}$	40	-	ns	R/W,RS
R/W and RS hold time	$t_H$	10	-	ns	R/W, RS
Data output delay time	$t_D$	-	120	ns	DB0-DB7
Data hold time	$t_{DH}$	20	-	ns	DB0-DB7

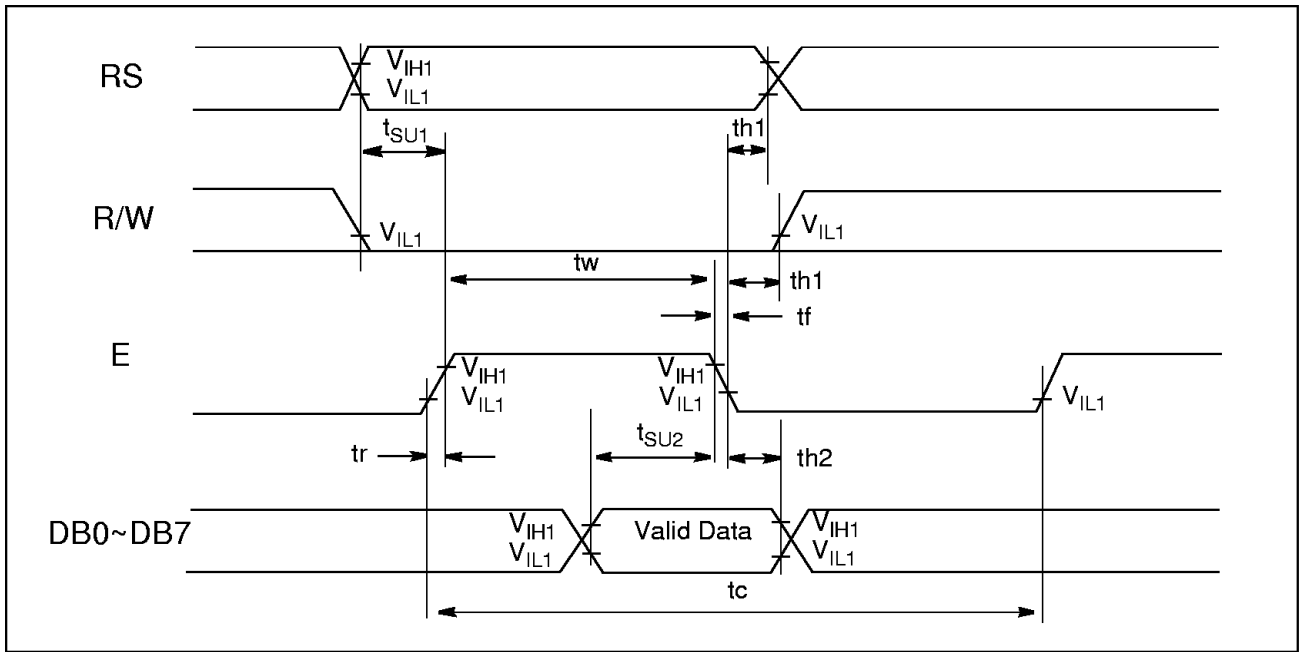


Figure 3: The bus timing diagram for write mode

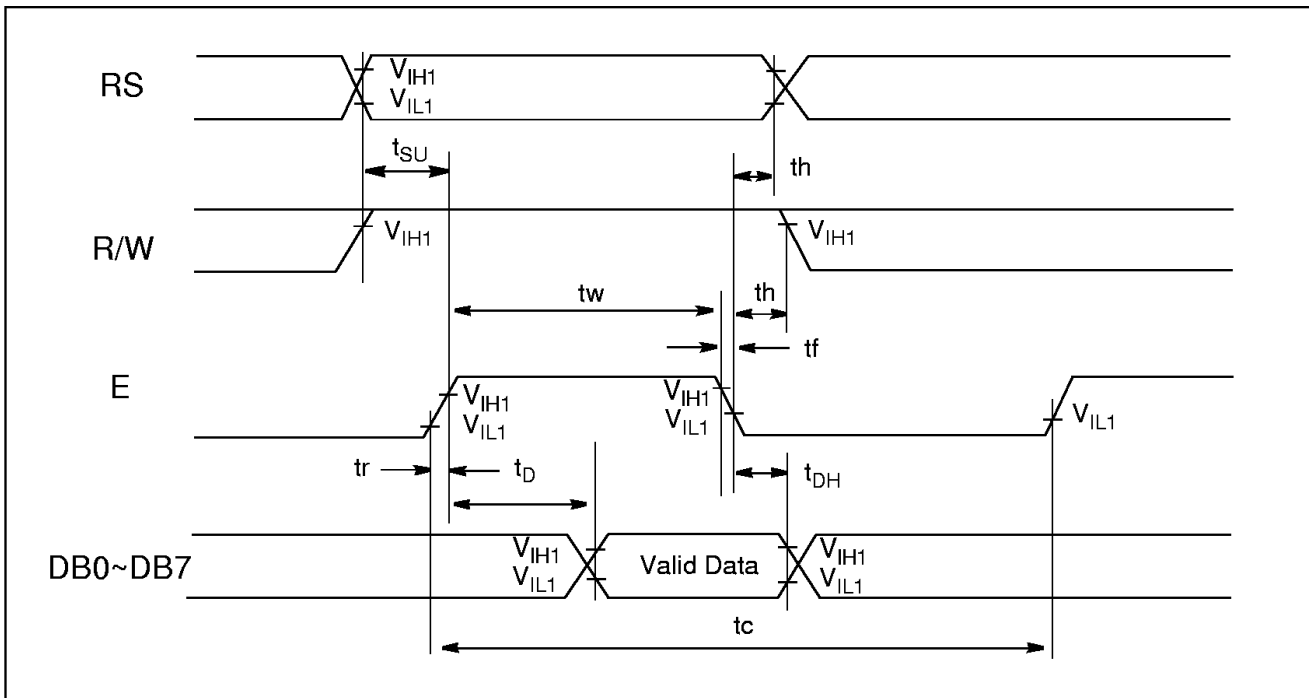


Figure 4: The bus timing diagram for read mode .

### 5.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 5, the timing diagram of VDD against V0.

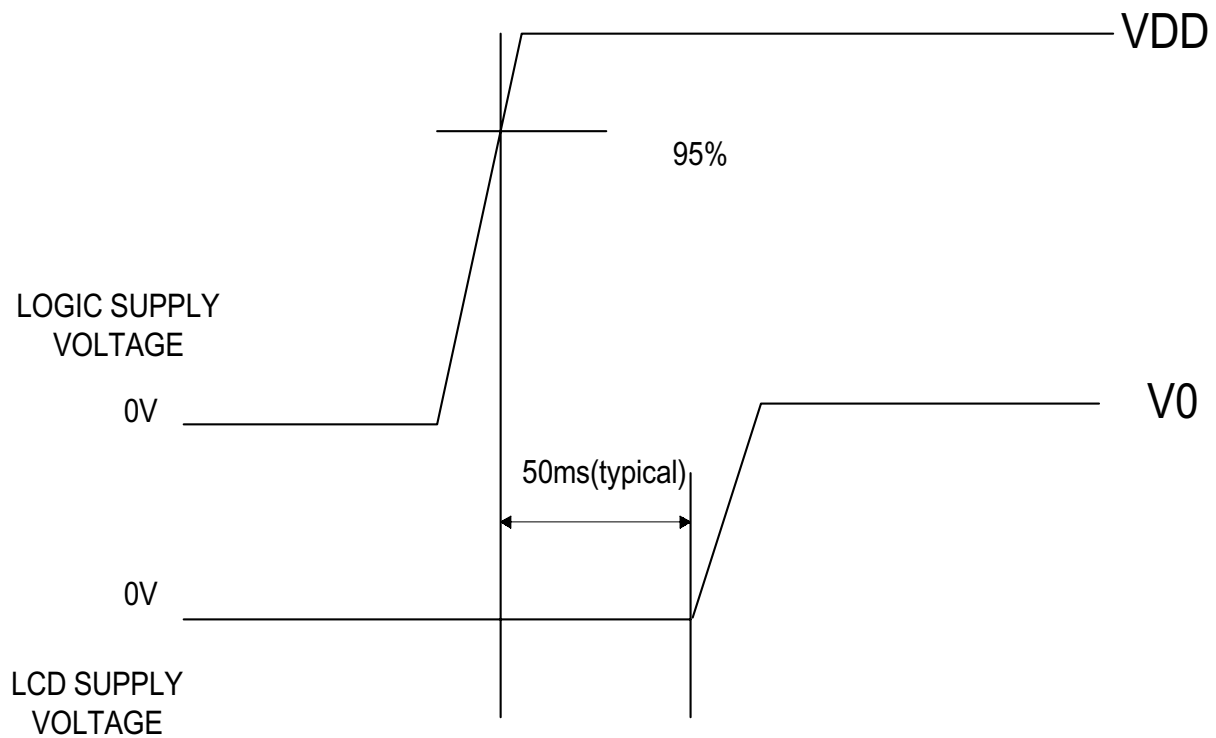


Figure 5: Timing diagram of VDD against V0.

## 6. CGROM Character Code Table

KS0070B-00														
Upper 4bit Lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHH
LLLL	CG RAM (1)													
LLLH	(2)													
LLHL	(3)													
LLHH	(4)													
LHLL	(5)													
LHLH	(6)													
LHHL	(7)													
LHHH	(8)													
HLLL	(1)													
HLLH	(2)													
HLHL	(3)													
HLHH	(4)													
HHLL	(5)													
HHLH	(6)													
HHHL	(7)													
HHHH	(8)													

## 7. APPENDIX

These specifications shall be applied to the White LED-Lamp (LED or LEDs), NSPWF50BS, which is supplied by Nichia Corporation (Nichia).

### 1. SPECIFICATIONS

#### (1) Absolute Maximum Rating

(Ta=25°C)

Item	Symbol	Absolute Maximum Rating	Unit
Forward Current	IF	30	mA
Pulse Forward Current	IFP	100	mA
Reverse Voltage	VR	5	V
Power Dissipation	PD	120	mW
Operating Temperature	Topr	-30 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +100	°C
Lead Soldering Temperature	Tsol	260±5°C for 5sec. (3.0mm from the base of the epoxy bulb)	

IFP Conditions : Pulse Width ≤ 10msec. and Duty ≤ 1/10

#### (2) Initial Electrical/Optical Characteristics

(Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Forward Voltage	VF	IF=20[mA]	—	3.6	4.0	V	
Reverse Current	IR	VR= 5[V]	—	—	50	μA	
Luminous Intensity	Rank S	Iv	IF=20[mA]	300	360	420	mcd
	Rank R	Iv	IF=20[mA]	210	260	300	mcd
	Rank Q	Iv	IF=20[mA]	150	180	210	mcd

※ One delivery will include three different ranks of products. The quantity-ratio of the three ranks is decided by Nichia.  
Measurement Uncertainty of the Luminous Intensity : ±10%

#### Color Ranks

(IF=20mA, Ta=25°C)

Rank a				
x	0.250	0.250	0.290	0.290
y	0.205	0.250	0.305	0.260

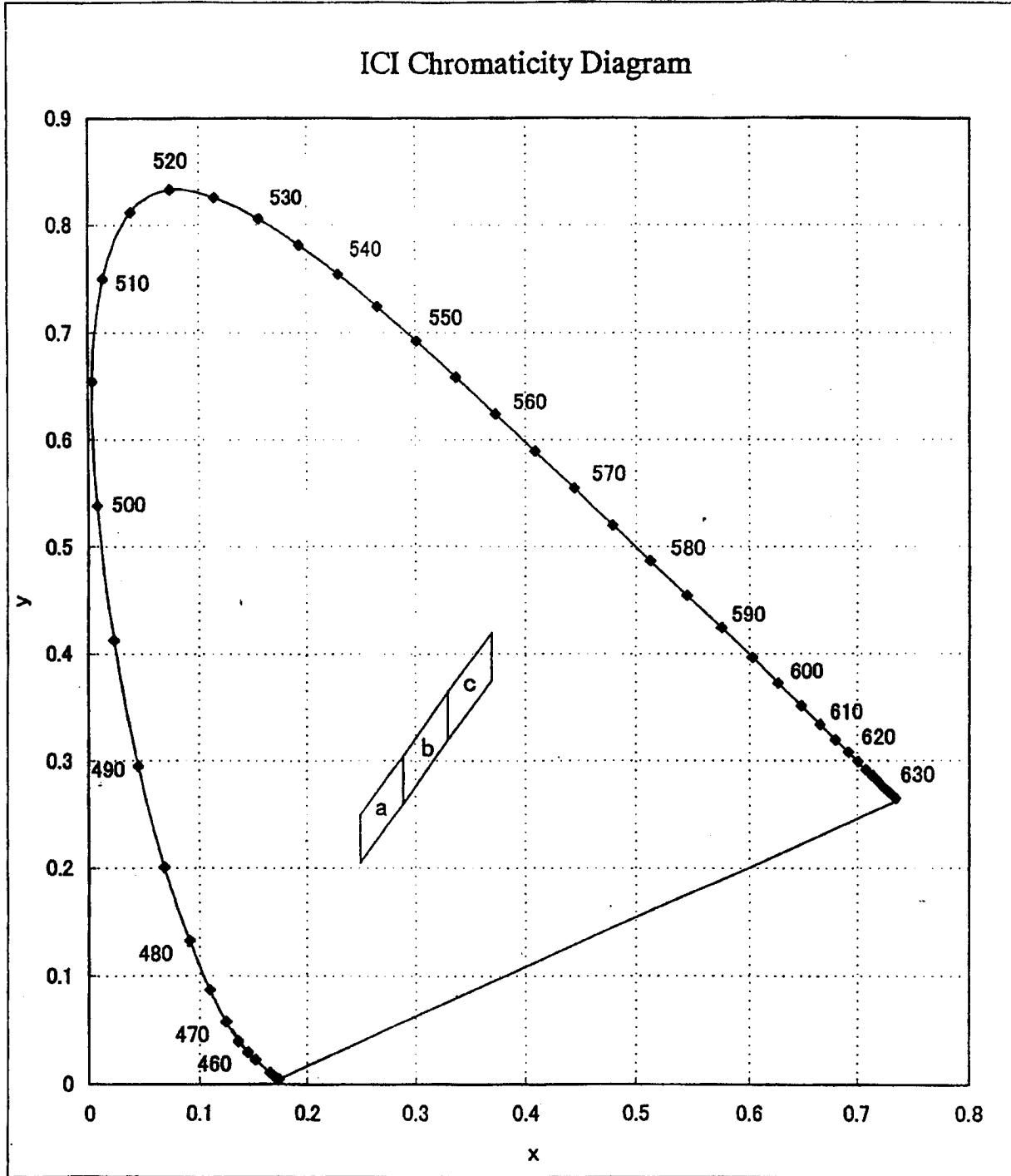
Rank b				
x	0.290	0.290	0.330	0.330
y	0.260	0.305	0.365	0.320

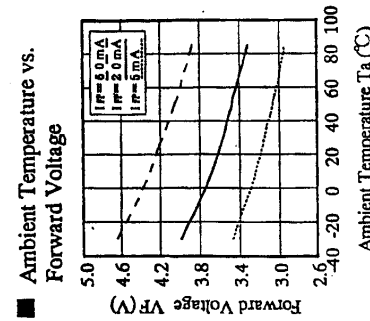
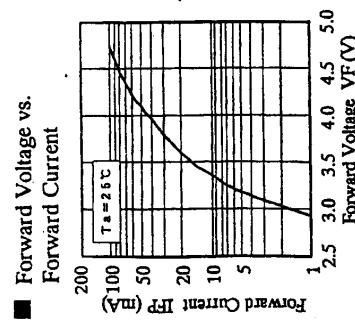
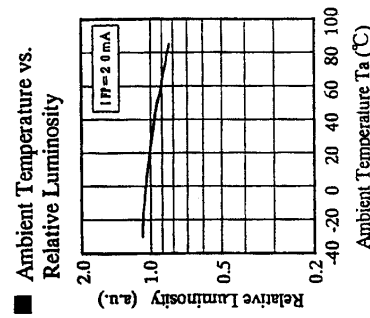
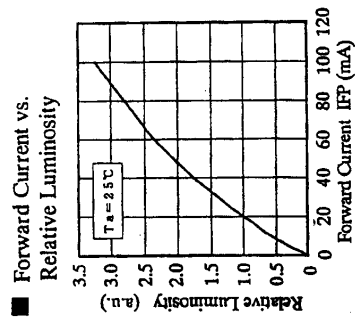
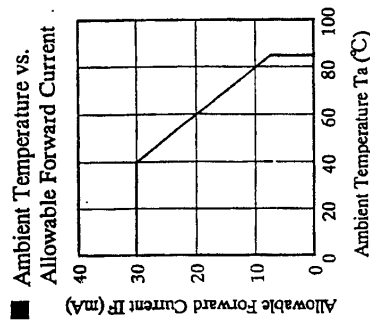
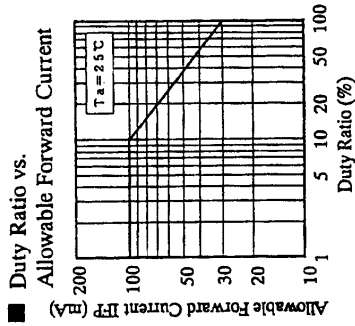
Rank c				
x	0.330	0.330	0.370	0.370
y	0.320	0.365	0.420	0.375

※ One delivery will include the consecutive two ranks of products.  
The quantity-ratio of the two ranks is decided by Nichia.  
Measurement Uncertainty of the Color Coordinates : ±0.02

### 2. TYPICAL INITIAL OPTICAL/ELECTRICAL CHARACTERISTICS

Please refer to figures No.STLZ-A906042, No.STLZ-A801473.



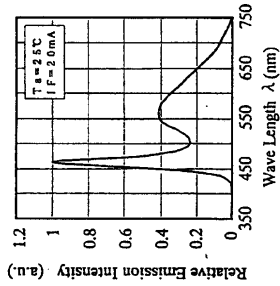


Rev.1	Section	Approve	Check	Draw
Rev.2	ST	Bando	Yanaseki	Tamura
Rev.3	Date	Jun.1,1999		
Rev.4	Model	NSPWxxxx		
<b>NICHIA CORPORATION</b>				
Title TYP.CHARACTERISTICS				
				No. STLZ-A906042

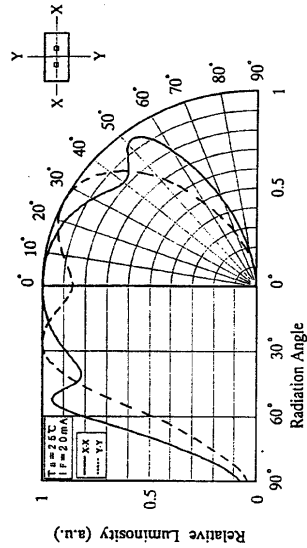




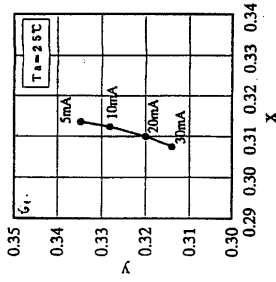
■ Spectrum



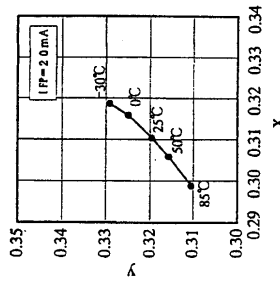
■ Directivity (NSPWF50BS)



■ Forward Current vs. Chromaticity diagram



■ Ambient Temperature vs. Chromaticity diagram



Rev.1	Section	Approve	Check	Draw
Rev.2	ST	<i>Bando</i>	<i>Yamada</i>	<i>Sareya</i>
Rev.3	Date	Jun.1.1999		
Rev.4	Model	NSPWF50BS		
NICHIA CORPORATION		Title TYP.CHARACTERISTICS		
		No. STLZ-A801473		