

Specification for BT 21605VSS-SRE-HQ

Version July 2003

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A	B	2003.07.30	(Based on Test Specification VL-TS-BTHQ 21605VSS-XX REV. D 2003-05-31). Item 1 to 4 were updated: 1) Module specification drawing was updated to the newest version. 2) Supply current of checkerboard mode were added. 3) CGROM Character Code Table was added. 4) Timing Diagram of VDD against V0 was updated.	SUNNY LEE	HE ZUO BING

CONTENTS

	<u>Page No.</u>
1. GENERAL DESCRIPTION	4
2. MECHANICAL SPECIFICATIONS	4
3. ABSOLUTE MAXIMUM RATINGS	7
3.1 ELECTRICAL MAXIMUM RATINGS (Ta=25°C)	7
3.2 ENVIRONMENTAL CONDITION	7
4. ELECTRICAL SPECIFICATIONS	8
4.1 INTERFACE SIGNALS	8
4.2 TYPICAL ELECTRICAL CHARACTERISTICS	9
4.3 TIMING SPECIFICATIONS	10
4.4 TIMING DIAGRAM OF VDD AGAINST V0	13
5. CGROM CHARACTER CODE TABLE	14

**Specification
of
LCD Module Type
Item No.: BTHQ 21605VSS-01**

1. General Description

- 16 characters (5 x 8 dots) x 2 lines STN Positive Yellow Reflective LCD Character Module.
- Viewing Angle: 6 o'clock direction.
- Driving scheme: 1/16 duty, 1/5 bias.
- 'SAMSUNG' KS0070BP-00CC (Die form) LCD Controller & Driver or equivalent.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1(b) and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	84.0(W) x 44.0(H) x 10.0 MAX.(D)	mm
Effective viewing area	61.0(W) x 15.8(H)	mm
Display format	16 characters x 2 lines	-
Character size	2.95(W) x 5.55(H) (5 x 8 dots)	mm
Character spacing	0.60(W) x 0.40(H)	mm
Character pitch	3.55(W) x 5.95(H)	mm
Dot size	0.578(W) x 0.681(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.593(W) x 0.696(H)	mm
Weight	TBD	grams

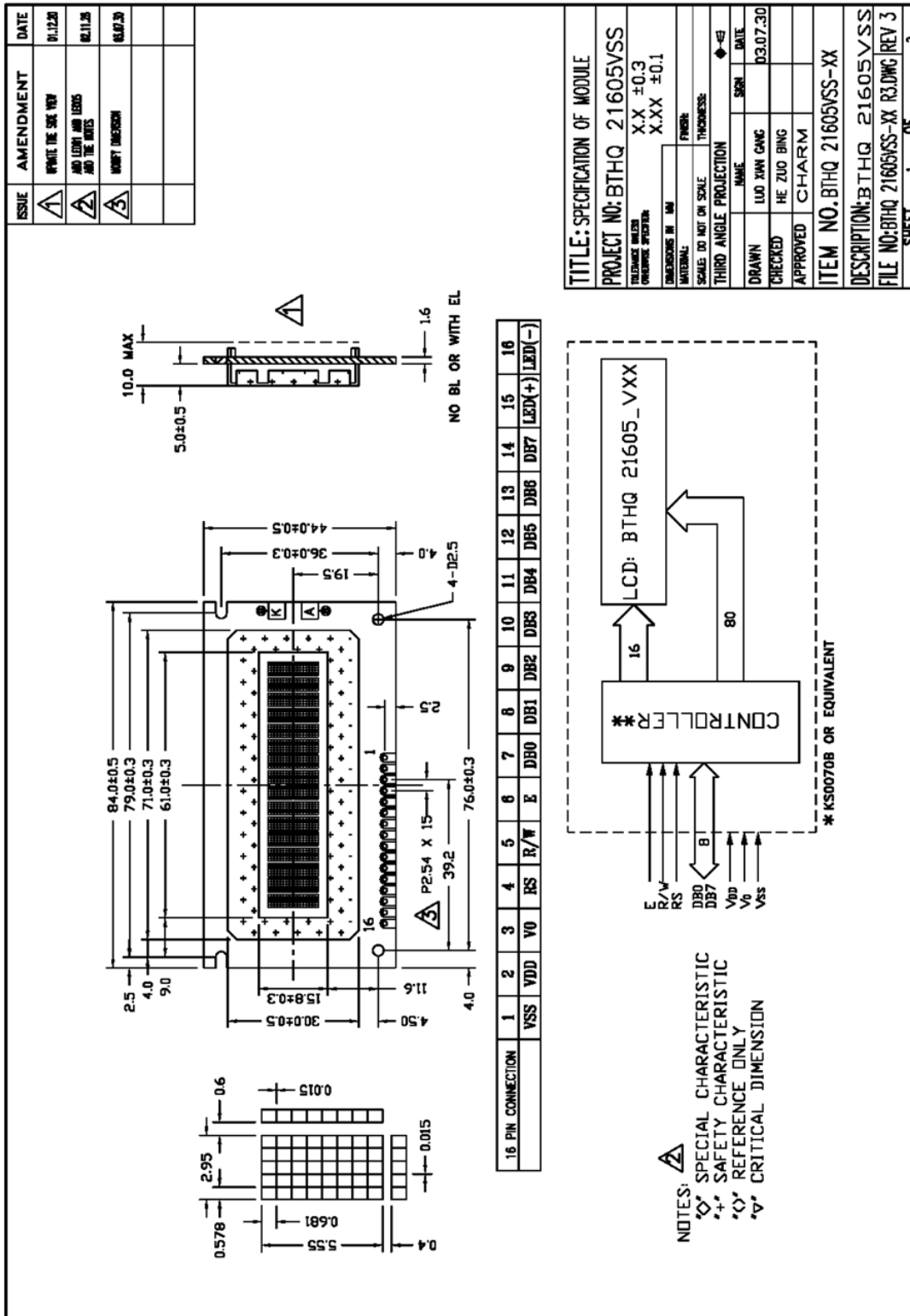


Figure 1(a): Outline Drawing

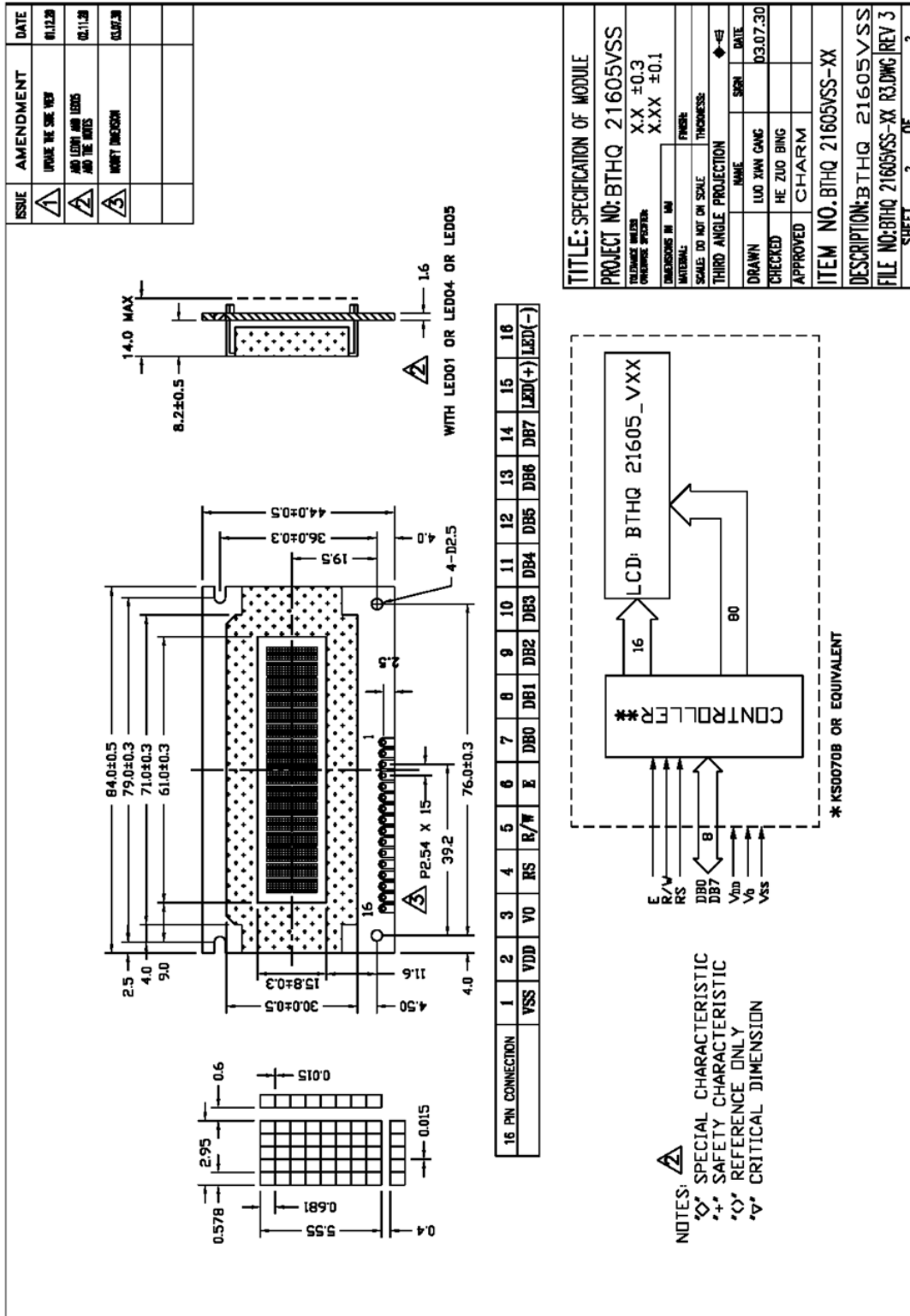


Figure 1(b): Outline Drawing

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+15.0	V
Input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

3.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

4. Interface signalsTable 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: "High" for Data register (for read and write) "Low" for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: "High" for Read mode. "Low" for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15	LED(+)	Anode of LED backlight
16	LED(-)	Cathode of LED backlight

4. Electrical Specifications

4.1 Typical Electrical Characteristics

At $T_a = 25\text{ }^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD = 5V, Note 1	4.1	4.6	5.1	V
Input signal voltage 1	V _{IH1}	“High” level	2.2	-	VDD	V
for E,DB0-DB7,R/W,RS	V _{IL1}	“Low” level	-0.3	-	0.6	V
Input signal voltage 2	V _{IH2}	“High” level	VDD -1.0	-	VDD	V
for OSC1	V _{IL2}	“Low” level	-	-	1.0	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.1	1.7	mA
		Checkerboard mode, Note 1		1.2	1.8	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.2	0.3	mA
		Checkerboard mode, Note 1	-	0.2	0.3	mA

Note 1 : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

4.2 Timing Specifications

At $T_a = 0\text{ }^{\circ}\text{C}$ To $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Refer to Fig. 2, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	t_C	500	-	ns	E
E rise time	t_R	-	25	ns	E
E fall time	t_F	-	25	ns	E
E pulse width (High, Low)	t_W	220	-	ns	E
R/W and RS set-up time	t_{SU1}	40	-	ns	R/W,RS
R/W and RS hold time	t_{H1}	10	-	ns	R/W, RS
Data set-up time	t_{SU2}	60	-	ns	DB0-DB7
Data hold time	t_{H2}	10	-	ns	DB0-DB7

Refer to Fig. 3, the bus timing diagram for read mode.

Table 7

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	t_C	500	-	ns	E
E rise time	t_R	-	25	ns	E
E fall time	t_F	-	25	ns	E
E pulse width	t_W	220	-	ns	E
R/W and RS set-up time	t_{SU}	40	-	ns	R/W,RS
R/W and RS hold time	t_H	10	-	ns	R/W, RS
Data output delay time	t_D	-	120	ns	DB0-DB7
Data hold time	t_{DH}	20	-	ns	DB0-DB7

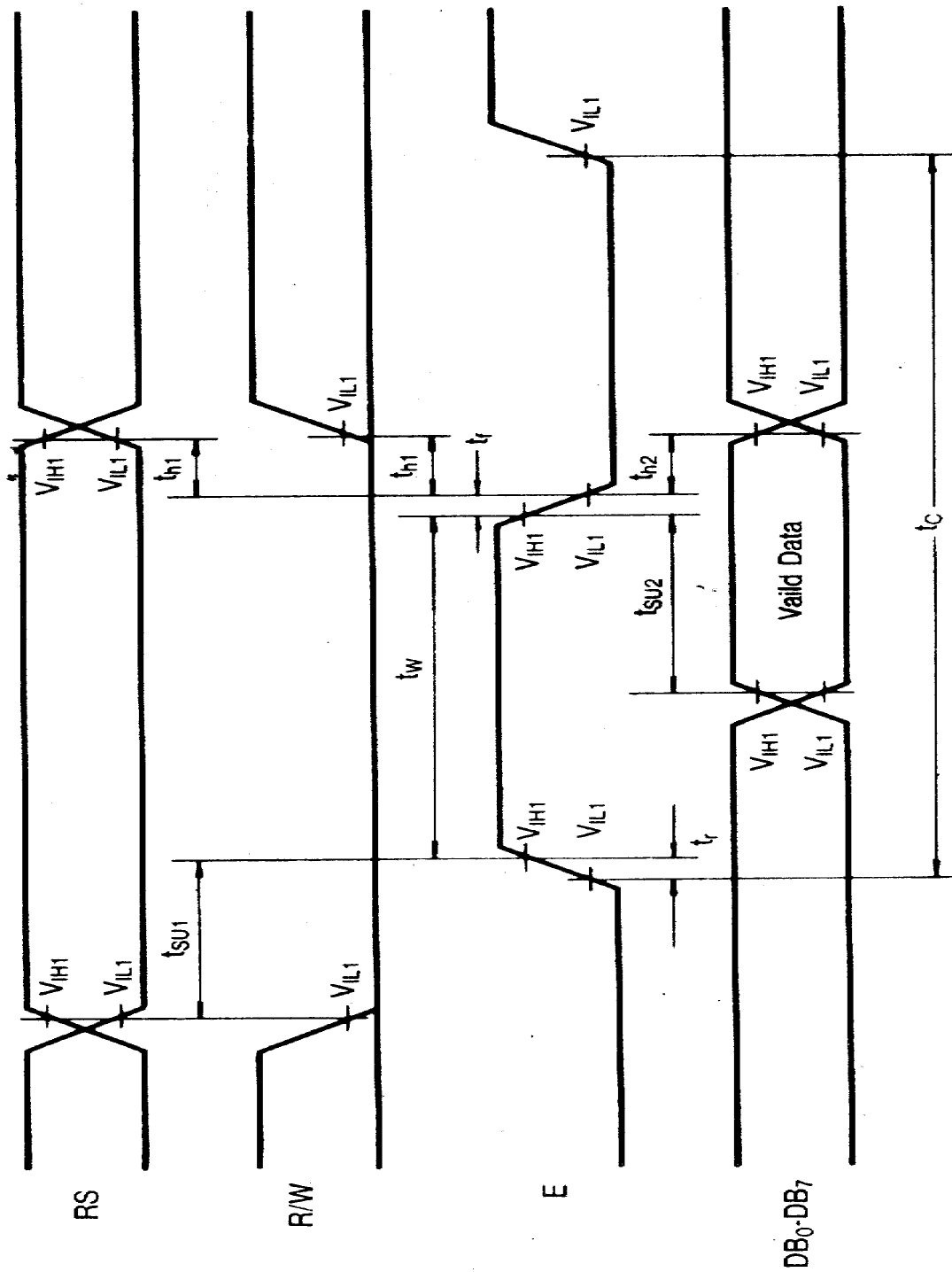


Figure 2: The bus timing diagram for write mode .

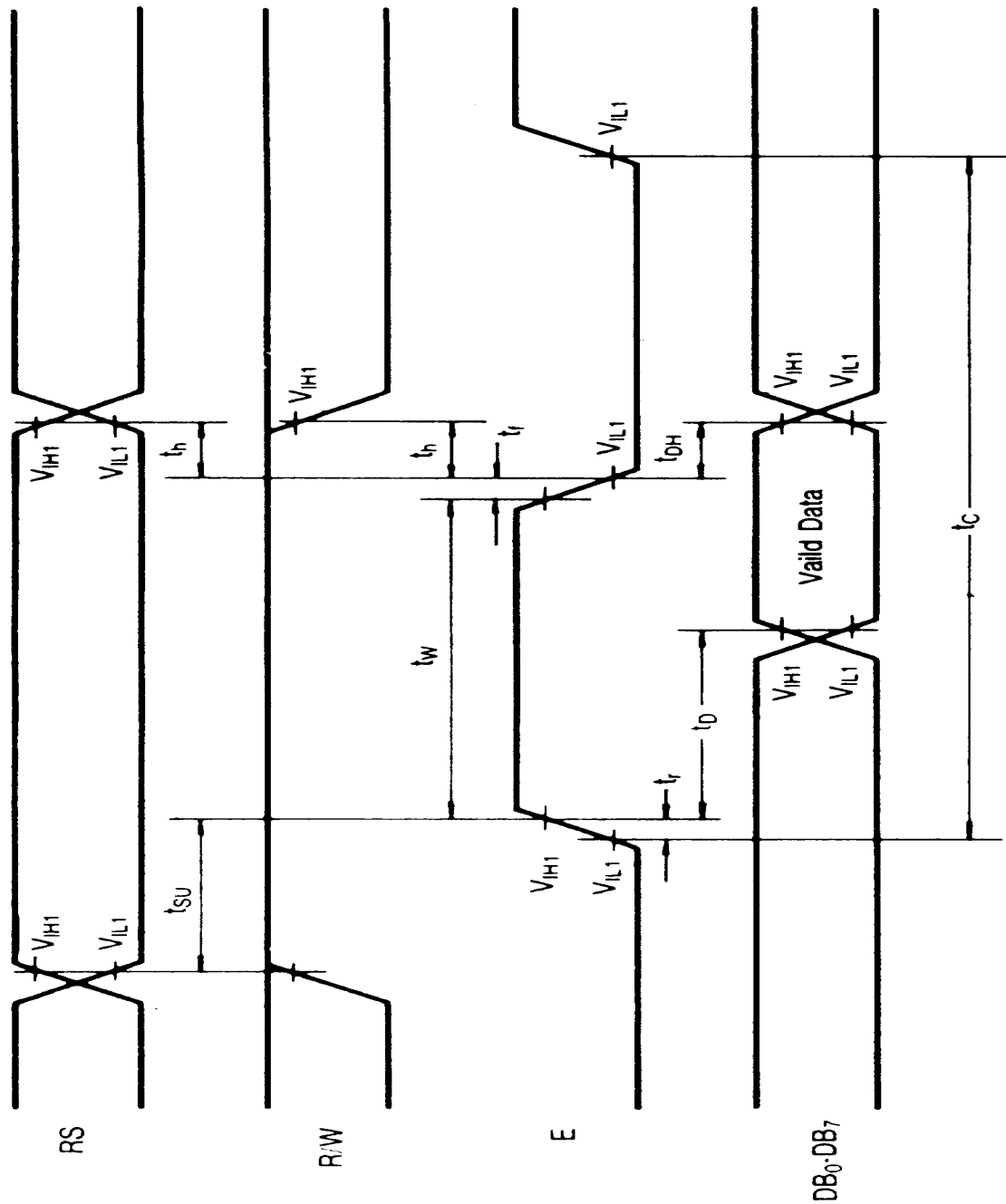


Figure 3: The bus timing diagram for read mode .

4.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

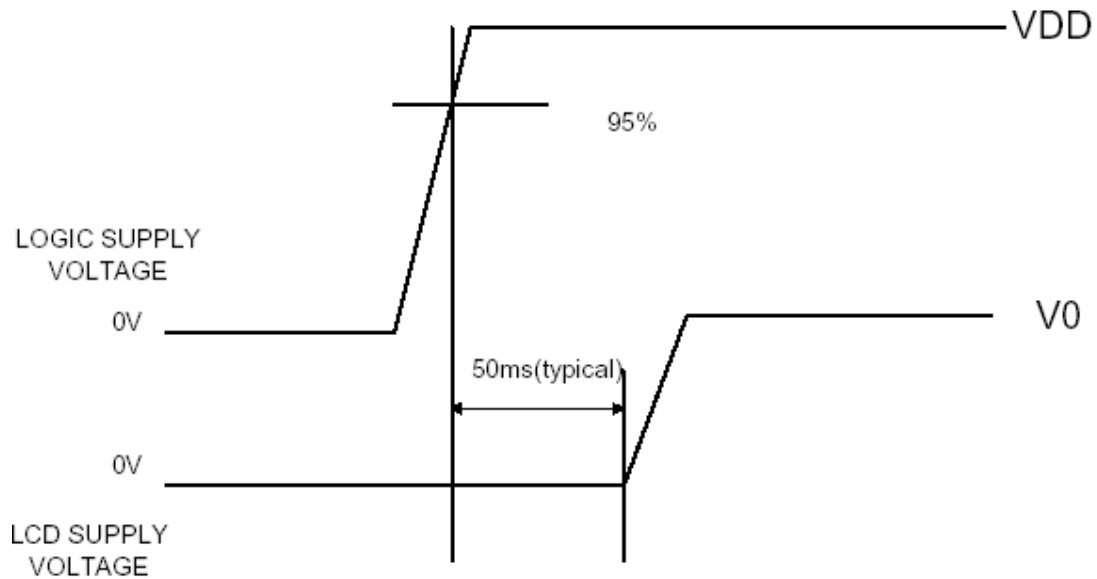


Figure 4: Timing diagram of VDD against V0.

5. CGROM Character Code Table (KS0070B-00)

KS0070B-00															
Upper 4bit Lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
	LLLL	CG RAM (1)													
LLLH	(2)														
LLHL	(3)														
LLHH	(4)														
LHLL	(5)														
LHLH	(6)														
LHHL	(7)														
LHHH	(8)														
HLLL	(1)														
HLLH	(2)														
HLHL	(3)														
HLHH	(4)														
HHLL	(5)														
HHLH	(6)														
HHHL	(7)														
HHHH	(8)														