BATRON

Specification for
BT HQ 21605AV-YETF-LED04-I2C-5V

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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2003.05.23	First release.	SUNNY LEE	WONG MAN CHARM

CONTENTS

Specification
of
LCD Module Type
Model No.: BTHQ 21605AV-02

1. General Description

- 16 characters (5x 8 dots) x 2 lines STN Positive Yellow Transflective LCD Character module.
- Driving scheme: 1:18 multiplexed drive, 1/4 bias.
- Optimal view direction: 6 O'clock.
- Driving IC: 'PHILIPS' PCF2119RU/F2/026 (Die form) LCD controller/driver or equivalent.
- Data interface: I^2C-bus.
- Yellow – green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1(b) and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	84.0(W) x 44.0(H) x 14.0 MAX.(D)	mm
Active area	61.0(W) x 15.8(H)	mm
Display format	16 characters (5x 8 dots) x 2 lines	-
Character size	2.95(W) x 5.553(H)	mm
Character spacing	0.60(W) x 0.394(H)	mm
Character pitch	3.55(W) x 5.947(H)	mm
Dot size	0.578(W) x 0.681(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.593(W) x 0.696(H)	mm
Weight	Approx. 42.0	grams

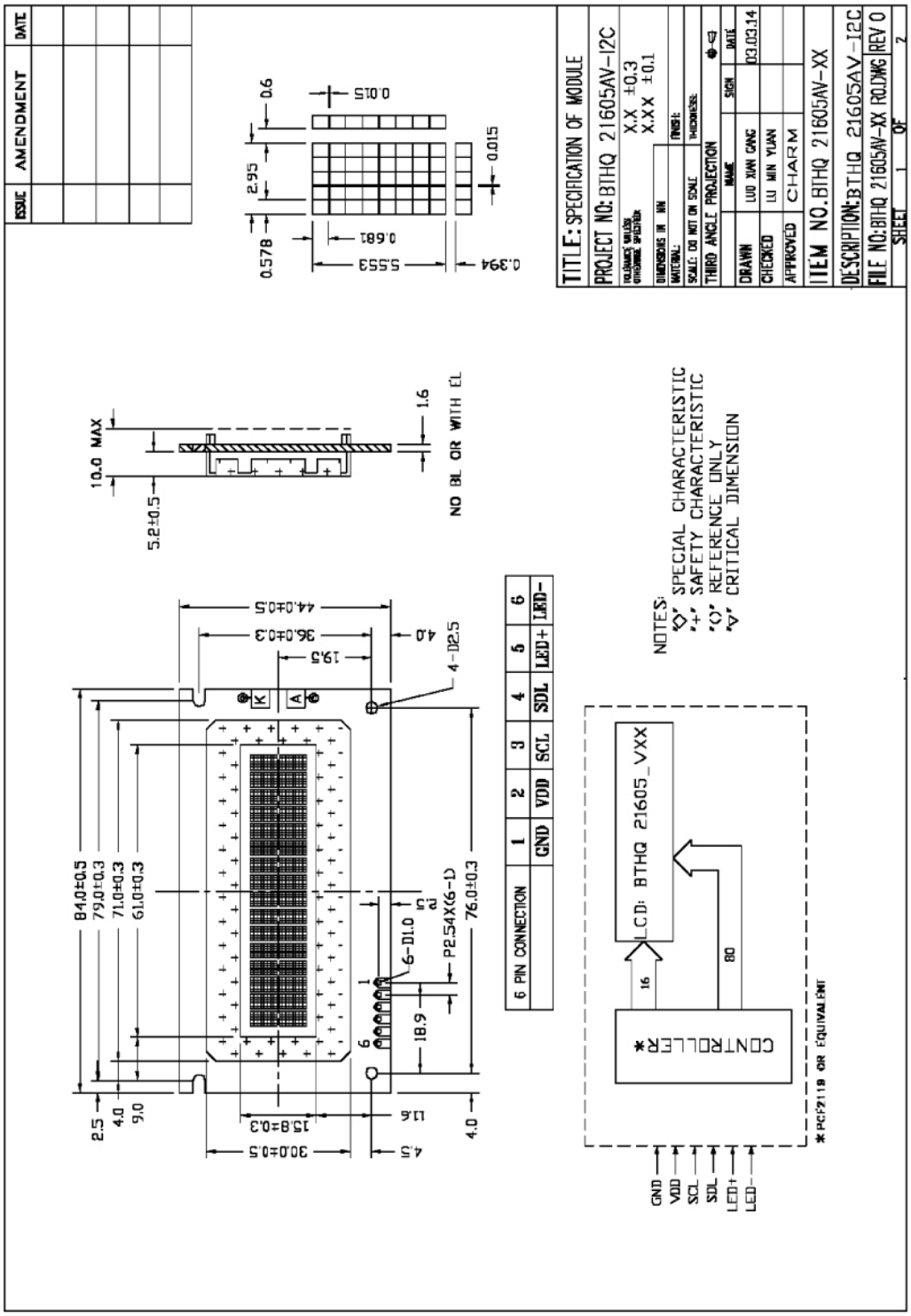


Figure 1(a): Specification Drawing with No BL or with EL

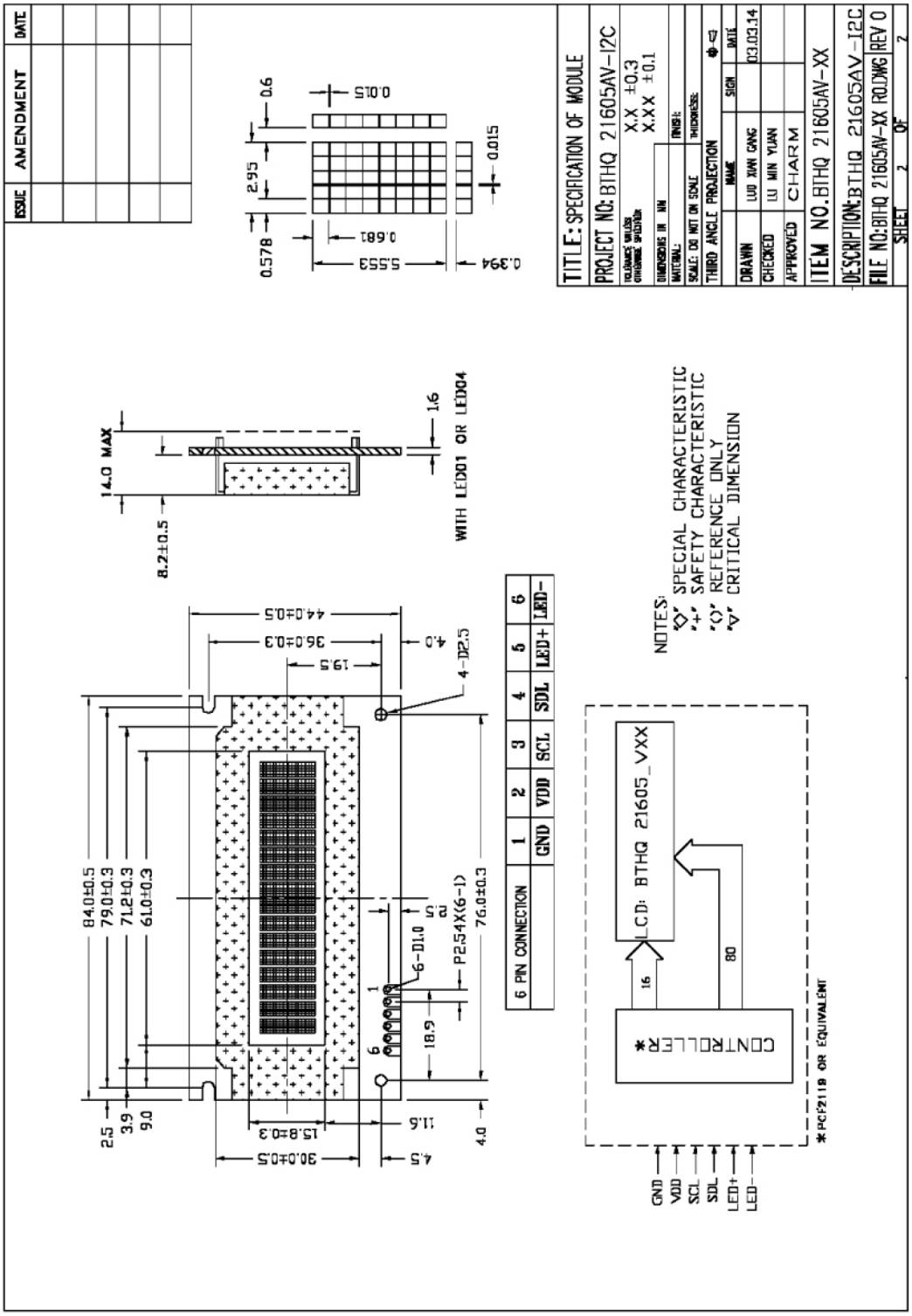


Figure 1(b): Specification Drawing with LED01 or LED04

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	GND	Ground (0V)
2	VDD	Power supply for logic.
3	SCL	I^2C serial clock input
4	SDL	I^2C serial data input/output (SDA)
5	LED+	Anode of backlight.
6	LED-	Cathode of backlight.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Supply voltage range (Logic)	VDD-GND	-0.5	+6.5	V
Input voltage range (LCD)	V_{LCD}	-0.5	+7.5	V
Input voltage range	Vi	-0.5	VDD +0.5	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to GND = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20∀C	+70∀C	-30∀C	+80∀C	Dry
Humidity	95% max. RH for Ta Ω 40∀C < 95% RH for Ta > 40∀C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ℑ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 ∀C, VDD = 5V∂5%, GND=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating voltage (Logic)	VDD-GND		4.75	5.0	5.25	V
Operating voltage for LCD (built-in)	VLCD-GND	Ta=-20 ∀C, Note1	-	4.4	-	V
		Ta=25 ∀C, Note1	4.0	4.3	4.6	V
		Ta=70 ∀C, Note1	-	3.8	-	V
Operating supply current	I_{DD}	Character mode, VDD =5.0V	-	1.1	1.8	mA
Input signal voltage low (SDA, SCL)	Vil		0	-	0.3 VDD	V
Input signal voltage high (SDA, SCL)	Vih		0.7 VDD	-	5.5	V
Supply Voltage of yellow-green LED04 backlight	VLED04	Forward current =90mA No. of LED chips=2x9=18	3.9	4.1	4.3	V

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Ta = -20 ∀C to +70 ∀C, VDD=5V∂5%, GND=0V; V_{LCD}= 2.2V to 6.5V.

Refer to Fig.2, I^2C Bus Timing Diagram of 'PHILIPS' PCF2119.

Table 6

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
LCD frame frequency (internal clock)	f_{FR}	VDD=5.0V	45	95	147	Hz
Oscillator frequency(not available at any pin)	f_{OSC}		140	250	450	kHz
External clock frequency	$f_{OSC(ext)}$		140	-	450	kHz
Oscillator start-up time after power-down	t_{OSCST}	Note 3	-	200	300	σs
Reset and power down high level pulse width	$t_{W(R,PD)}$		1			σs
Tolerable spike width on PD and Reset pads	$t_{SW(R,PD)}$				90	ns
Timing characteristics: I^2C-bus interface; (note 1)						
SCL clock frequency	f_{SCL}		-	-	400	kHz
SCL clock LOW period	t_{LOW}		1.3	-	-	σs
SCL clock HIGH period	t_{HIGH}		0.6	-	-	σs
Data set-up time	$t_{SU;DAT}$		100	-	-	ns
Data hold time	$t_{HD;DAT}$		0	-	-	ns
SCL and SDA rise time	t_r	Note 2,3	15+0.1C_B	-	300	ns
SCL and SDA fall time	t_f	Note 2,3	15+0.1C_B	-	300	ns
Capacitive bus line load	C_B		-		400	pF
Set-up time for a repeated START condition	$t_{SU;STA}$		0.6	-	-	σs
START condition hold time	$t_{HD;STA}$		0.6	-	-	σs
Set-up time for STOP condition	$t_{SU;STO}$		0.6	-	-	σs
Tolerable spike width on bus	t_{SW}		-	-	50	ns
Bus free time between STOP and START condition	t_{BUF}		1.3			σs

Notes :

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing to GND to VDD.
2. C_B=total capacitance of one bus line in pF.
3. Tested on a sample.

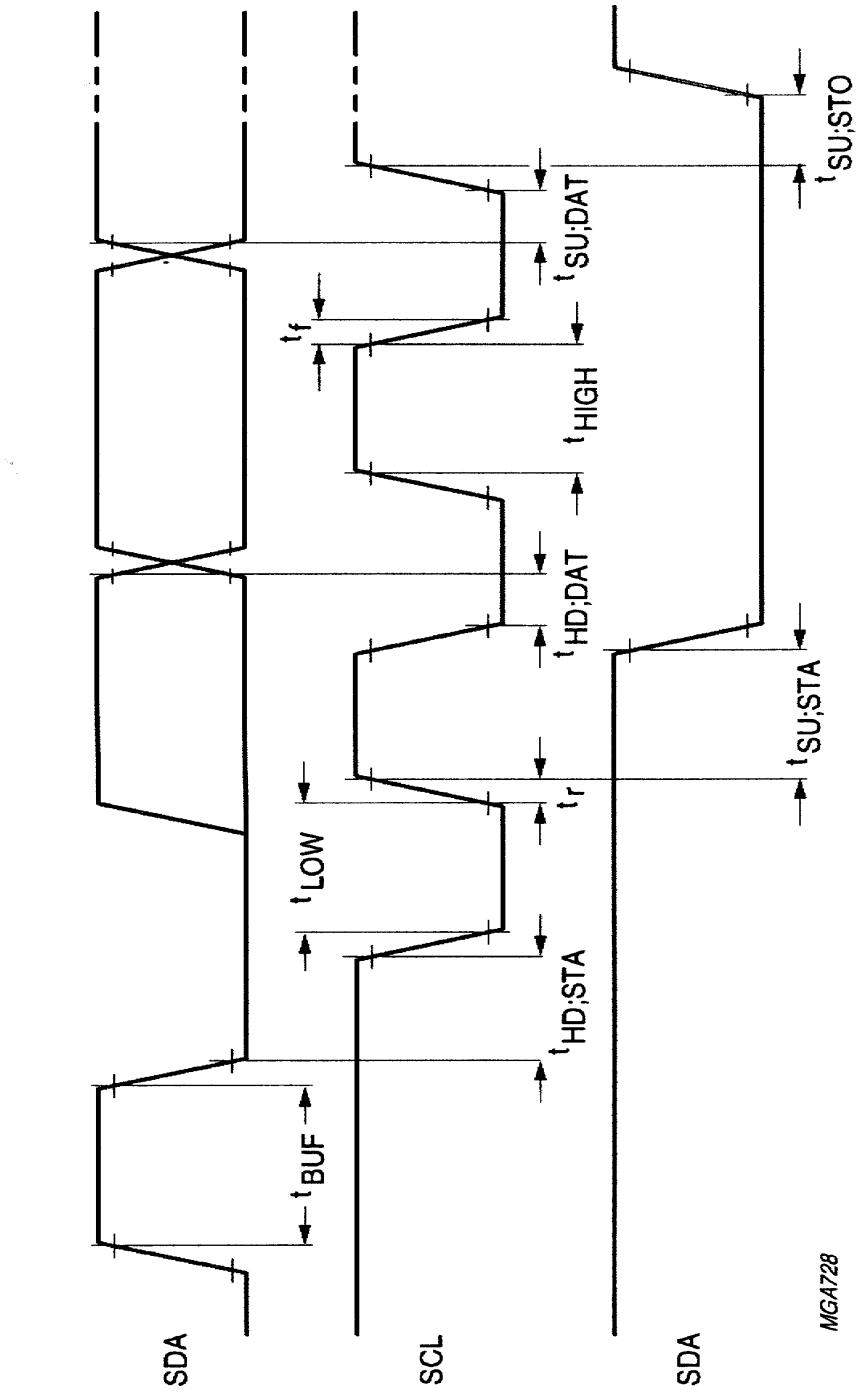
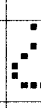


Figure 2: I^2C Bus Timing Diagram of 'PHILIPS' PCF2119.

6. Character Set 'R' in CGROM

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

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