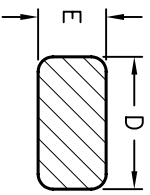
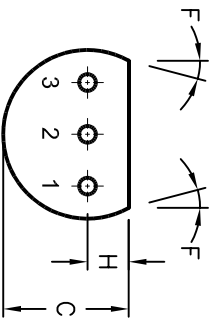


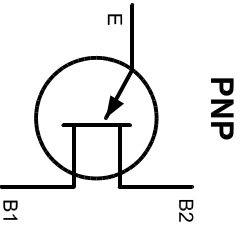
DIM.	MIN.	MAX.
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.50
F	5°	
G	1.14	1.40
H	1.14	1.53
K	12.70	



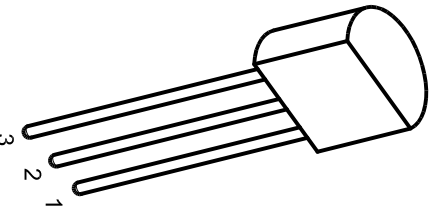
SECTION A-A



TO-92



- 1 Base 2
- 2 Emitter
- 3 Base 1



REVISIONS

DCP #	REV	DESCRIPTION	DRAWN	DATE	CHECKD	DATE	APPRD	DATE
1262	A	RELEASED	HO	5/13/02	JWM	1/10/03	DJC	1/10/03

Description:
A PN unijunction transistor in a TO-92 type package designed for use in pulse and timing circuits, sensing circuit and thyristor trigger circuits.

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

- Power Dissipation, P_D : 300mW
- Derate Above 25°C : 3.0mW/ $^\circ\text{C}$
- RMS Emitter Current, $I_{E(RMS)}$: 50mA
- Peak Pulse Emitter Current (Note 1) Current, I_E : 1.5A
- Emitter Reverse Voltage, V_{BZE} : 30V
- Interbase Voltage, V_{B2B1} : 35V
- Operating Junction Temperature Range, T_J : $-65^\circ\text{C} \sim +125^\circ\text{C}$
- Storage Temperature Range, T_{stg} : $-65^\circ\text{C} \sim +150^\circ\text{C}$

Electrical Characteristics: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Intrinsic Standoff Ratio		$V_{B2B1} = 10V$, Note 3	0.70	-	0.85	-
Interbase Resistance	r_{BB}		4.0	6.0	9.1	k Ohms
Interbase Resistance Temperature Coefficient			0.1	-	0.9	%/ $^\circ\text{C}$
Emitter Saturation Voltage	$V_{EB1(sat)}$	$V_{B2B1} = 10V$, $I_E = 50mA$, Note 4	-	2.5	-	V
Modulated Interbase Current	$I_{B2(mod)}$	$V_{B2B1} = 10V$, $I_E = 50mA$	-	15	-	mA
Emitter Reverse Current	I_{EB20}	$V_{BZE} = 30V$, $I_{B1} = 0$	-	0.005	1	μA
Peak Point Emitter Current	I_P	$V_{B2B1} = 25V$	-	1	5	μA
Valley Point Current	I_V	$V_{B2B1} = 20V$, $R_{B2} = 100$ Ohms, Note 4	4	7	-	mA
Base-One Peak Pulse Voltage	V_{OB1}		5	8	-	V

Notes:

1. Duty Cycle $\leq 1\%$, PRR = 10PPS.
2. Based upon power dissipation at $T_A = +25^\circ\text{C}$.
3. Intrinsic standoff ratio is essentially constant with temperature and interbase voltage and is defined by the equation:

$$\frac{V_P - V_{BB} + V_D}{V_D}$$
 where: V_P = Peak Point Emitter Voltage; V_{BB} = Interbase Voltage; V_D = Junction Diode Drop ($\sim 0.5V$)
4. Use pulse techniques: Pulse Width $\sim 300\mu\text{s}$, Duty Cycle $\leq 2\%$ to avoid internal heating due to interbase modulation which may result in erroneous readings.

DISCLAIMER:

ALL STATEMENTS AND TECHNICAL INFORMATION CONTAINED HEREIN ARE BASED UPON INFORMATION AND/OR TESTS WE BELIEVE TO BE ACCURATE AND RELIABLE. SINCE CONDITIONS OF USE ARE BEYOND OUR CONTROL, THE USER SHALL DETERMINE THE SUITABILITY OF THE PRODUCT FOR THE INTENDED USE AND ASSUME ALL RISK AND LIABILITY WHATSOEVER IN CONNECTION THEREWITH.

TOLERANCES:

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE FOR REFERENCE PURPOSES ONLY.

DRAWN BY:	DATE:	DRAWING TITLE:		ELECTRONIC FILE		REV
HISHAM ODISH	4/13/02	Unijunction Transistor, TO-92, PN		35C0718.DWG		A
CHECKED BY:	DATE:	SIZE	DWG. NO.			
JEFF MCWICKER	1/10/03	A	2N4871			
APPROVED BY:	DATE:	SCALE:	NTS	U.O.M.:	Millimeters	SHEET: 1 OF 1
DANIEL CAREY	1/10/03					