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SPC-P008.DWG

REVISONS		DOC. NO.	SPC-P008	Effective	7/8/02	Doc No	1308
DWG #	REV	DESCRIPTION	DATE	CHECK/D	DATE	APPR/D	DATE
1975	A	RELEASED	05/02/08	JN	05/02/08	JN	05/02/08

**Absolute Maximum Ratings:**

Collector-Emitter Voltage, $V_{ce0}$	200V
Collector-Base Voltage, $V_{cbo}$	200V
Emitter-Base Voltage, $V_{ebo}$	4V
Continuous Collector Current, $I_c$	1A
Base Current, $I_b$	500mA
Total Device Dissipation ( $T_c = +25^\circ\text{C}$ , Note 1), $P_d$	10W
Derate above $25^\circ\text{C}$	57mW/ $^\circ\text{C}$
Operating Junction Temperature Range, $T_j$	-65 $^\circ\text{C}$ to +200 $^\circ\text{C}$
Storage Temperature Range, $T_{sg}$	-65 $^\circ\text{C}$ to +200 $^\circ\text{C}$
Thermal Resistance, Junction-to-Case, $R_{\theta jc}$	17.5 $^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, $R_{\theta ja}$	150 $^\circ\text{C}/\text{W}$

**Electrical Characteristics:** ( $T_a = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OFF Characteristics</b>						
Collector-Emitter Sustaining Voltage	$V_{ce(sat)}$	$I_c = 30\text{mA}$ , $I_b = 0$ , Nme 1	200	-	-	V
Collector Cutoff Current	$I_{cbo}$	$V_{ce} = 175\text{V}$ , $I_b = 0$	-	-	50	$\mu\text{A}$
Emitter Cutoff Current	$I_{ebo}$	$V_{eb} = 4\text{V}$ , $I_c = 0$	-	-	20	$\mu\text{A}$
<b>ON Characteristics (Note 1)</b>						
DC Current Gain	$h_{FE}$	$I_c = 30\text{mA}$ , $V_{ce} = 10\text{V}$	30	-	150	
<b>Small-Signal Characteristics</b>						
Output Capacitance	$C_{obo}$	$V_{ce} = 10\text{V}$ , $I_b = 0$ , $f = 1\text{MHz}$	-	-	15	pF
Input Capacitance	$C_{ibo}$	$V_{ce} = 5\text{V}$ , $I_c = 0$ , $f = 1\text{MHz}$	-	-	75	pF
Small-Signal Current Gain	$h_{fe}$	$I_c = 10\text{mA}$ , $V_{ce} = 10\text{V}$ , $f = 5\text{MHz}$	25	-	-	
Real Part of Input Impedance	$\text{Re}(h_{ie})$	$V_{ce} = 10\text{V}$ , $I_c = 5\text{mA}$ , $f = 1\text{MHz}$	-	-	300	Ohm

Note 1. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .  
**CAUTION:** The sustaining voltage *must not* be measured on a curve tracer.

**DISCLAIMER:**  
ALL STATEMENTS AND TECHNICAL INFORMATION CONTAINED HEREIN ARE BASED UPON INFORMATION AND/OR TESTS WE BELIEVE TO BE ACCURATE AND RELIABLE. SINCE CONDITIONS OF USE ARE BEYOND OUR CONTROL, THE USER SHALL DETERMINE THE SUITABILITY OF THE PRODUCT FOR THE INTENDED USE AND ASSUME ALL RISK AND LIABILITY WHATSOEVER IN CONNECTION THEREWITH.

**TOLERANCES:**  
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE FOR REFERENCE PURPOSES ONLY.

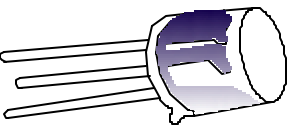
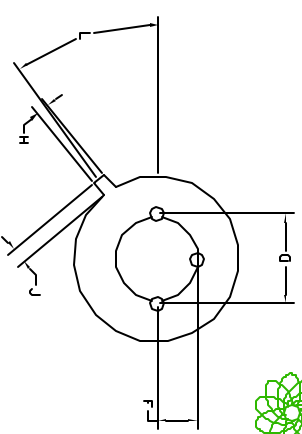
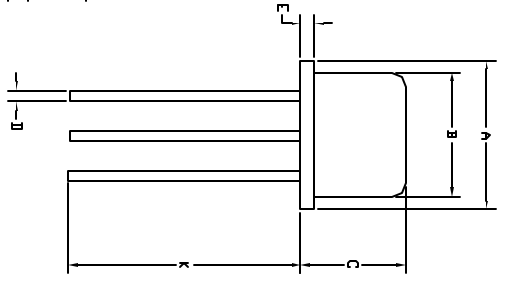
**DRAWN BY:** Jason Nash  
**CHECKED BY:** Jason Nash  
**APPROVED BY:** Jason Nash

**DATE:** 05/02/08  
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**DRAWING TITLE:** A silicon PNP transistor  
**SIZE:** A  
**SCALE:** NTS

**DWG. NO.:** 2N5415  
**ELECTRONIC FILE:** 35C0725.DWG

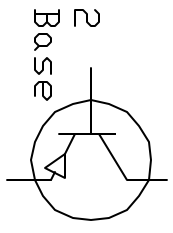
**SHEET:** 1 OF 1



**PIN CONFIGURATION**  
1. Emitter  
2. BASE  
3. COLLECTOR

**PNP**

3 Collector



1 Emitter

DIM	Millimeters	
	MIN	MAX
A	8.5	9.39
B	7.74	8.5
C	6.09	6.6
D	0.4	0.53
E	----	0.88
F	2.41	2.66
G	4.82	5.33
H	0.71	0.86
J	0.73	1.02
K	12.7	----
L	42 DEG	48 DEG