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SPC-F005.DWG

REVISIONS

DOC. NO. SPC-F005 * Effective: 7/8/02 * DCP No: 1398

DCP #	REV	DESCRIPTION	DRAWN	DATE	CHECKD	DATE	APPRVD	DATE
1885	A	RELEASED	BYF	02/03/06	HO	2/6/06	JWM	2/6/06



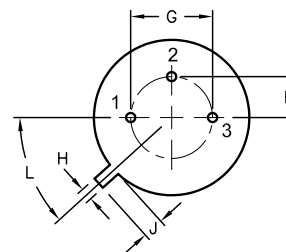
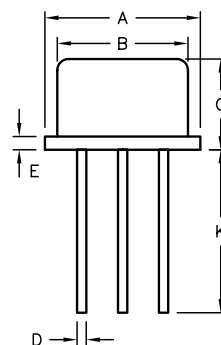
Description:

A silicon PNP transistor in a TO-39 type case designed primarily for amplifier and switching applications. This device features high breakdown voltage, low leakage current, low capacity, and beta useful over an extremely wide current range.

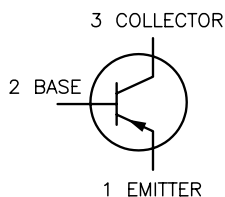
Absolute Maximum Ratings:

- Collector-Base Voltage, $V_{CB0} = 60V$
- Collector-Emitter Voltage, $V_{CE0} = 60V$
- Emitter-Base Voltage, $V_{EB0} = 5V$
- Continuous Collector Current, $I_C = 1A$
- Total Device Dissipation ($T_A = +25^\circ C$), $P_D = 0.8W$
Derate above $25^\circ C = 4.56mW/^\circ C$
- Total Device Dissipation ($T_C = +25^\circ C$), $P_D = 4W$
Derate above $25^\circ C = 22.8mW/^\circ C$
- Operating Junction Temperature Range, $T_J = -65^\circ C$ to $+200^\circ C$
- Storage Temperature Range, $T_{stg} = -65^\circ C$ to $+200^\circ C$
- Thermal Resistance, Junction-to-Case, $R_{thJC} = 20^\circ C/W$
- Thermal Resistance, Junction-to-Ambient, $R_{thJA} = 140^\circ C/W$
- Lead Temperature (During Soldering 1/16" from case, 60sec max), $T_L = 300^\circ C$

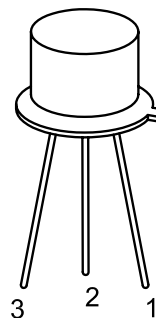
Dim	Min	Max
A	8.50	9.39
B	7.74	8.50
C	6.09	6.60
D	0.40	0.53
E	-	0.88
F	2.41	2.66
G	4.82	5.33
H	0.71	0.86
J	0.73	1.02
K	12.70	-
L	42 DEG	48 DEG



PNP



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DISCLAIMER:
ALL STATEMENTS AND TECHNICAL INFORMATION CONTAINED HEREIN ARE BASED UPON INFORMATION AND/OR TESTS WE BELIEVE TO BE ACCURATE AND RELIABLE. SINCE CONDITIONS OF USE ARE BEYOND OUR CONTROL, THE USER SHALL DETERMINE THE SUITABILITY OF THE PRODUCT FOR THE INTENDED USE AND ASSUME ALL RISK AND LIABILITY WHATSOEVER IN CONNECTION THEREWITH.

TOLERANCES:
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE FOR REFERENCE PURPOSES ONLY.

DRAWN BY:	DATE:
BASAM YOUSIF	02/03/06
CHECKED BY:	DATE:
HISHAM ODISH	2/6/06
APPROVED BY:	DATE:
JEFF MCVICKER	2/6/06

DRAWING TITLE: Power Transistor, Silicon, TO-39, PNP			
SIZE	DWG. NO.	ELECTRONIC FILE	REV
A	2N4032	35C0709.DWG	A
SCALE: NTS	U.O.M.: MILLIMETERS	SHEET: 1 OF 2	

Electrical Characteristics: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
OFF Characteristics					
Collector–Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10\text{mA}, I_B = 0$	60	–	V
Collector–Base Breakdown Voltage	$V_{(BR)CE0}$	$I_C = 10\mu\text{A}, I_E = 0$	60	–	V
Emitter–Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu\text{A}, I_C = 0$	5	–	V
Collector Cut–Off Current	I_{CBO}	$V_{CB} = 50\text{V}, I_E = 0$	–	50	nA
		$V_{CB} = 50\text{V}, I_E = 0, T_A = +150^\circ\text{C}$	–	50	μA
Emitter Cut–Off Current	I_{EBO}	$V_{BE} = 5\text{V}, I_C = 0$	–	10	μA

ON Characteristics

DC Current Gain	h_{FE}	$V_{CE} = 5\text{V}, I_C = 100\mu\text{A}$	75	–	–
		$V_{CE} = 5\text{V}, I_C = 100\text{mA}$	100	300	–
		$V_{CE} = 5\text{V}, I_C = 100\text{mA}, T_A = -55^\circ\text{C}$	40	–	–
		$V_{CE} = 5\text{V}, I_C = 500\text{mA}$	70	–	–
		$V_{CE} = 5\text{V}, I_C = 1\text{A}$	40	–	–
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 150\text{mA}, I_B = 15\text{mA}$	–	0.15	V
		$I_C = 500\text{mA}, I_B = 50\text{mA}$	–	0.5	V
Base–Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 150\text{mA}, I_B = 15\text{mA}$	–	0.9	V
Base–Emitter ON Voltage	$V_{BE(on)}$	$V_{CE} = 500\text{mV}, I_C = 500\text{mA}$	–	1.1	V

Small-Signal Characteristics

Output Capacitance	C_{obo}	$V_{CE} = 10\text{V}, f = 1\text{MHz}$	–	20	pF
Input Capacitance	C_{iBO}	$V_{EB} = 500\text{mV}, f = 1\text{MHz}$	–	110	pF
Small–Signal Current Gain	h_{fe}	$V_{CE} = 10\text{V}, I_C = 50\text{mA}, f = 100\text{MHz}$	1	4	–

Switching Characteristics

Storage Time	t_s	$I_C = 500\text{mA}, I_{B1} = I_{B2} = 50\text{mA}$	–	350	ns
Turn–On Time	t_{on}	$I_C = 500\text{mA}, I_{B1} = 50\text{mA}$	–	100	ns
Fall Time	t_f	$I_C = 500\text{mA}, I_{B1} = I_{B2} = 50\text{mA}$	–	50	ns

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A

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