

Power management (dual transistors)

EMF32 / UMF32N

DTA143T and 2SK3019 are housed independently in a EMT6 package.

●Application

Power management circuit

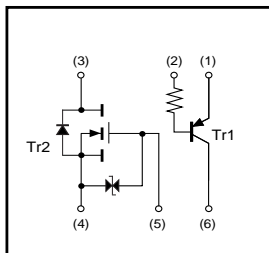
●Features

- 1) Power switching circuit in a single package.
- 2) Mounting cost and area can be cut in half.

●Structure

Silicon epitaxial planar transistor

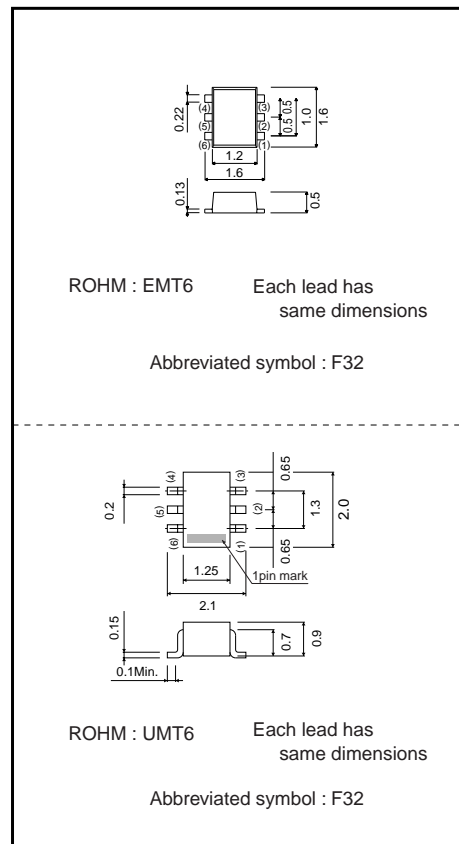
●Equivalent circuits



●Packaging specifications

Type	EMF32	UMF32
Package	EMT6	UMT6
Marking	F32	F32
Code	T2R	TR
Basic ordering unit (pieces)	8000	3000

●External dimensions (Unit : mm)



Transistors

●Absolute maximum ratings (Ta=25°C)

Tr1

Parameter	Symbol	Limits	Unit
Collector-base voltage	V _{CB0}	-50	V
Collector-emitter voltage	V _{CE0}	-50	V
Emitter-base voltage	V _{EB0}	-5	V
Collector current	I _c	-100	mA
Power dissipation	P _c	150(TOTAL)	mW *1
Junction temperature	T _j	150	°C
Range of storage temperature	T _{stg}	-55 to +150	°C

*1 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

Tr2

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{DSS}	30	V	
Gate-source voltage	V _{GSS}	±20	V	
Drain current	Continuous	I _D	100	mA
	Pulsed	I _{DP}	200	mA *1
Reverse drain current	Continuous	I _{DR}	100	mA
	Pulsed	I _{DRP}	200	mA *1
Total power dissipation	P _D	150(TOTAL)	mW *2	
Channel temperature	T _{ch}	150	°C	
Range of storage temperature	T _{stg}	-55 to +150	°C	

*1 PW≤10ms Duty cycle≤50%

*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

●Electrical characteristics (Ta=25°C)

Tr1

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV _{CB0}	-50	-	-	V	I _c =-50μA
Collector-emitter breakdown voltage	BV _{CE0}	-50	-	-	V	I _c =-1mA
Emitter-base breakdown voltage	BV _{EB0}	-5	-	-	V	I _E =-50μA
Collector cutoff current	I _{CB0}	-	-	-0.5	μA	V _{CB} =-50V
Emitter cutoff current	I _{EB0}	-	-	-0.5	μA	V _{EB} =-4V
Collector-emitter saturation voltage	V _{CE(sat)}	-	-	-0.3	V	I _c /I _B =-5mA/-0.25mA
DC current transfer ratio	h _{FE}	100	250	600	-	I _c =-1mA, V _{CE} =-5V
Input resistance	R ₁	3.29	4.7	6.11	kΩ	-
Transition frequency	f _T	-	250	-	MHz	V _{CE} =-10V, I _E =5mA, f=100MHz *

* Transition frequency of the device

Tr2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±1	μA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	30	-	-	V	I _D =10μA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	-	-	1.0	μA	V _{DS} =30V, V _{GS} =0V
Gate-threshold voltage	V _{GS(th)}	0.8	-	1.5	V	V _{DS} =3V, I _D =100μA
Static drain-source on-state resistance	R _{DS(on)}	-	5	8	Ω	I _D =10mA, V _{GS} =4V
		-	7	13	Ω	I _D =1mA, V _{GS} =2.5V
Forward transfer admittance	Y _{fs}	20	-	-	ms	V _{DS} =3V, I _D =10mA
Input capacitance	C _{iss}	-	13	-	pF	V _{DS} =5V, V _{GS} =0V, f=1MHz
Output capacitance	C _{oss}	-	9	-	pF	
Reverse transfer capacitance	C _{rss}	-	4	-	pF	
Turn-on delay time	t _{d(on)}	-	15	-	ns	
Rise time	t _r	-	35	-	ns	
Turn-off delay time	t _{d(off)}	-	80	-	ns	I _D =10mA, V _{DD} =5V, V _{GS} =5V, R _L =500Ω, R _{GS} =10Ω
Fall time	t _f	-	80	-	ns	

Transistors

● Electrical characteristic curves

Tr1

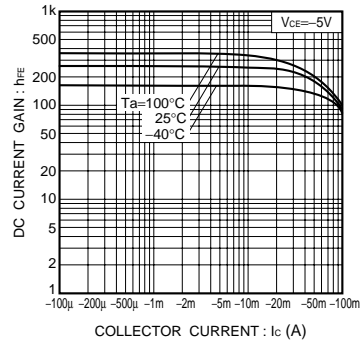


Fig.1 DC current gain vs. collector current

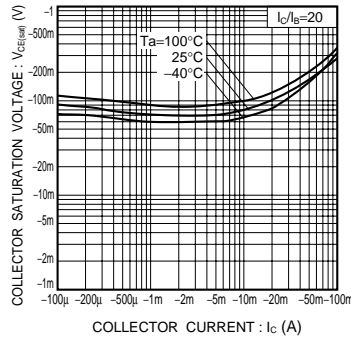


Fig.2 Collector-emitter saturation voltage vs. collector current

Tr2

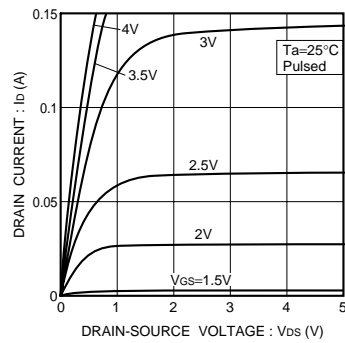


Fig.3 Typical output characteristics

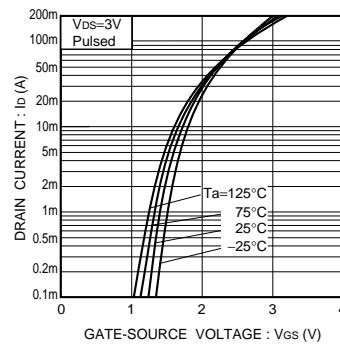


Fig.4 Typical transfer characteristics

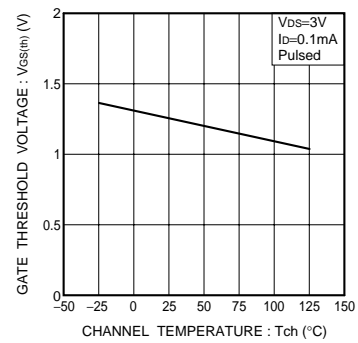


Fig.5 Gate threshold voltage vs. channel temperature

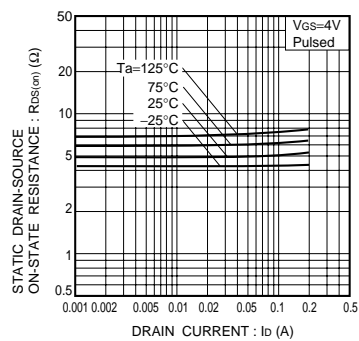


Fig.6 Static drain-source on-state resistance vs. drain current (I)

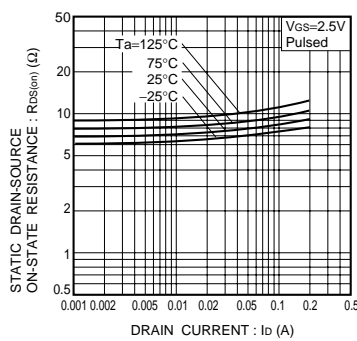


Fig.7 Static drain-source on-state resistance vs. drain current (II)

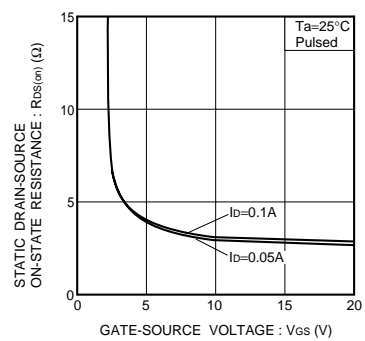


Fig.8 Static drain-source on-state resistance vs. gate-source voltage

Transistors

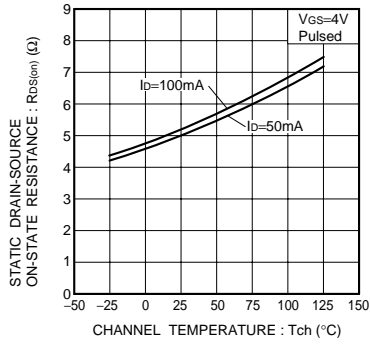


Fig.9 Static drain-source on-state resistance vs. channel temperature

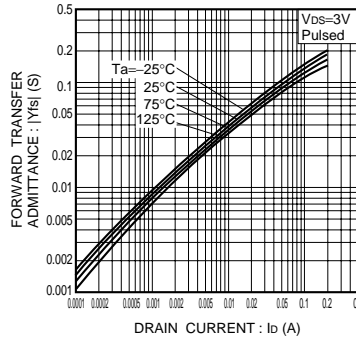


Fig.10 Forward transfer admittance vs. drain current

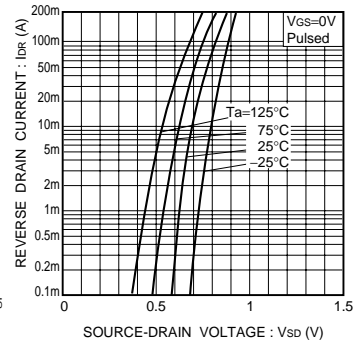


Fig.11 Reverse drain current vs. source-drain voltage (I)

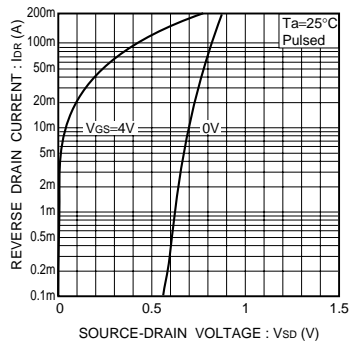


Fig.12 Reverse drain current vs. source-drain voltage (II)

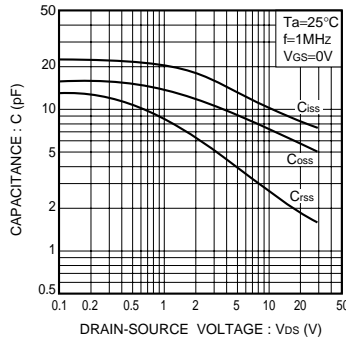


Fig.13 Typical capacitance vs. drain-source voltage

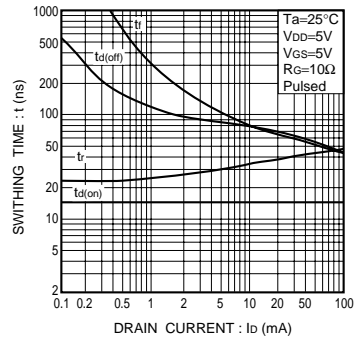


Fig.14 Switching characteristics

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