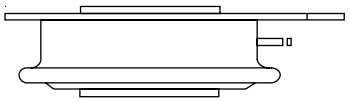
Phase Control Thyristors (Hockey PUK Version), 500 A



TO-200AB (A-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (A-PUK)
- Lead (Pb)-free
- Designed and qualified for industrial level

Pb-free

RoHS COMPLIANT

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY	
$I_{T(AV)}$	500 A

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		500	A
	T_{hs}	55	°C
$I_{T(RMS)}$		960	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	7850	A
	60 Hz	8220	
I^2t	50 Hz	308	kA^2s
	60 Hz	281	
V_{DRM}/V_{RRM}		400 to 600	V
t_q	Typical	100	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST280C..C	04	400	500	30
	06	600	700	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side(single side) cooled			500 (185)	A
					55 (85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled			960	A
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	7850	
		t = 8.3 ms			8220	
		t = 10 ms	100 % V_{RRM} reapplied		6600	
		t = 8.3 ms			6900	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		308	kA^2s
		t = 8.3 ms			281	
		t = 10 ms	100 % V_{RRM} reapplied		218	
		t = 8.3 ms			200	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			3080	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.84	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.88	
Low level value of on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.50	mΩ
High level value of on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.47	
Maximum on-state voltage	V_{TM}	I_{pk} = 1050 A, T_J = 125 °C, t_p = 10 ms sine pulse			1.36	V
Maximum holding current	I_H	T_J = 25 °C, anode supply 12 V resistive load			600	mA
Maximum (typical) latching current	I_L				1000 (300)	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ µs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	1000	A/µs
Typical delay time	t_d	Gate current 1 A, dI_g/dt = 1 A/µs V_d = 0.67 % V_{DRM}, T_J = 25 °C	1.0	µs
Typical turn-off time	t_q	I_{TM} = 300 A, $T_J = T_J$ maximum, dI/dt = 20 A/µs, V_R = 50 V, dV/dt = 20 V/µs, gate 0 V 100 Ω, t_p = 500 µs	100	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/µs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		10.0		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		2.0		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3.0		A
Maximum peak positive gate voltage	+ V_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		20		V
Maximum peak negative gate voltage	- V_{GM}			5.0		V
DC gate current required to trigger	I_{GT}	T_J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	180	-	mA
		T_J = 25 °C		90	150	mA
		T_J = 125 °C		40	-	mA
DC gate voltage required to trigger	V_{GT}	T_J = - 40 °C		2.9	-	V
		T_J = 25 °C		1.8	3.0	V
		T_J = 125 °C		1.2	-	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.30		V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	°C
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.17	K/W
		DC operation double side cooled	0.08	K/W
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.033	K/W
		DC operation double side cooled	0.017	K/W
Mounting force, ± 10 %			4900 (500)	N (kg)
Approximate weight			50	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (A-PUK)	

ΔR_{thJC} CONDUCTION

CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.016	0.016	0.011	0.011	$T_J = T_J$ maximum	K/W
120°	0.019	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.037		
30°	0.060	0.060	0.060	0.061		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

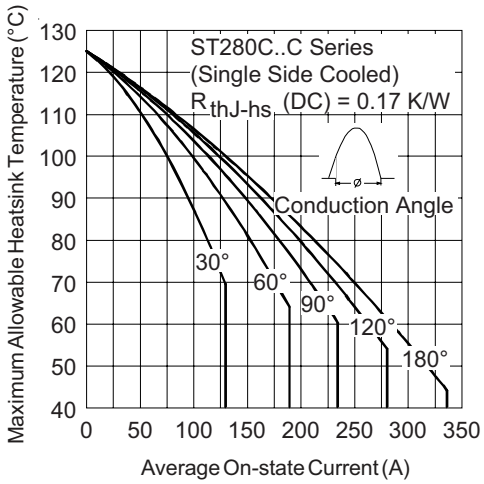


Fig. 1 - Current Ratings Characteristics

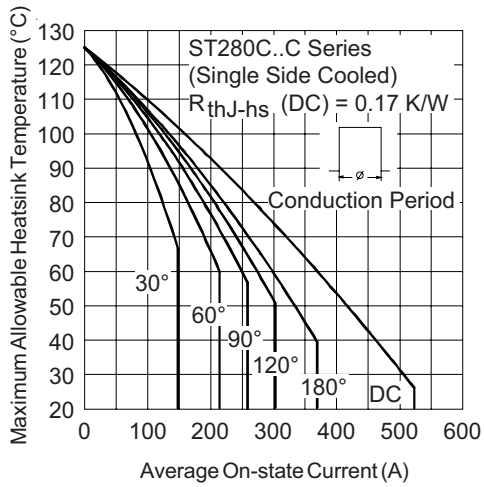


Fig. 2 - Current Ratings Characteristics

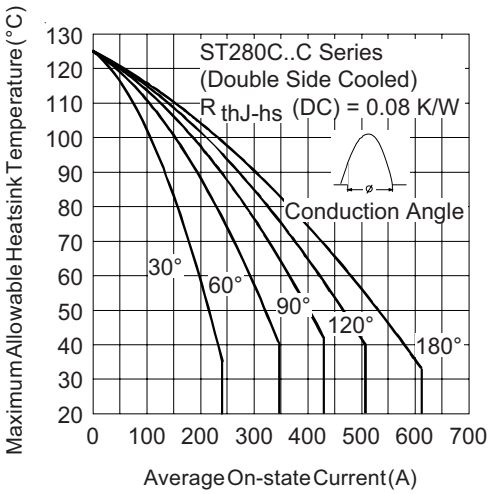


Fig. 3 - Current Ratings Characteristics

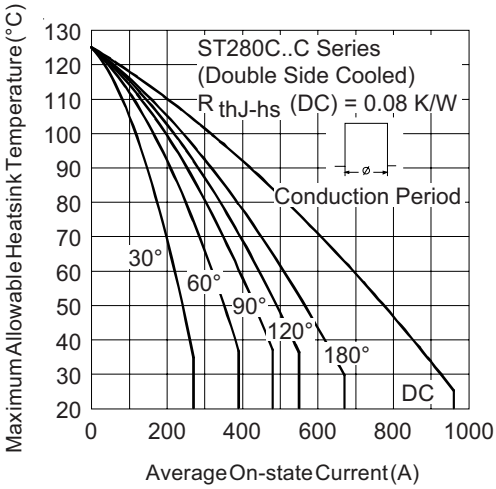


Fig. 4 - Current Ratings Characteristics

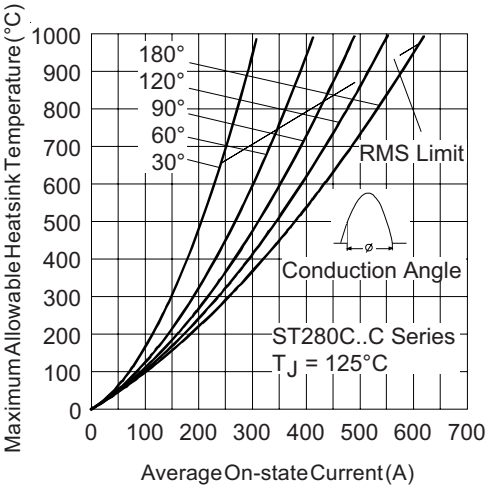


Fig. 5 - On-State Power Loss Characteristics

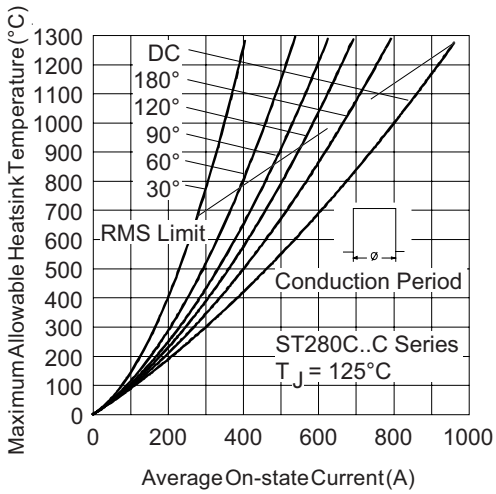


Fig. 6 - On-State Power Loss Characteristics

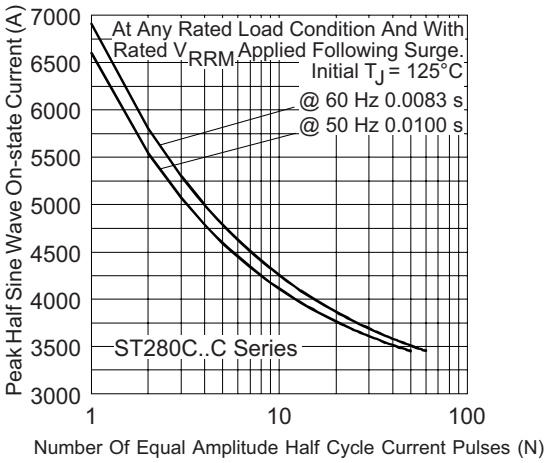


Fig. 7 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

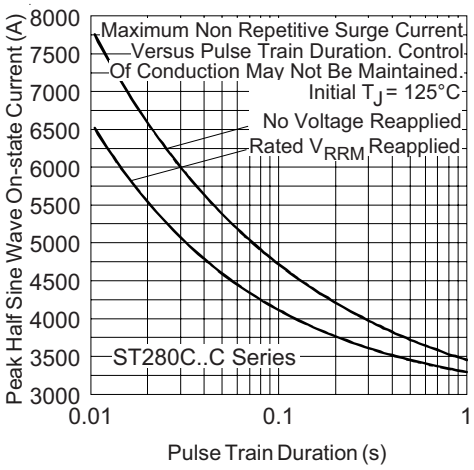


Fig. 8 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

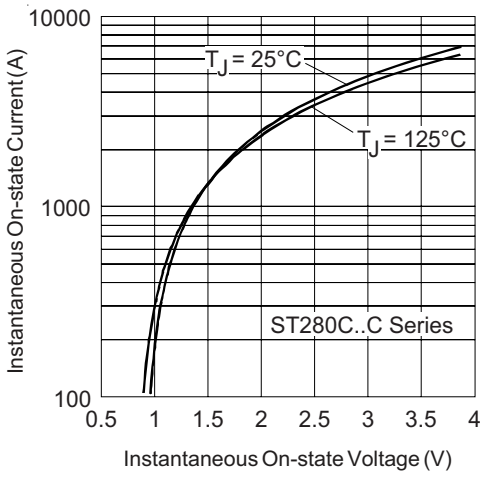


Fig. 9 - On-State Voltage Drop Characteristics

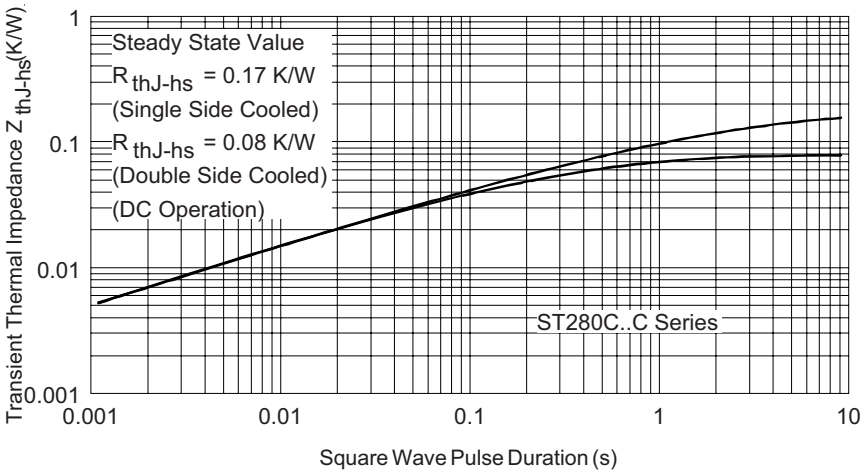


Fig. 10 - Thermal Impedance $Z_{thJ\text{-}hs}$ Characteristics

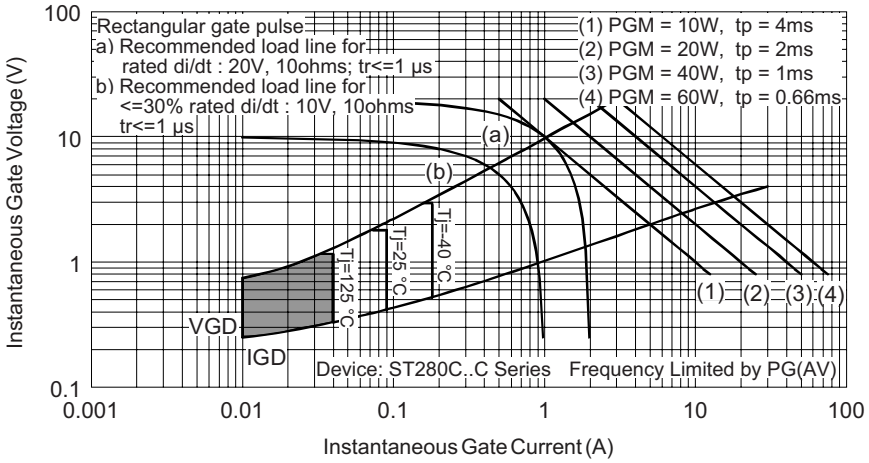


Fig. 11 - Gate Characersitics

ORDERING INFORMATION TABLE

Device code

ST	28	0	C	06	C	1	-	PbF
1	2	3	4	5	6	7	8	9

1 - Thyristor

2 - Essential part number

3 - 0 = Converter grade

4 - C = Ceramic PUK

5 - Voltage code: code x 100 = V_{RRM} (see Voltage Ratings table)

6 - C = PUK case TO-200AB (A-PUK)

7 - 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)
1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)
2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
3 = Fast-on terminals (gate and auxiliary cathode soldered leads)

8 - Critical dV/dt:
- None = 500 V/µs (standard selection)
- L = 1000 V/µs (special selection)

9 - Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95074

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