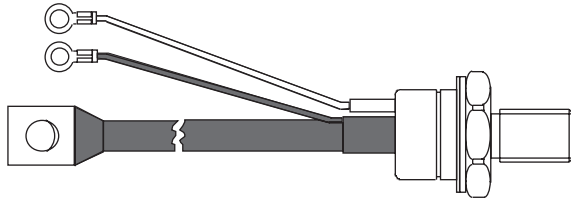


## Inverter Grade Thyristors (Stud Version), 105 A



TO-209AC (TO-94)

**FEATURES**

- All diffused design
- Center amplifying gate
- Guaranteed high  $dV/dt$
- Guaranteed high  $dI/dt$
- High surge current capability
- Low thermal impedance
- High speed performance
- Compression bonding
- Lead (Pb)-free
- Designed and qualified for industrial level


**RoHS  
COMPLIANT**
**PRODUCT SUMMARY**

$I_{T(AV)}$	105 A
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**TYPICAL APPLICATIONS**

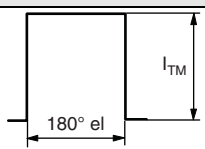
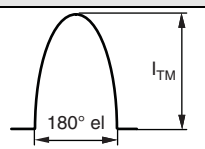
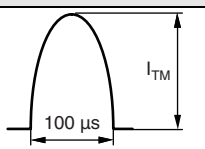
- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

**MAJOR RATINGS AND CHARACTERISTICS**

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		105	A
	$T_C$	85	°C
$I_{T(RMS)}$		165	A
$I_{TSM}$	50 Hz	3000	
	60 Hz	3150	
$I^2t$	50 Hz	45	kA <sup>2</sup> s
	60 Hz	41	
$V_{DRM}/V_{RRM}$		400 to 800	V
$t_q$	Range	10 to 25	µs
$T_J$		- 40 to 125	°C

**ELECTRICAL SPECIFICATIONS**
**VOLTAGE RATINGS**

TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST103S	04	400	500	30
	08	800	900	

CURRENT CARRYING CAPABILITY							
FREQUENCY							UNITS
50 Hz	280	180	440	330	4730	3630	A
400 Hz	310	200	470	300	2500	1850	
1000 Hz	320	200	480	310	1530	1090	
2500 Hz	340	210	490	320	840	580	
Recovery voltage $V_r$	50		50		50		V
Voltage before turn-on $V_d$	$V_{DRM}$		$V_{DRM}$		$V_{DRM}$		
Rise of on-state current $di/dt$	50		-		-		A/ $\mu$ s
Case temperature	60	85	60	85	60	85	$^{\circ}$ C
Equivalent values for RC circuit	22/0.15		22/0.15		22/0.15		$\Omega/\mu$ F

ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			105	A
					85	$^{\circ}$ C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 76 $^{\circ}$ C case temperature			165	A
Maximum peak, one half cycle, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reappplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	3000	
		t = 8.3 ms			3150	
		t = 10 ms	100 % $V_{RRM}$ reappplied		2530	
		t = 8.3 ms			2650	
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reappplied		45	
		t = 8.3 ms			41	
		t = 10 ms	100 % $V_{RRM}$ reappplied		32	
		t = 8.3 ms			29	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reappplied			450	$kA^2\sqrt{s}$
Maximum peak on-state voltage	$V_{TM}$	$I_{TM} = 300$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine wave pulse			1.73	V
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			1.32	
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			1.35	
Low level value of forward slope resistance	$r_{t1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			1.40	$m\Omega$
High level value of forward slope resistance	$r_{t2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum			1.30	
Maximum holding current	$I_H$	$T_J = 25$ $^{\circ}$ C, $I_T > 30$ A			600	mA
Typical latching current	$I_L$	$T_J = 25$ $^{\circ}$ C, $V_A = 12$ V, $R_a = 6$ $\Omega$ , $I_G = 1$ A			1000	



<b>SWITCHING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ , $I_{TM} = 2 \times di/dt$	1000	A/ $\mu$ s
Typical delay time	$t_d$	$T_J = 25^\circ\text{C}$ , $V_{DM} = \text{Rated } V_{DRM}$ , $I_{TM} = 50 \text{ A DC}$ , $t_p = 1 \mu\text{s}$ Resistive load, gate pulse: 10 V, 5 $\Omega$ source	0.80	$\mu$ s
Maximum turn-off time	minimum	$T_J = T_J$ maximum, $I_{TM} = 100 \text{ A}$ , commutating di/dt = 10 A/ $\mu$ s $V_R = 50 \text{ V}$ , $t_p = 200 \mu\text{s}$ , dV/dt: See table in device code	10	
	maximum		25	

<b>BLOCKING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % $V_{DRM}$ , higher value available on request	500	V/ $\mu$ s
Maximum peak reverse and off-state leakage current	$I_{RRM}$ , $I_{DRM}$	$T_J = T_J$ maximum, rated $V_{DRM}/V_{RRM}$ applied	30	mA

<b>TRIGGERING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$	$T_J = T_J$ maximum, $f = 50 \text{ Hz}$ , $d\% = 50$	40	W
Maximum average gate power	$P_{G(AV)}$		5	
Maximum peak positive gate current	$I_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5 \text{ ms}$	5	A
Maximum peak positive gate voltage	+ $V_{GM}$		20	V
Maximum peak negative gate voltage	- $V_{GM}$		5	
Maximum DC gate current required to trigger	$I_{GT}$	$T_J = 25^\circ\text{C}$ , $V_A = 12 \text{ V}$ , $R_a = 6 \Omega$	200	mA
Maximum DC gate voltage required to trigger	$V_{GT}$		3	V
Maximum DC gate current not to trigger	$I_{GD}$	$T_J = T_J$ maximum, rated $V_{DRM}$ applied	20	mA
Maximum DC gate voltage not to trigger	$V_{GD}$		0.25	V

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	$T_J$		- 40 to 125	$^\circ\text{C}$
Maximum storage temperature range	$T_{Stg}$		- 40 to 150	
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation	0.195	K/W
Maximum thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth, flat and greased	0.08	
Mounting torque, $\pm 10\%$		Non-lubricated threads	15.5 (137)	N · m (lbf · in)
		Lubricated threads	14 (120)	
Approximate weight			130	g
Case style		See dimensions - link at the end of datasheet	TO-209AC (TO-94)	

$\Delta R_{thJC}$ CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.034	0.025	$T_J = T_{J \text{ maximum}}$	K/W
120°	0.040	0.042		
90°	0.052	0.056		
60°	0.076	0.079		
30°	0.126	0.127		

**Note**

- The table above shows the increment of thermal resistance  $R_{thJC}$  when devices operate at different conduction angles than DC

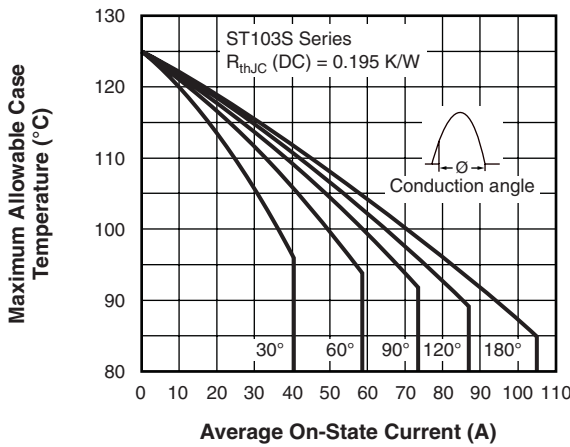


Fig. 1 - Current Ratings Characteristics

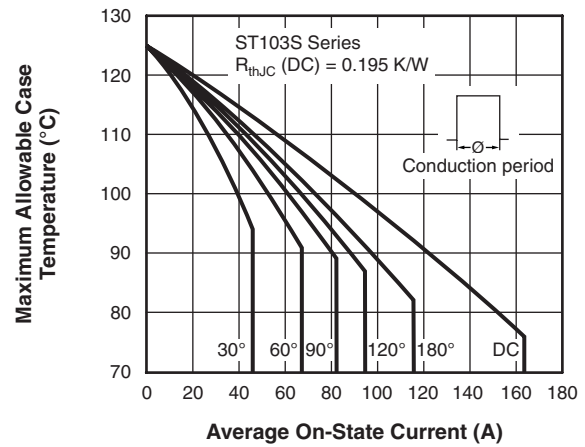


Fig. 2 - Current Ratings Characteristics

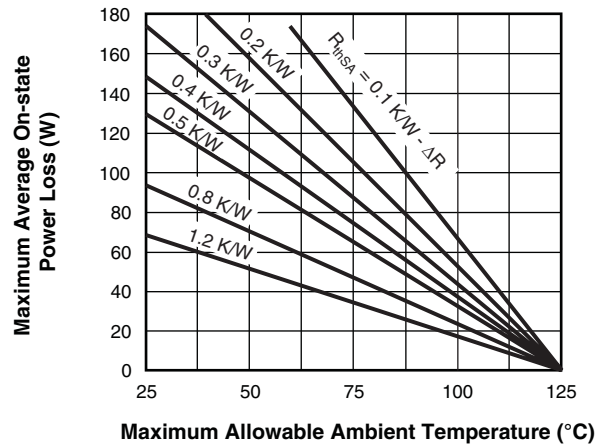
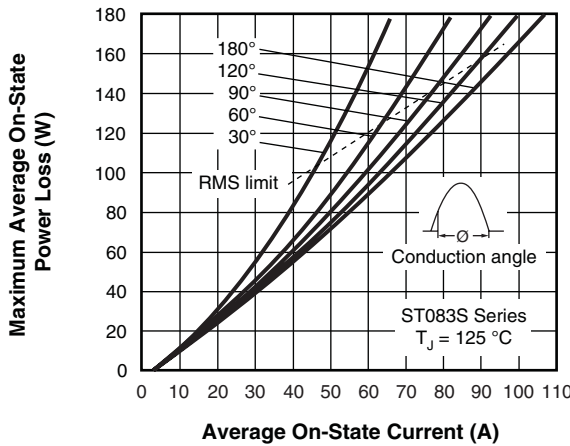


Fig. 3 - On-State Power Loss Characteristics

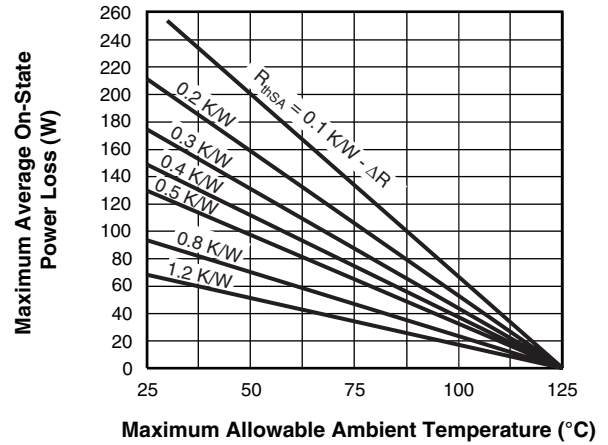
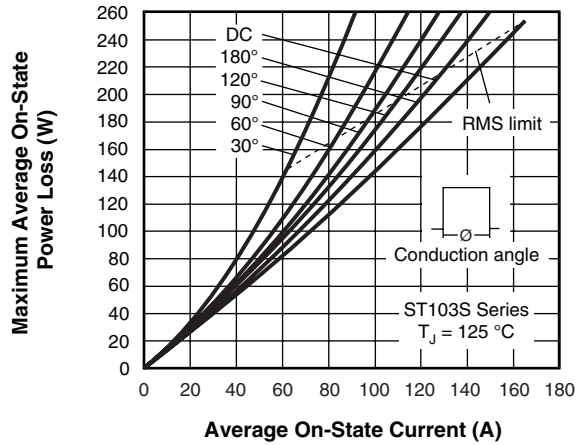


Fig. 4 - On-State Power Loss Characteristics

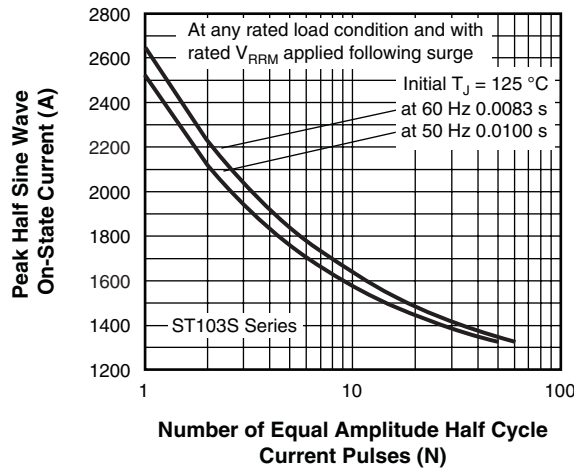


Fig. 5 - Maximum Non-Repetitive Surge Current

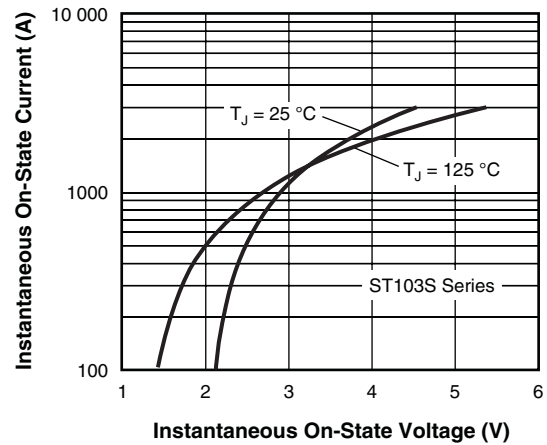


Fig. 7 - On-State Voltage Drop Characteristics

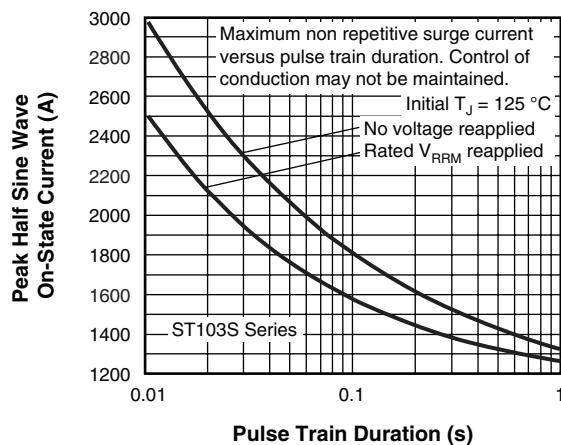


Fig. 6 - Maximum Non-Repetitive Surge Current

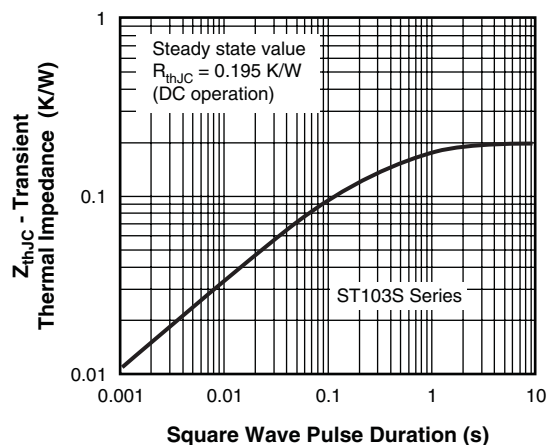


Fig. 8 - Thermal Impedance  $Z_{\theta JC}$  Characteristic

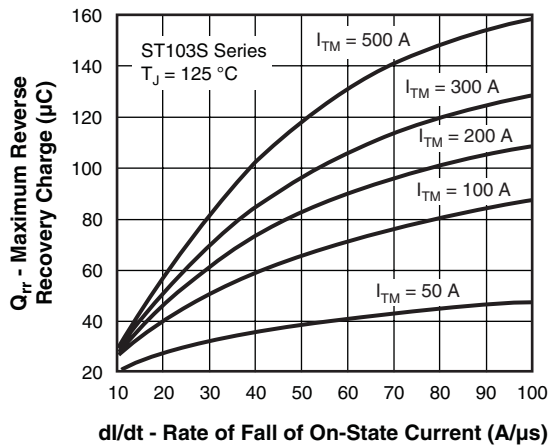


Fig. 9 - Reverse Recovered Charge Characteristics

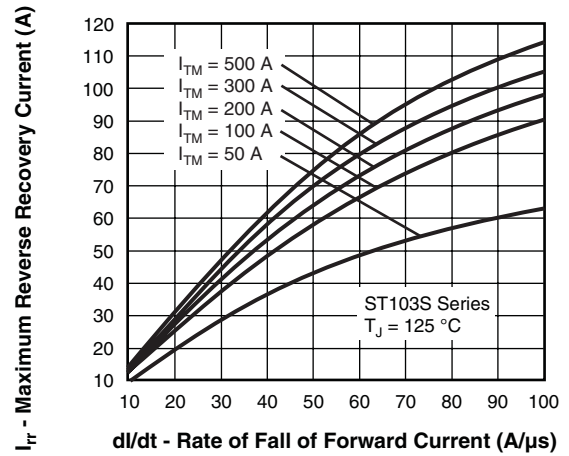


Fig. 10 - Reverse Recovery Current Characteristics

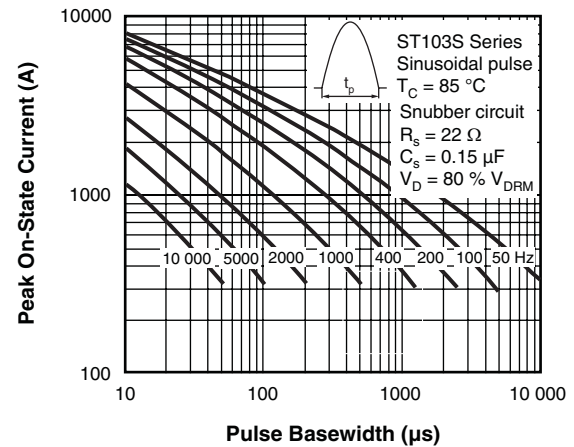
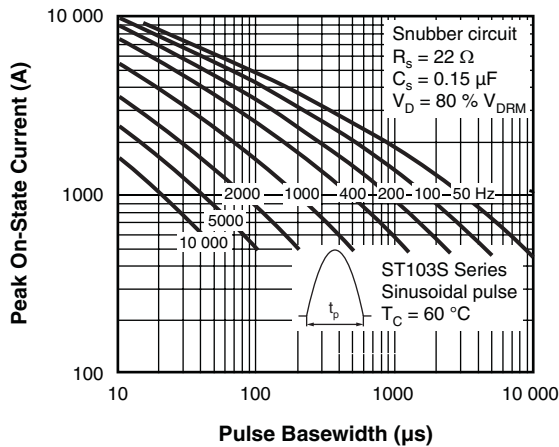


Fig. 11 - Frequency Characteristics

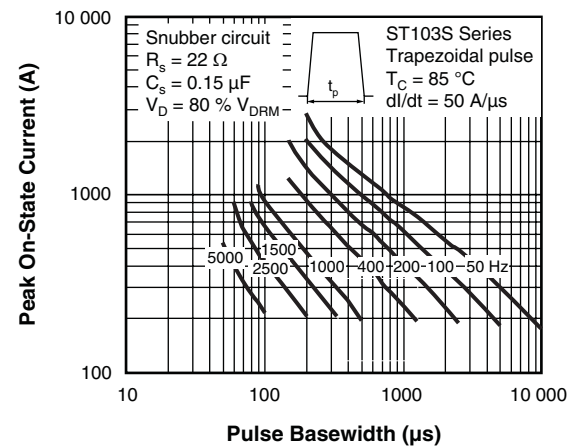
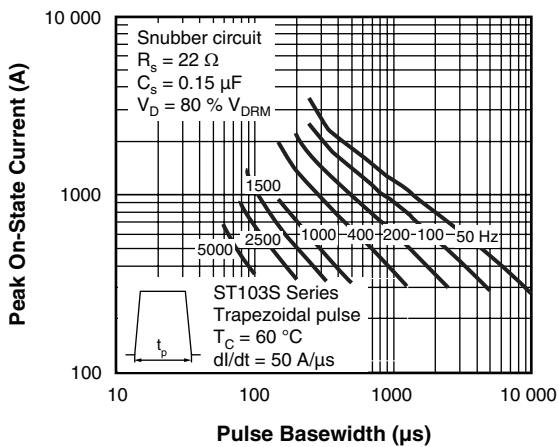


Fig. 12 - Frequency Characteristics

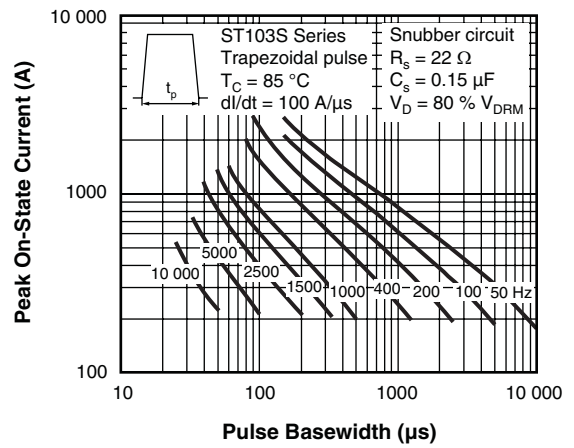
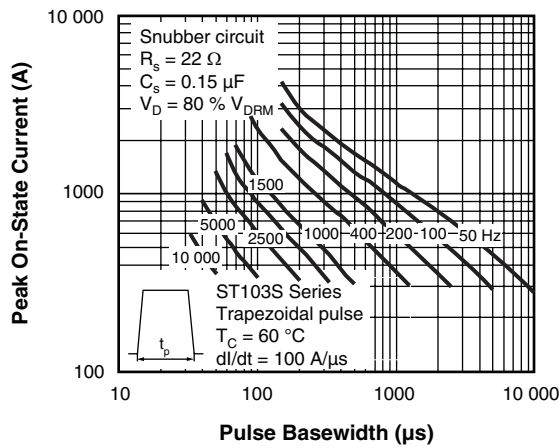


Fig. 13 - Frequency Characteristics

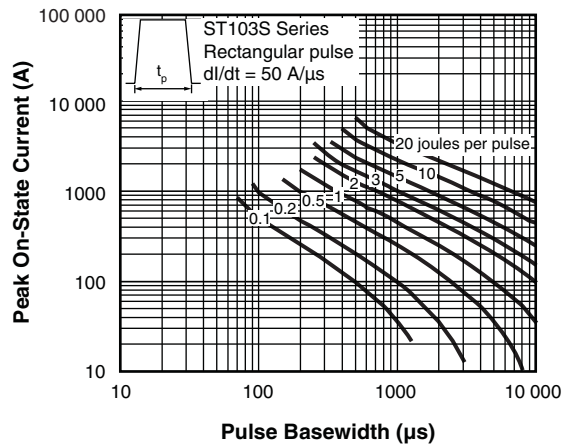
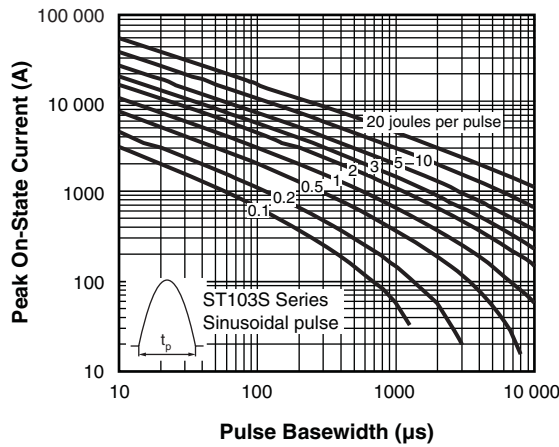


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

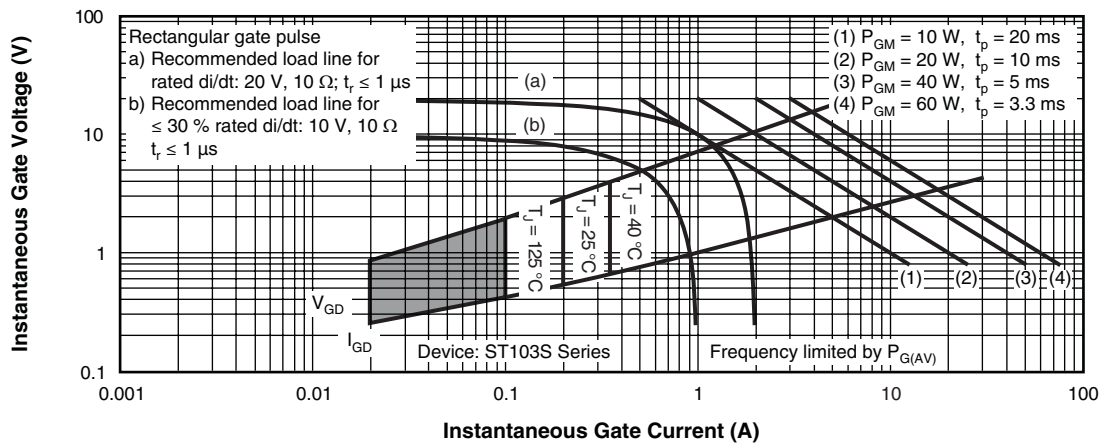


Fig. 15 - Gate Characteristics

# ST103SP Series



Vishay High Power Products Inverter Grade Thyristors  
(Stud Version), 105 A

## ORDERING INFORMATION TABLE

Device code	ST	10	3	S	08	P	F	N	0	P
	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩

- 1** - Thyristor
- 2** - Essential part number
- 3** - 3 = Fast turn-off
- 4** - S = Compression bonding stud
- 5** - Voltage code x 100 =  $V_{RRM}$  (see Voltage ratings table)
- 6** - P = Stud base 1/2"-20UNF-2A
- 7** - Reapplied dV/dt code (for  $t_q$  test conditions)
- 8** -  $t_q$  code
- 9** - 0 = Eyelet terminals  
(gate and aux. cathode leads)  
1 = Fast-on terminals  
(gate and aux. cathode leads)
- 10** - Lead (Pb)-free

dV/dt - $t_q$ combinations available					
dV/dt (V/ $\mu$ s)	20	50	100	200	400
10	CN	DN	EN	<b>FN*</b>	-
12	CM	DM	EM	FM	HM
15	CL	DL	EL	<b>FL*</b>	HL
18	CP	DP	EP	FP	HP
20	CK	DK	EK	FK	HK
25	-	-	-	-	HJ

\* Standard part number.  
All other types available only on request.

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95003">http://www.vishay.com/doc?95003</a>





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