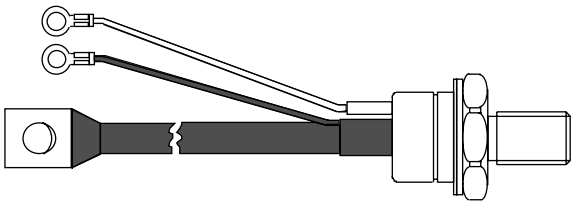
Inverter Grade Thyristors (Stud Version), 85 A



TO-209AC (TO-94)

FEATURES

- Center amplifying gate
- High surge current capability
- Low thermal impedance
- High speed performance
- Compression bonding
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level

Pb-free
RoHS COMPLIANT

TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

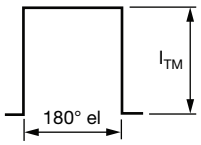
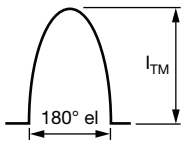
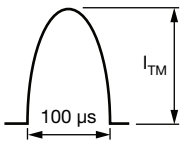
PRODUCT SUMMARY	
$I_{T(AV)}$	85 A

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		85	A
	T_C	85	°C
$I_{T(RMS)}$		135	A
I_{TSM}	50 Hz	2450	A
	60 Hz	2560	A
I^2t	50 Hz	30	kA^2s
	60 Hz	27	
V_{DRM}/V_{RRM}		400 to 1200	V
t_q	Range	10 to 20	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAX. AT $T_J = T_J$ MAX. mA
ST083S	04	400	500	30
	08	800	900	
	10	1000	1100	
	12	1200	1300	

CURRENT CARRYING CAPABILITY

FREQUENCY							UNITS
50 Hz	210	120	330	270	2540	1930	A
400 Hz	200	120	350	210	1190	810	
1000 Hz	150	80	320	190	630	400	
2500 Hz	70	25	220	85	250	100	
Recovery voltage V_r	50	50	50	50	50	50	V
Voltage before turn-on V_d	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current dI/dt	50	50	-	-	-	-	A/µs
Case temperature	60	85	60	85	60	85	°C
Equivalent values for RC circuit	22/0.15		22/0.15		22/0.15		W/µF

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			85	A
					85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 77 °C case temperature			135	A
Maximum peak, one half cycle, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	2450	
		t = 8.3 ms			2560	
		t = 10 ms	100 % V_{RRM} reapplied		2060	
		t = 8.3 ms			2160	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		30	kA^2s
		t = 8.3 ms			27	
		t = 10 ms	100 % V_{RRM} reapplied		21	
		t = 8.3 ms			19	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			300	$kA^2\sqrt{s}$
Maximum peak on-state voltage	V_{TM}	I_{TM} = 300 A, $T_J = T_J$ maximum, t_p = 10 ms sine wave pulse			2.15	V
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.46	
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.52	
Low level value of forward slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			2.32	mΩ
High level value of forward slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			2.34	
Maximum holding current	I_H	T_J = 25 °C, I_T > 30 A			600	mA
Typical latching current	I_L	T_J = 25 °C, V_A = 12 V, R_a = 6 Ω, I_G = 1 A			1000	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS
			MIN.	MAX.	
Maximum non-repetitive rate of rise of turned on current	dI/dt	$T_J = T_J$ max., V_{DRM} = Rated V_{DRM}, I_{TM} = 2 x dI/dt	1000		A/µs
Typical delay time	t_d	T_J = 25 °C, V_{DM} = Rated V_{DM}, I_{TM} = 50 A DC, t_p = 1 µs Resistive load, gate pulse: 10 V, 5 Ω source	0.80		µs
Maximum turn-off time	t_q	$T_J = T_J$ maximum, I_{TM} = 100 A, commutating dI/dt = 10 A/µs V_R = 50 V, t_p = 200 µs, dV/dt = 200 V/µs	10	20	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM}, higher value available on request	500	V/µs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA

TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, f = 50 Hz, d% = 50	40	W
Maximum average gate power	$P_{G(AV)}$		5	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	5	A
Maximum peak positive gate voltage	+ V_{GM}		20	V
Maximum peak negative gate voltage	- V_{GM}		5	
Maximum DC gate currrent required to trigger	I_{GT}	T_J = 25 °C, V_A = 12 V, R_a = 6 Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.195	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.08	
Mounting torque, ± 10 %		Non-lubricated threads	15.5 (137)	N · m (lbf · in)
		Lubricated threads	14 (120)	
Approximate weight			130	g
Case style		See dimensions - link at the end of datasheet	TO-209AC (TO-94)	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.034	0.025	$T_J = T_J$ maximum	K/W
120°	0.041	0.042		
90°	0.052	0.056		
60°	0.076	0.079		
30°	0.126	0.127		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

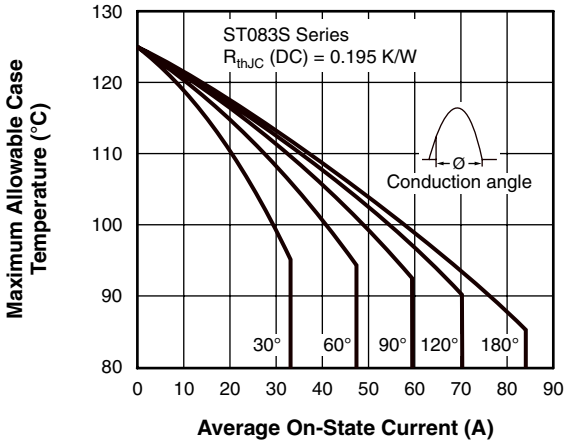


Fig. 1 - Current Ratings Characteristics

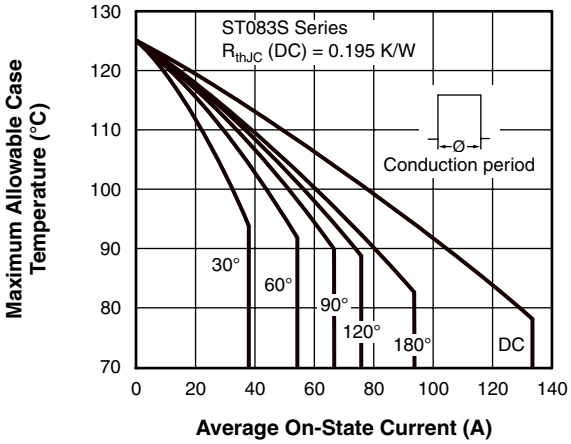
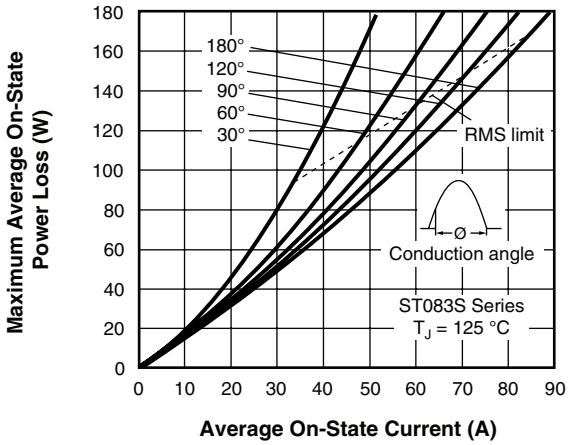


Fig. 2 - Current Ratings Characteristics



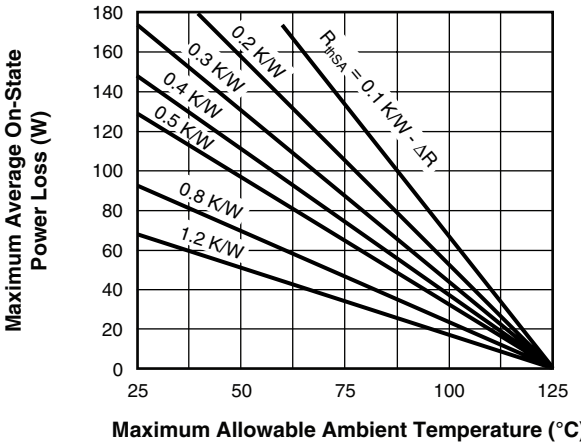
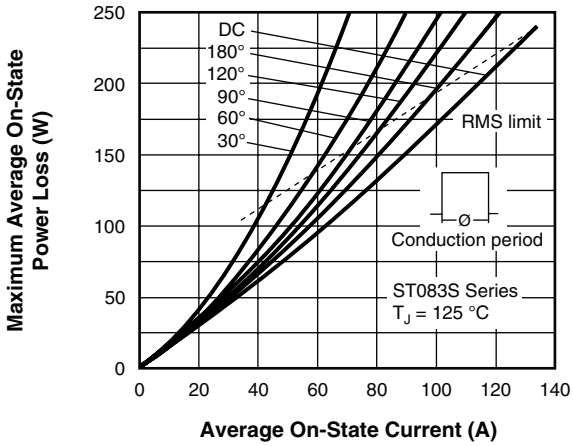


Fig. 3 - On-State Power Loss Characteristics



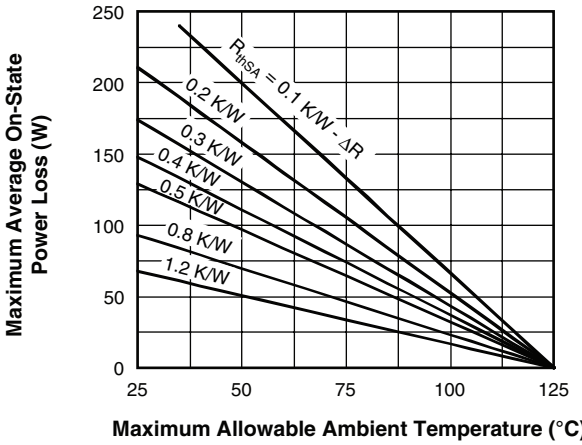


Fig. 4 - On-State Power Loss Characteristics

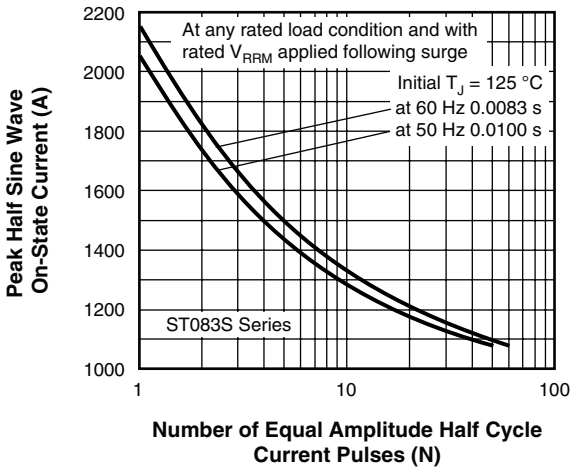


Fig. 5 - Maximum Non-Repetitive Surge Current

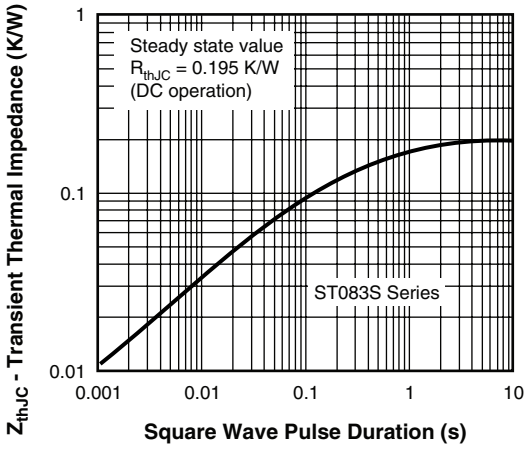


Fig. 8 - Thermal Impedance Z_{thJC} Characteristic

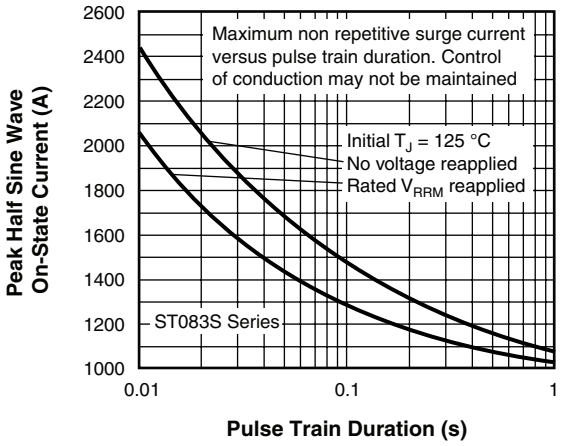


Fig. 6 - Maximum Non-Repetitive Surge Current

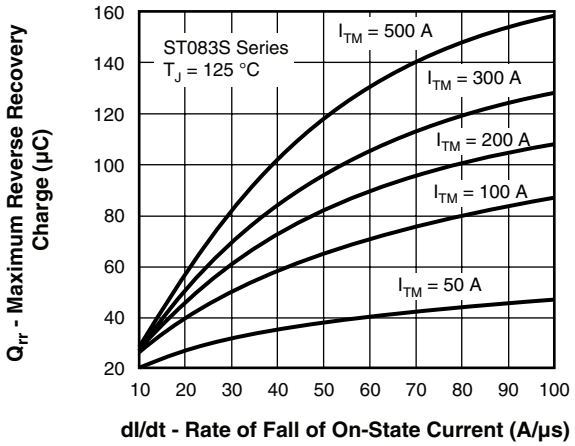


Fig. 9 - Reverse Recovered Charge Characteristics

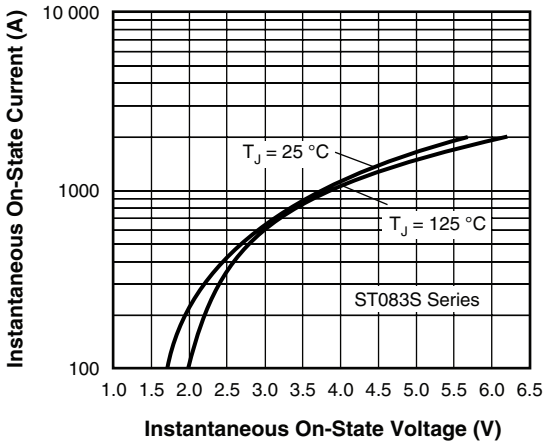


Fig. 7 - On-State Voltage Drop Characteristics

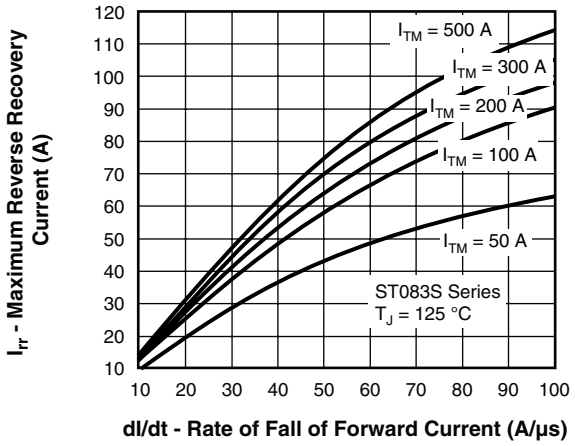


Fig. 10 - Reverse Recovery Current Characteristics

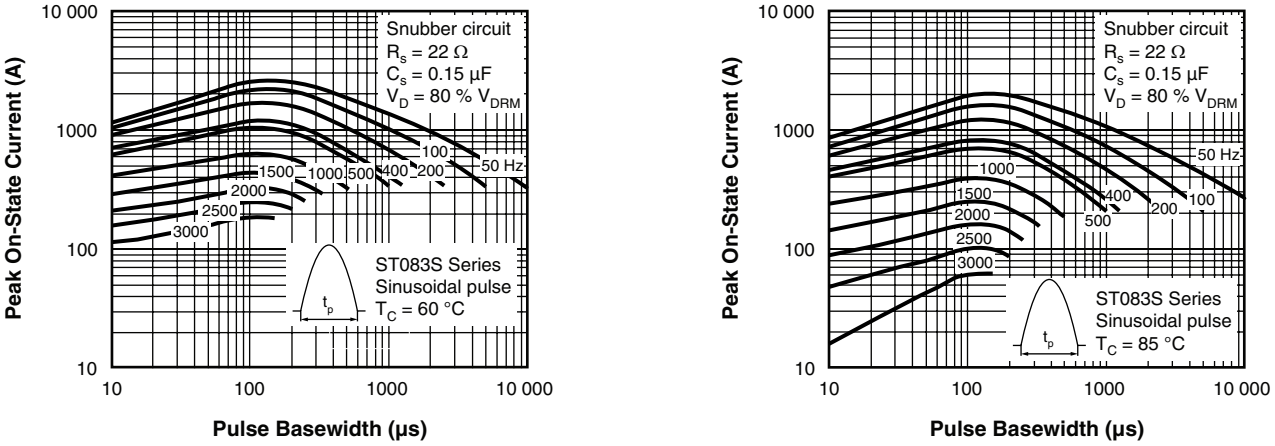


Fig. 11 - Frequency Characteristics

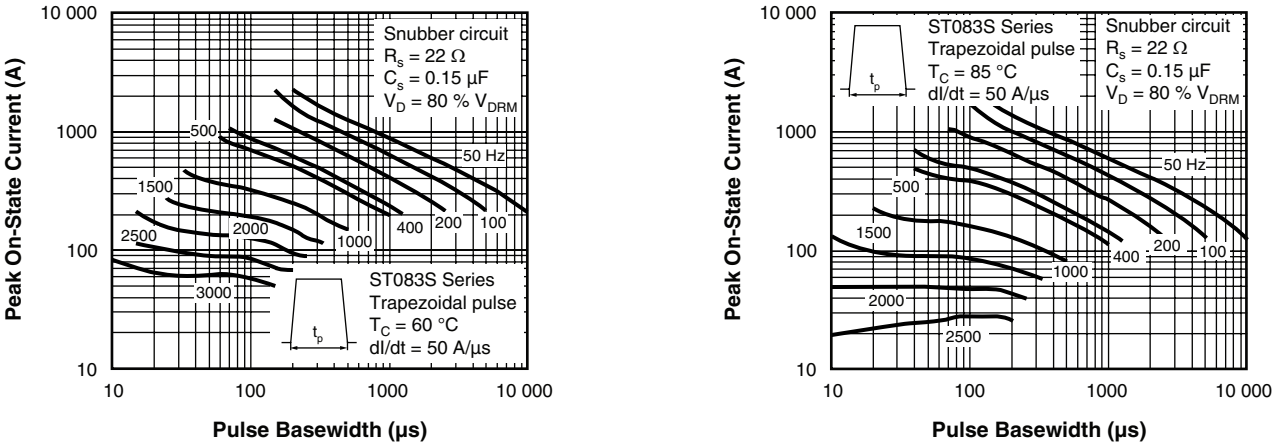


Fig. 12 - Frequency Characteristics

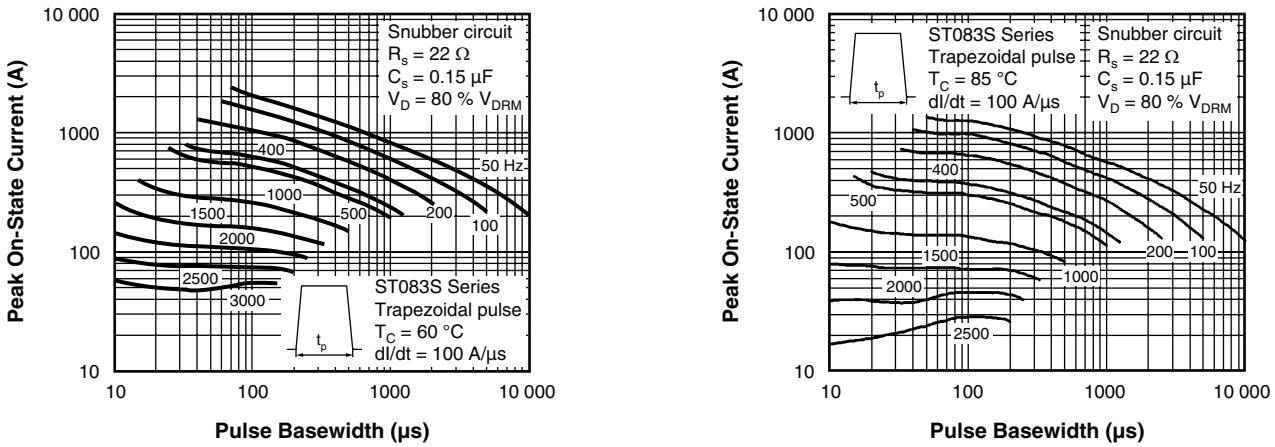


Fig. 13 - Frequency Characteristics

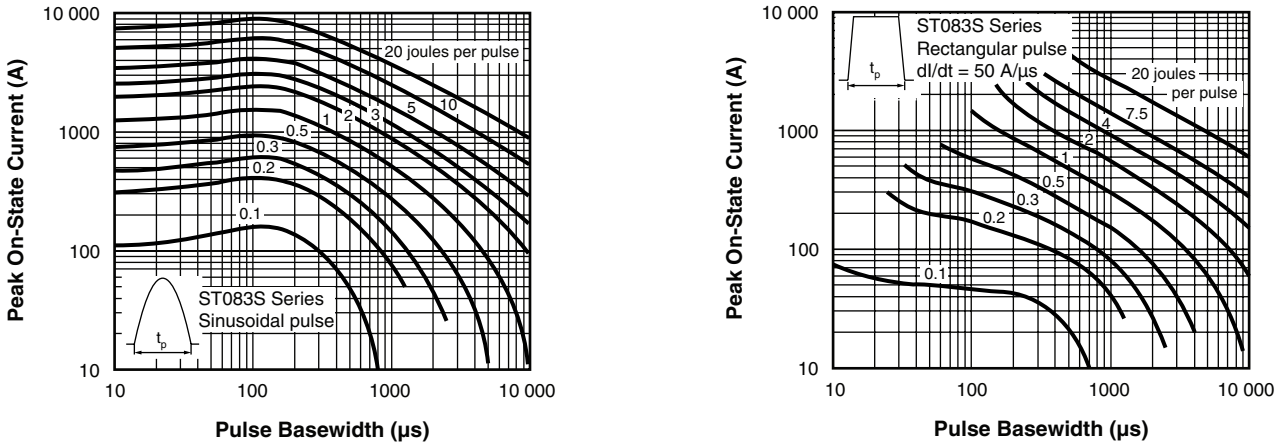


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

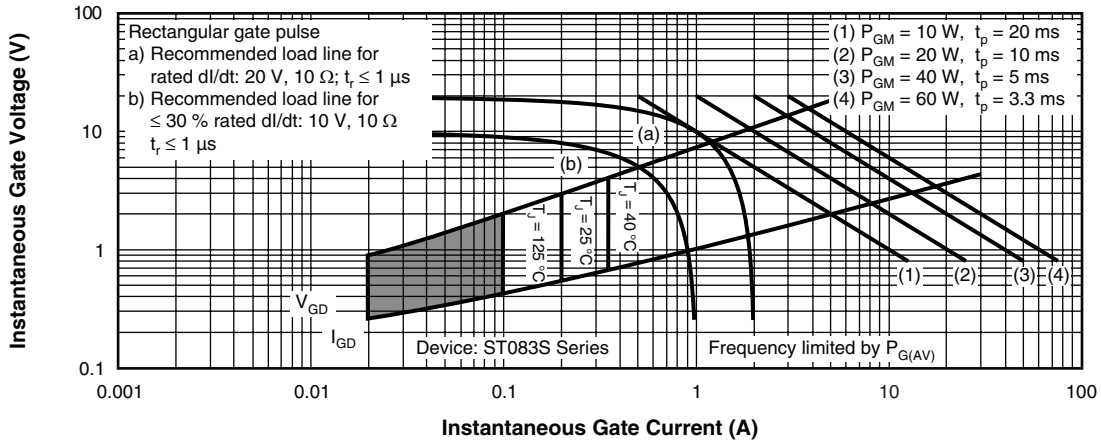


Fig. 15 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

ST	08	3	S	12	P	F	N	0	PbF
1	2	3	4	5	6	7	8	9	10

1 - Thyristor

2 - Essential part number

3 - 3 = Fast turn-off

4 - S = Compression bonding stud

5 - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)

6 - • P = Stud base 1/2"-20UNF-2A threads
• M = Metric M12, contact factory for availability

7 - Reapplied dV/dt code (for t_q test condition)

8 - t_q code

9 - • 0 = Eyelet terminals (gate and aux. cathode leads)
• 1 = Fast-on terminals (gate and aux. cathode leads)
• 2 = Flag terminals (gate and aux. cathode leads)

10 - PbF = Lead (Pb)-free

dV/dt - t_q combinations available		
	dV/dt (V/µs)	**200**
t_q (µs) up to 800V	10	FN
	20	FK
t_q (µs) only for 1000/1200 V	20	FK

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95003

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