

N-Channel 60-V (D-S) MOSFET

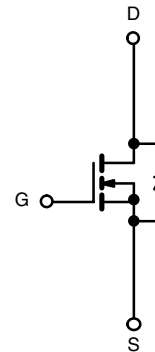
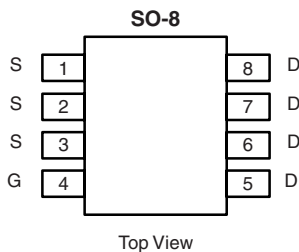
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
60	0.024 at $V_{GS} = 10$ V	7.5
	0.03 at $V_{GS} = 6.0$ V	6.5

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si4450DY-T1-E3 (Lead (Pb)-free)
Si4450DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	A
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	50	
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	W
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	°C/W

Notes:

a. Surface Mounted on FR4 board, $t \leq 10$ s.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

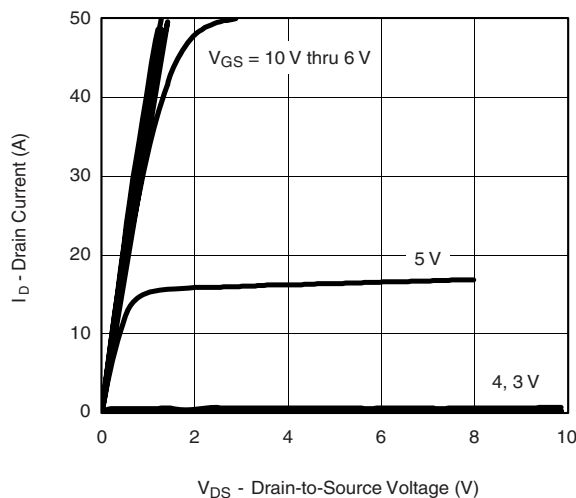
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$		0.020	0.024	Ω
		$V_{GS} = 6.0\text{ V}, I_D = 6.5\text{ A}$		0.025	0.03	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 7.5\text{ A}$		18.5		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$		31	50	nC
Gate-Source Charge	Q_{gs}			7.7		
Gate-Drain Charge	Q_{gd}			8.3		
Gate Resistance	R_g		1		5.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 30\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$		16	30	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			41	80	
Fall Time	t_f			21	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		46	80	

Notes:

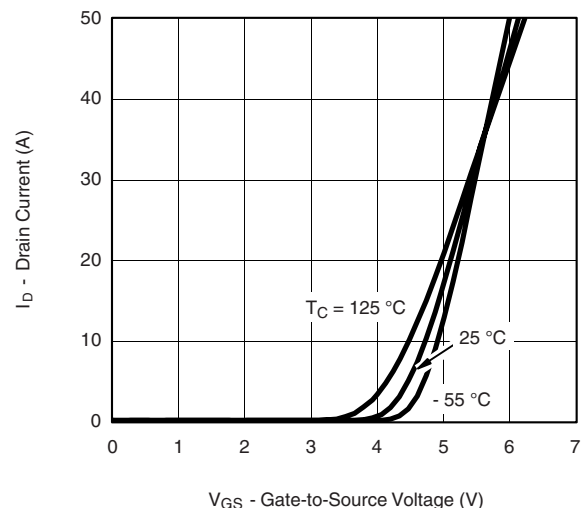
- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

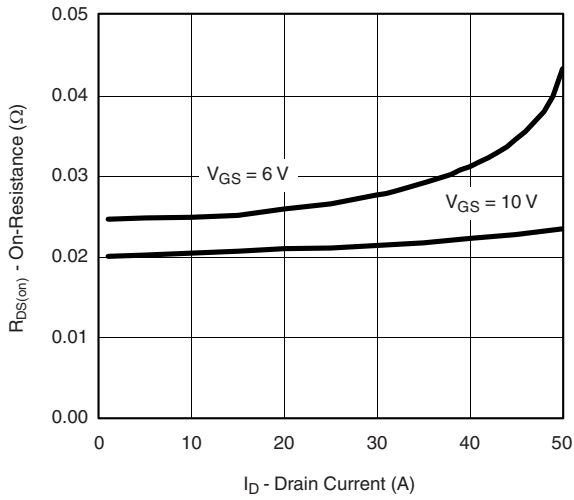


Output Characteristics

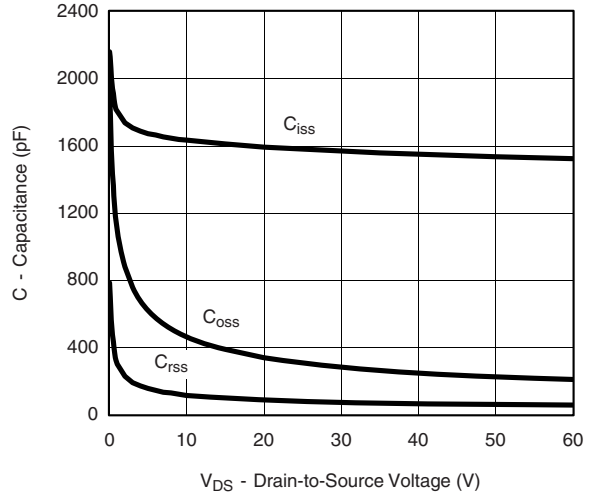


Transfer Characteristics

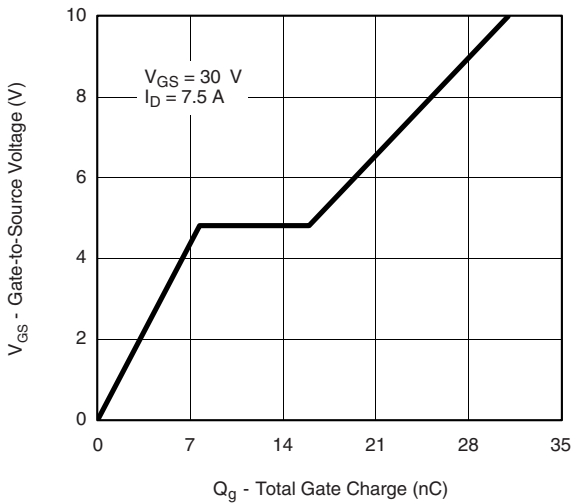
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



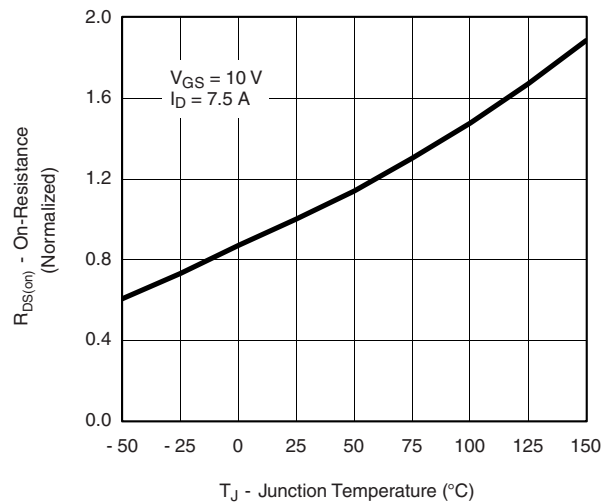
On-Resistance vs. Drain Current



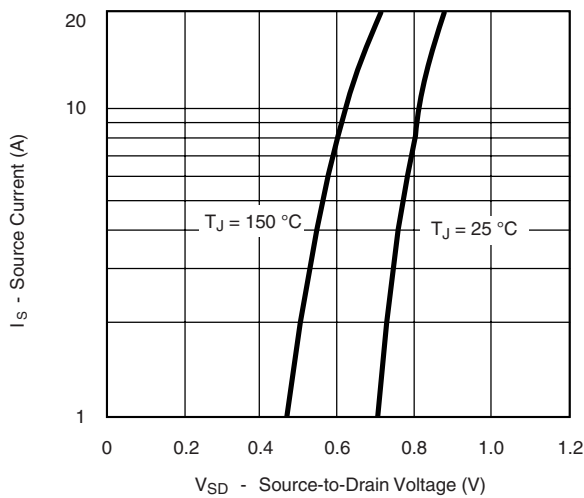
Capacitance



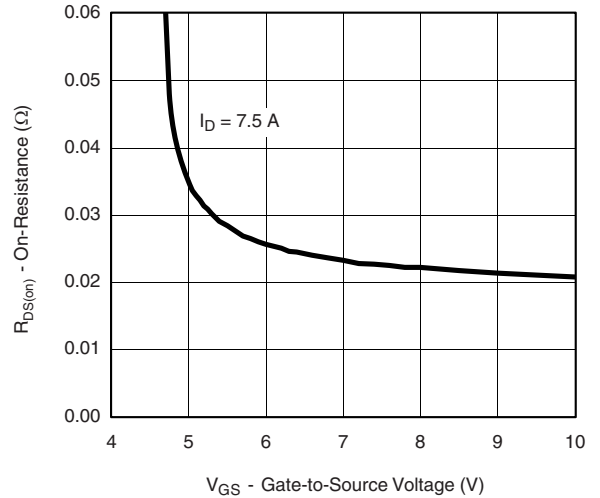
Gate Charge



On-Resistance vs. Junction Temperature

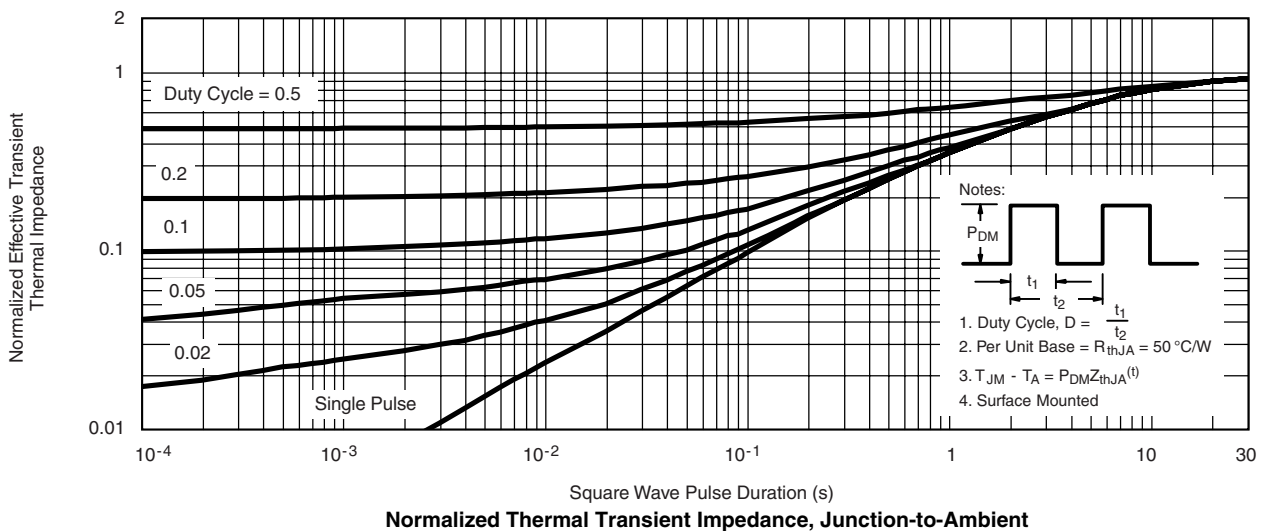
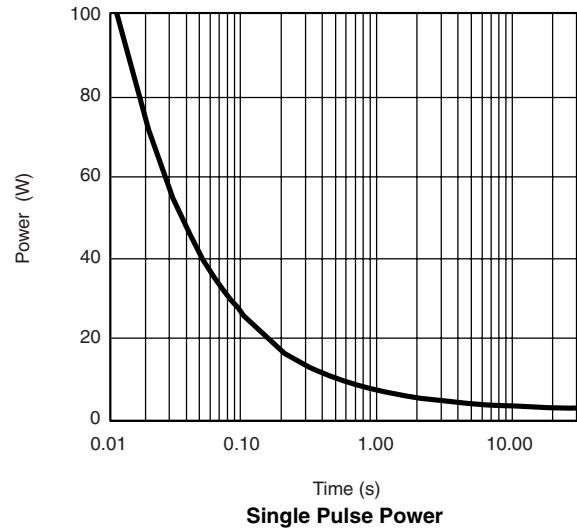
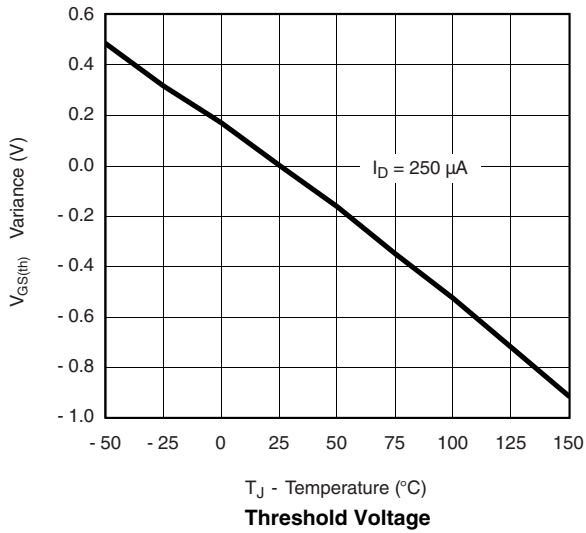


Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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